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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	122
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gu814-i-pl

TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES^(1,2) (CONTINUED)

Pin Number	Full Pin Name	Pin Number	Full Pin Name
E1	AN19/PWM6H/RPI52/RC4	J8	No Connect
E2	AN18/PWM6L/RPI51/RC3	J9	No Connect
E3	C1IN3-/SCK2/PMA5/RP118/RG6	J10	RP104/RF8
E4	AN17/PWM5H/RPI50/RC2	J11	D-/RG3 ⁽⁵⁾
E5	No Connect	K1	PGEC3/AN1/RPI33/RB1
E6	RP113/RG1	K2	PGED3/AN0/RPI32/RB0
E7	No Connect	K3	VREF+/RA10
K4	AN8/PMA6/RPI40/RB8	L3	AVss
K5	No Connect	L4	AN9/PMA7//RPI41/RB9
K6	RP108/RF12	L5	AN10/CVREF/PMA13/RPI42/RB10
K7	AN14/PMA1/RPI46/RB14	L6	RP109/RF13
K8	VDD	L7	AN13/PMA10/RPI45/RB13
K9	RP79/RD15	L8	AN15/PMA0/RPI47/RB15
K10	USBID/RP99/RF3	L9	RPI78/RD14
K11	RP98/RF2	L10	SDA2 ⁽³⁾ /PMA9/RP100/RF4
L1	PGEC1/AN6/RPI38/RB6	L11	SCL2 ⁽³⁾ /PMA8/RP101/RF5
L2	VREF-/RA9		

- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select”** for available peripherals and for information on limitations.
- 2:** Every I/O port pin (RAX-RGX) can be used as change notification (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- 3:** The availability of I²C™ interfaces varies by device. Selection (SDAX/SCLx or ASDAX/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.
- 4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.
- 5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES^(1,2)

Pin Number	Full Pin Name	Pin Number	Full Pin Name
A1	AN28/PMD4/RP84/RE4	E8	RPI31/RA15
A2	AN27/PMD3/RPI83/RE3	E9	RTCC/DMLN/RPI72/RD8
A3	RP125/RG13	E10	ASDA1 ⁽³⁾ /DPLN/RPI73/RD9
A4	AN24/PMD0/RP80/RE0	E11	RPI30/RA14
A5	RP112/RG0	F1	MCLR
A6	VCMPST2/RP97/RF1	F2	C2IN3-/SDO2/PMA3/RP120/RG8
A7	VDD	F3	C2IN1-/PMA2/RPI121/RG9
A8	No Connect	F4	C1IN1-/SDI2/PMA4/RPI119/RG7
A9	RPI76/RD12	F5	Vss
A10	DPH/RP66/RD2	F6	No Connect
A11	VCPCON/RP65/RD1	F7	No Connect
B1	No Connect	F8	VDD
B2	RP127/RG15	F9	OSC1/RPI60/RC12
B3	AN26/PMD2/RP82/RE2	F10	Vss
B4	AN25/PMD1/RPI81/RE1	F11	OSC2/CLKO/RC15
B5	AN23/RPI23/RA7	G1	AN20/RPI88/RE8
B6	VCMPST1/RP96/RF0	G2	AN21/RPI89/RE9
B7	VCAP	G3	TMS/RPI16/RA0
B8	PMRD/RP69/RD5	G4	No Connect
B9	PMBE/RP67/RD3	G5	VDD
B10	Vss	G6	Vss
B11	PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14	G7	Vss
C1	AN30/PMD6/RPI86/RE6	G8	No Connect
C2	VDD	G9	TDO/RPI21/RA5
C3	RPI124/RG12	G10	ASDA2 ⁽³⁾ /RPI19/RA3
C4	RP126/RG14	G11	TDI/RPI20/RA4
C5	AN22/RPI22/RA6	H1	AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5
C6	No Connect	H2	AN4/C1IN2-/USBOEN/RPI36/RB4
C7	C3IN1+/VCMPST3/RP71/RD7	H3	No Connect
C8	PMWR/RP68/RD4	H4	No Connect
C9	No Connect	H5	No Connect
C10	PGED2/SOSCI/C3IN3-/RPI61/RC13	H6	VDD
C11	PMCS1/RPI75/RD11	H7	No Connect
D1	AN16/RPI49/RC1	H8	VBUS
D2	AN31/PMD7/RP87/RE7	H9	VUSB3V3
D3	AN29/PMD5/RP85/RE5	H10	D+/RG2 ⁽⁴⁾
D4	No Connect	H11	ASCL2 ⁽³⁾ /RPI18/RA2
D5	No Connect	J1	AN3/C2IN1+/VP10/RPI35/RB3
D6	No Connect	J2	AN2/C2IN2-/VMIO/RPI34/RB2
D7	C3IN2-/RP70/RD6	J3	PGED1/AN7/RCV/RPI39/RB7
D8	RPI77/RD13	J4	AVDD
D9	INT0/DMH/RP64/RD0	J5	AN11/PMA12/RPI43/RB11
D10	No Connect	J6	TCK/RPI17/RA1
D11	ASCL1 ⁽³⁾ /PMCS2/RPI74/RD10	J7	AN12/PMA11/RPI44/RB12

- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as change notification (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** The availability of I²C™ interfaces varies by device. Selection (SDAX/SCLx or ASDAX/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.
- Note 4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.
- Note 5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

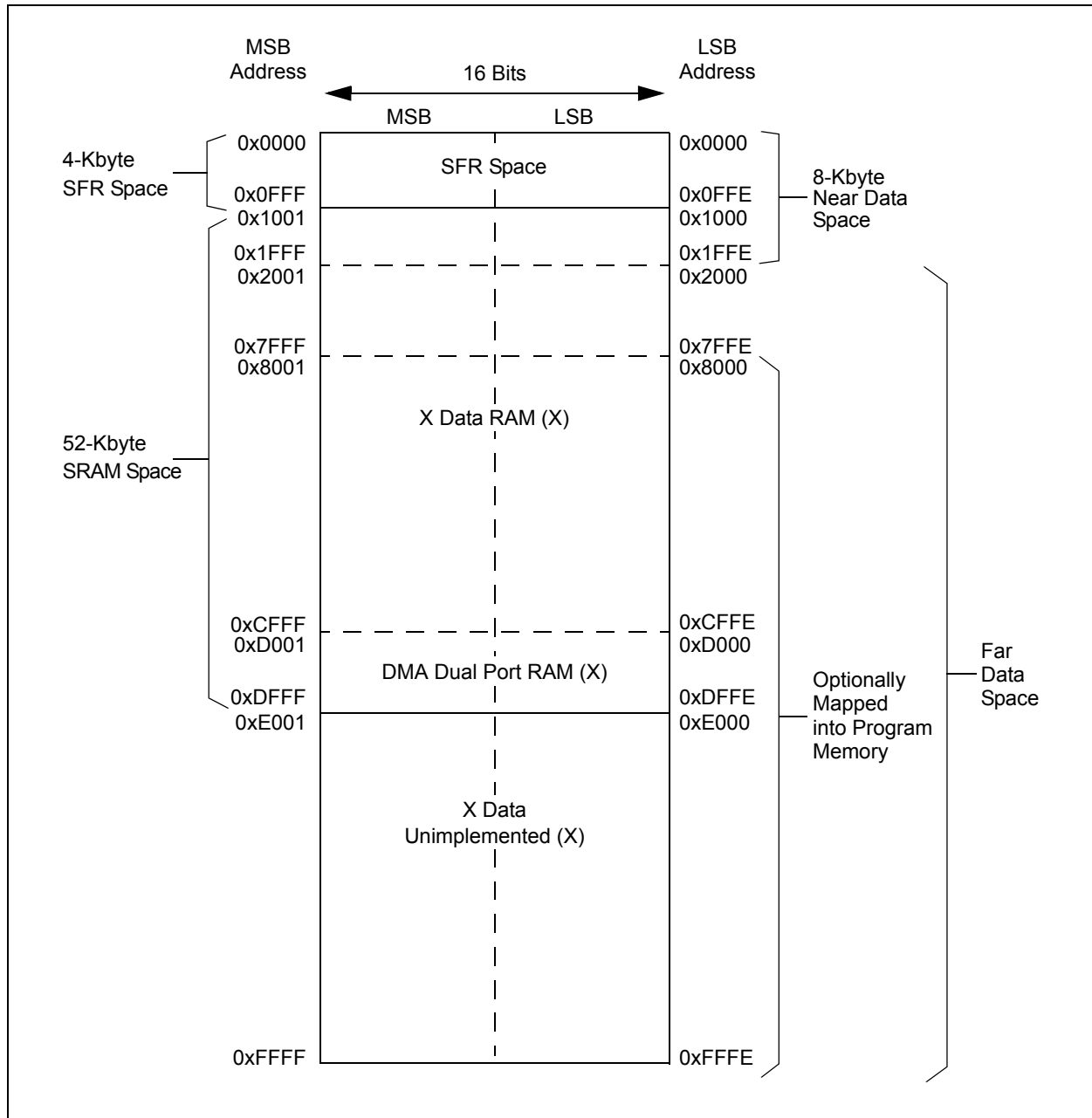
FIGURE 4-4: DATA MEMORY MAP FOR PIC24EP512(GP/GU)806/810/814 DEVICES WITH 52-KBYTE RAM

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	DMA4IF	PMPIF	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	RTCIF	DMA5IF	DCIIF	DCIEIF	QE11IF	PSEMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	—	—	QE12IF	—	PSESMIF	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	IC9IF	OC9IF	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	USB1IF	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	IC11IF	OC11IF	IC10IF	OC10IF	SPI4IF	SPI4EIF	DMA11IF	DMA10IF	DMA9IF	DMA8IF	—	—	—	—	—	—	0000
IFS8	0810	—	ICDIF	IC16IF	OC16IF	IC15IF	OC15IF	IC14IF	OC14IF	IC13IF	OC13IF	—	DMA14IF	DMA13IF	DMA12IF	IC12IF	OC12IF	0000
IEC0	0820	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	DMA4IE	PMPIE	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	RTCIE	DMA5IE	DCIIE	DCIEIE	QE11IE	PSEMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	—	—	QE12IE	—	PSESMIE	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	IC9IE	OC9IE	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	USB1IE	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	IC11IE	OC11IE	IC10IE	OC10IE	SPI4IE	SPI4EIE	DMA11IE	DMA10IE	DMA9IE	DMA8IE	—	—	—	—	—	—	0000
IEC8	0830	—	ICDIE	IC16IE	OC16IE	IC15IE	OC15IE	IC14IE	OC14IE	IC13IE	OC13IE	—	DMA14IE	DMA13IE	DMA12IE	IC12IE	OC12IE	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	NVMIP<2:0>			—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			4444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	IC8IP<2:0>			—	IC7IP<2:0>			—	AD2IP<2:0>			—	INT1IP<2:0>			4444
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	IC5IP<2:0>			—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			4444
IPC10	0854	—	OC7IP<2:0>			—	OC6IP<2:0>			—	OC5IP<2:0>			—	IC6IP<2:0>			4444
IPC11	0856	—	T6IP<2:0>			—	DMA4IP<2:0>			—	PMPIP<2:0>			—	OC8IP<2:0>			4444
IPC12	0858	—	T8IP<2:0>			—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	T7IP<2:0>			4444
IPC13	085A	—	C2RXIP<2:0>			—	INT4IP<2:0>			—	INT3IP<2:0>			—	T9IP<2:0>			4444
IPC14	085C	—	DCIEIP<2:0>			—	QE11IP<2:0>			—	PSEMIP<2:0>			—	C2IP<2:0>			4444
IPC15	085E	—	—	—	—	—	RTCIP<2:0>			—	DMA5IP<2:0>			—	DCIIP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	INT3R<6:0>							—	INT2R<6:0>							0000
RPINR2	06A4	—	—	—	—	—	—	—	—	—	INT4R<6:0>							0000
RPINR3	06A6	—	T3CKR<6:0>							—	T2CKR<6:0>							0000
RPINR4	06A8	—	T5CKR<6:0>							—	T4CKR<6:0>							0000
RPINR5	06AA	—	T7CKR<6:0>							—	T6CKR<6:0>							0000
RPINR6	06AC	—	T9CKR<6:0>							—	T8CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR9	06B2	—	IC6R<6:0>							—	IC5R<6:0>							0000
RPINR10	06B4	—	IC8R<6:0>							—	IC7R<6:0>							0000
RPINR11	06B6	—	OCFBR<6:0>							—	OCFAR<6:0>							0000
RPINR18	06C4	—	U1CTSR<6:0>							—	U1RXR<6:0>							0000
RPINR19	06C6	—	U2CTSR<6:0>							—	U2RXR<6:0>							0000
RPINR20	06C8	—	SCK1R<6:0>							—	SDI1R<6:0>							0000
RPINR21	06CA	—	—	—	—	—	—	—	—	—	SS1R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR26	06D4	—	C2RXR<6:0>							—	C1RXR<6:0>							0000
RPINR27	06D6	—	U3CTSR<6:0>							—	U3RXR<6:0>							0000
RPINR28	06D8	—	U4CTSR<6:0>							—	U4RXR<6:0>							0000
RPINR29	06DA	—	SCK3R<6:0>							—	SDI3R<6:0>							0000
RPINR30	06DC	—	—	—	—	—	—	—	—	—	SS3R<6:0>							0000
RPINR31	06DE	—	SCK4R<6:0>							—	SDI4R<6:0>							0000
RPINR32	06E0	—	—	—	—	—	—	—	—	—	SS4R<6:0>							0000
RPINR33	06E2	—	IC10R<6:0>							—	IC9R<6:0>							0000
RPINR34	06E4	—	IC12R<6:0>							—	IC11R<6:0>							0000
RPINR35	06E6	—	IC14R<6:0>							—	IC13R<6:0>							0000
RPINR36	06E8	—	IC16R<6:0>							—	IC15R<6:0>							0000
RPINR37	06EA	—	—	—	—	—	—	—	—	—	OCFCR<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit 1 = Device was in Idle mode 0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupts and associated IE bits are enabled
0 = Interrupts are disabled, but traps are still enabled
- bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active
- bit 13 **SWTRAP:** Software Trap Status bit
1 = Software trap is enabled
0 = Software trap is disabled
- bit 12-5 **Unimplemented:** Read as '0'
- bit 4 **INT4EP:** External Interrupt 4 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge
- bit 3 **INT3EP:** External Interrupt 3 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge
- bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge
- bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge
- bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PWCOL14	PWCOL13	PWCOL12	PWCOL11	PWCOL10	PWCOL9	PWCOL8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **PWCOL14:** Channel 14 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 13 **PWCOL13:** Channel 13 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 12 **PWCOL12:** Channel 12 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 11 **PWCOL11:** Channel 11 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 10 **PWCOL10:** Channel 10 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 9 **PWCOL9:** Channel 9 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 8 **PWCOL8:** Channel 8 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 7 **PWCOL7:** Channel 7 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 6 **PWCOL6:** Channel 6 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 5 **PWCOL5:** Channel 5 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 4 **PWCOL4:** Channel 4 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected
- bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

9.1 CPU Clocking System

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices provides seven system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- Low-Power RC (LPRC) Oscillator
- FRC Oscillator with postscaler

Instruction execution speed or device operating frequency, F_{CY} , is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

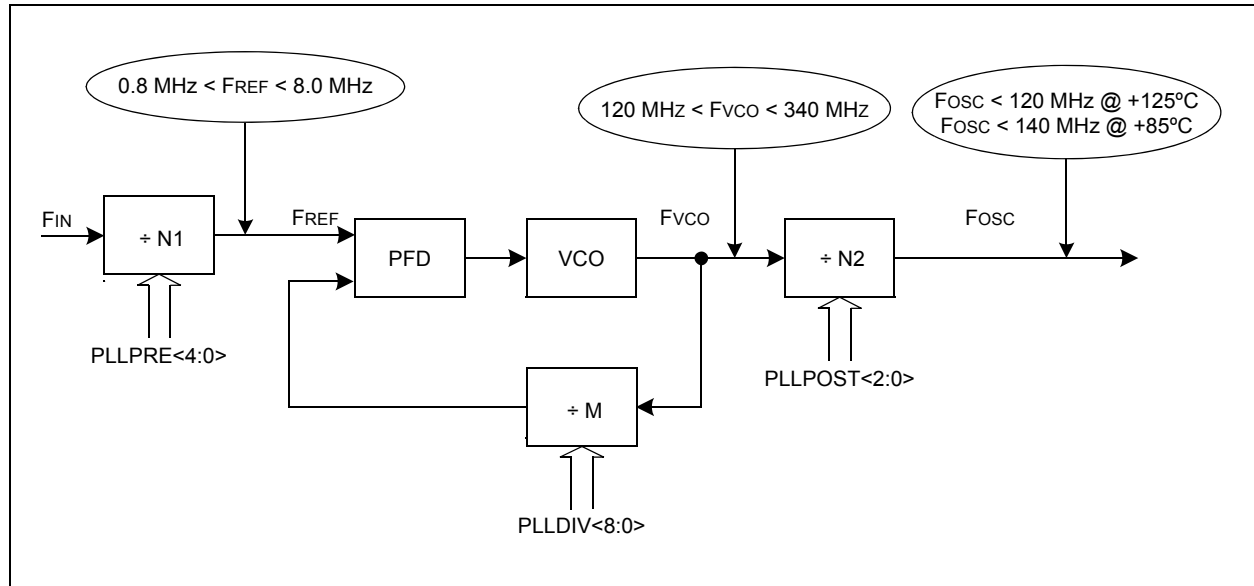
$$F_{CY} = F_{OSC}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relation between input frequency (F_{IN}) and output frequency (F_{OSC}).

Equation 9-3 provides the relation between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 9-2: PLL BLOCK DIAGRAM



EQUATION 9-2: F_{OSC} CALCULATION

$$F_{OSC} = F_{IN} \times \left(\frac{M}{N1 \times N2} \right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)} \right)$$

Where,

$$N1 = PLLPRE + 2$$

$$N2 = 2 \times (PLLPOST + 1)$$

$$M = PLLDIV + 2$$

EQUATION 9-3: F_{VCO} CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1} \right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)} \right)$$

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

bit 3	CF: Clock Fail Detect bit (read/clear by application) 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure
bit 2	Unimplemented: Read as '0'
bit 1	LPOSCEN: Secondary (LP) Oscillator Enable bit 1 = Enables Secondary Oscillator 0 = Disables Secondary Oscillator
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"* (available from the Microchip web site) for details.
- 2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
- 3:** This register resets only on a Power-on Reset (POR).

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER⁽²⁾

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE<2:0> ⁽³⁾			DOZEN ^(1,4)	FRCDIV<2:0>		
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST<1:0>		—	PLLPRE<4:0>				
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit and the processor clock and peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit
- bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits⁽³⁾
111 = Fcy divided by 128
110 = Fcy divided by 64
101 = Fcy divided by 32
100 = Fcy divided by 16
011 = Fcy divided by 8 (default)
010 = Fcy divided by 4
001 = Fcy divided by 2
000 = Fcy divided by 1
- bit 11 **DOZEN:** Doze Mode Enable bit^(1,4)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio forced to 1:1
- bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)
- bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4 (default)
00 = Output divided by 2
- bit 5 **Unimplemented:** Read as '0'

- Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.
Note 2: This register resets only on a Power-on Reset (POR).
Note 3: DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
Note 4: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 11-5: RPNR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T5CKR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T4CKR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T5CKR<6:0>:** Assign Timer5 External Clock (T5CK) to the Corresponding RPN/RPN Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T4CKR<6:0>:** Assign Timer4 External Clock (T4CK) to the Corresponding RPN/RPN Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-57: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP113R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP118R<5:0>**: Peripheral Output Function is Assigned to RP118 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP113R<5:0>**: Peripheral Output Function is Assigned to RP113 Output Pin bits
(see Table 11-3 for peripheral function numbers)**REGISTER 11-58: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP125R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'bit 13-8 **RP125R<5:0>**: Peripheral Output Function is Assigned to RP125 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **RP120R<5:0>**: Peripheral Output Function is Assigned to RP120 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 17-4: POSxCNTH: POSITION COUNTER x HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSCNT<31:16>**: High Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-5: POSxCNTL: POSITION COUNTER x LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSCNT<15:0>**: Low Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **POSHLD<15:0>**: Hold Register for Reading and Writing POSxCNTH bits

REGISTER 22-7: UxADDR: USB ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
LSPDEN ⁽¹⁾	DEVADDR<6:0>							
bit 7								bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7 **LSPDEN:** USB Low-Speed Enable Indicator bit⁽¹⁾
 1 = USB module operates at low-speed
 0 = USB module operates at full-speed
 bit 6-0 **DEVADDR<6:0>:** USB Device Address bits

Note 1: Host mode only. In Device mode, this bit is unimplemented.

REGISTER 22-8: UxTOK: USB TOKEN REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PID<3:0> ⁽¹⁾				EP<3:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'
 bit 7-4 **PID<3:0>:** Token Type Identifier bits⁽¹⁾
 1101 = SETUP (TX) token type transaction
 1001 = IN (RX) token type transaction
 0001 = OUT (TX) token type transaction
 bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
 This value must specify a valid endpoint on the attached device.

Note 1: All other combinations are reserved and are not to be used.

REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE15	RSE14	RSE13	RSE12	RSE11	RSE10	RSE9	RSE8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE7	RSE6	RSE5	RSE4	RSE3	RSE2	RSE1	RSE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **RSE<15:0>**: Receive Slot Enable bits

1 = CSDI data is received during the individual time slot n

0 = CSDI data is ignored during the individual time slot n

REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE15	TSE14	TSE13	TSE12	TSE11	TSE10	TSE9	TSE8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE7	TSE6	TSE5	TSE4	TSE3	TSE2	TSE1	TSE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TSE<15:0>**: Transmit Slot Enable Control bits

1 = Transmit buffer contents are sent during the individual time slot n

0 = CSDO pin is tri-stated or driven to logic '0' during the individual time slot, depending on the state of the CSDOM bit

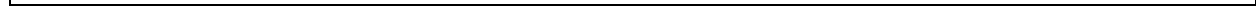
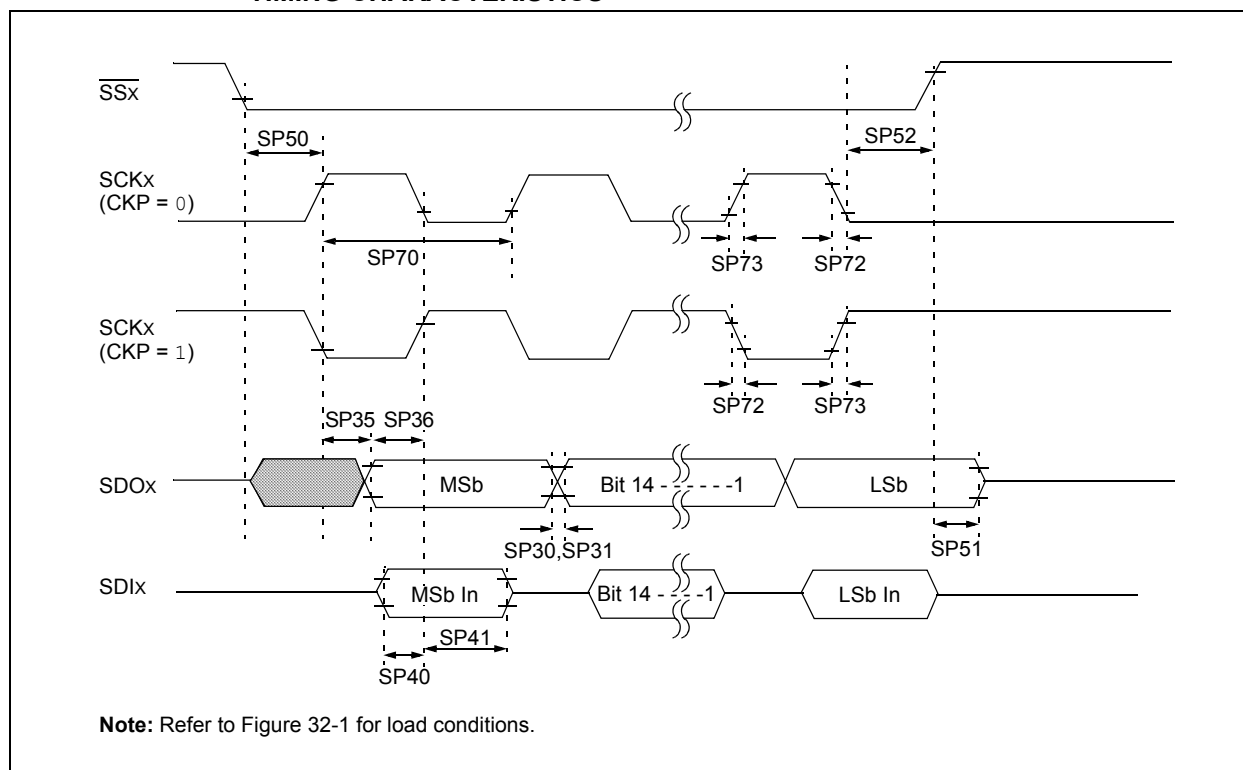


FIGURE 32-21: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



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