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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	122
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep256gu814t-i-ph

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TABLE 4-34: PARALLEL MASTER/SLAVE PORT REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON	0600	PMPEN	—	PSIDL	ADRMUX<1:0>		PTBEEN	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	BEP	WRSP	RDSP	0000
PMMODE	0602	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>			WAITE<1:0>			0000
PMADDR ⁽¹⁾	0604	CS2	CS1	Parallel Port Address (ADDR<13:0>)														0000
PMDOUT1 ⁽¹⁾	0604	Parallel Port Data Out Register 1 (Buffers Level 0 and 1)																0000
PMDOUT2	0606	Parallel Port Data Out Register 2 (Buffers Level 2 and 3)																0000
PMDIN1	0608	Parallel Port Data In Register 1 (Buffers Level 0 and 1)																0000
PMDIN2	060A	Parallel Port Data In Register 2 (Buffers Level 2 and 3)																0000
PMAEN	060C	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000
PMSTAT	060E	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the PMP module.

Note 1: PMADDR and PMDOUT1 are the same physical register, but are defined differently depending on the module's operating mode.

TABLE 4-35: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL	VWORD<4:0>					CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—	0000
CRCCON2	0642	—	—	—	DWIDTH<4:0>					—	—	—	PLEN<4:0>					0000
CRCXORL	0644	X<15:1>															—	0000
CRCXORH	0646	X<31:16>																0000
CRCDATL	0648	CRC Data Input Low Word																0000
CRCDATH	064A	CRC Data Input High Word																0000
CRCWDATL	064C	CRC Result Low Word																0000
CRCWDATH	064E	CRC Result High Word																0000

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-36: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	0620	Alarm Value Register Window based on ALRMPTR<1:0>																xxxx
ALCFGRPT	0622	ALRMEN	CHIME	AMASK<3:0>				ALRMPTR<1:0>		ARPT<7:0>							0000	
RTCVAL	0624	RTCC Value Register Window based on RTCPTR<1:0>																xxxx
RCFGCAL	0626	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR<1:0>			CAL<7:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The **TBLRDL** and **TBLWTL** instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through data space. The **TBLRDH** and **TBLWTH** instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. **TBLRDL** and **TBLWTL** access the space that contains the least significant data word. **TBLRDH** and **TBLWTH** access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- **TBLRDL** (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location ($P<15:0>$) to a data address ($D<15:0>$).

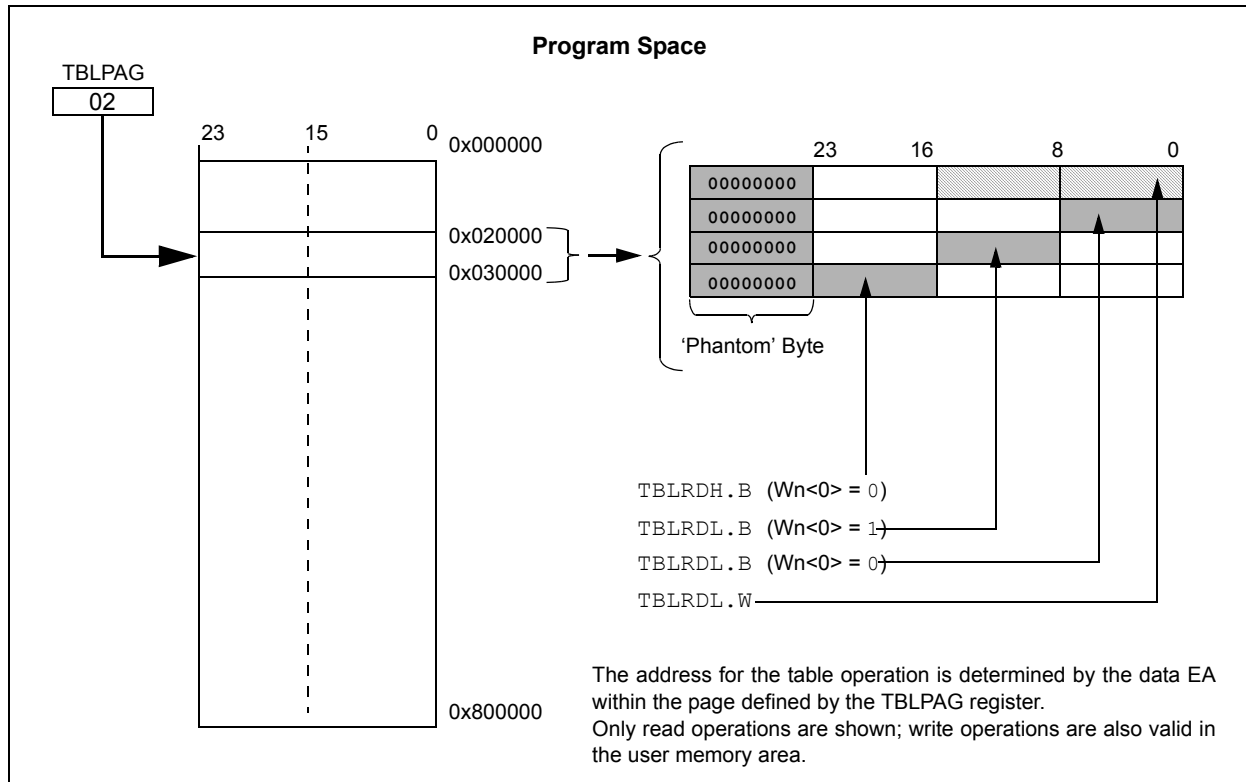
- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- **TBLRDH** (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address ($P<23:16>$) to a data address. The 'phantom' byte ($D<15:8>$), is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to $D<7:0>$ of the data address, in the **TBLRDL** instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, **TBLWTH** and **TBLWTL**, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (**TBLPAG**). **TBLPAG** covers the entire program memory space of the device, including user application and configuration spaces. When $TBLPAG<7> = 0$, the table page is located in the user memory space. When $TBLPAG<7> = 1$, the page is located in configuration space.

FIGURE 4-13: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. “Flash Programming”** (DS70609) of the “dsPIC33E/PIC24E Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

- 2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming

pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{\text{MCLR}}$). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user application can write program memory data either in blocks or ‘rows’ of 128 instructions (384 bytes) at a time or a single program memory word, and erase program memory in blocks or ‘pages’ of 1024 instructions (3072 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS

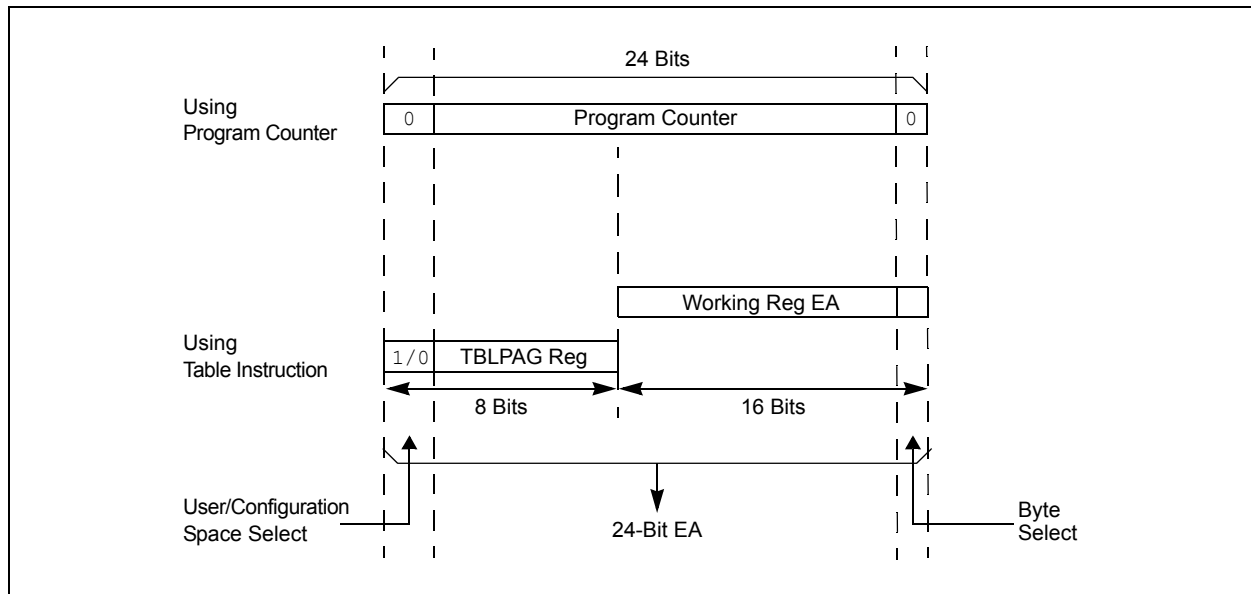


TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
USB1 – USB OTG Interrupt ⁽²⁾	94	86	0x0000C0	IFS5<6>	IEC5<6>	IPC21<10:8>
U4E – UART4 Error Interrupt	95	87	0x0000C2	IFS5<7>	IEC5<7>	IPC21<14:12>
U4RX – UART4 Receiver	96	88	0x0000C4	IFS5<8>	IEC5<8>	IPC22<2:0>
U4TX – UART4 Transmitter	97	89	0x0000C6	IFS5<9>	IEC5<9>	IPC22<6:4>
SPI3E – SPI3 Error	98	90	0x0000C8	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 – SPI3 Transfer Done	99	91	0x0000CA	IFS5<11>	IEC5<11>	IPC22<14:12>
OC9 – Output Compare 9	100	92	0x0000CC	IFS5<12>	IEC5<12>	IPC23<2:0>
IC9 – Input Capture 9	101	93	0x0000CE	IFS5<13>	IEC5<13>	IPC23<6:4>
PWM1 – PWM Generator 1 ⁽¹⁾	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>
PWM2 – PWM Generator 2 ⁽¹⁾	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>
PWM3 – PWM Generator 3 ⁽¹⁾	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>
PWM4 – PWM Generator 4 ⁽¹⁾	105	97	0x0000D6	IFS6<1>	IEC6<1>	IPC24<6:4>
PWM5 – PWM Generator 5 ⁽¹⁾	106	98	0x0000D8	IFS6<2>	IEC6<2>	IPC24<10:8>
PWM6 – PWM Generator 6 ⁽¹⁾	107	99	0x0000DA	IFS6<3>	IEC6<3>	IPC24<14:12>
PWM7 – PWM Generator 7 ⁽¹⁾	108	100	0x0000DC	IFS6<4>	IEC6<4>	IPC25<2:0>
Reserved	109-125	101-117	0x0000DE-0x0000FC	—	—	—
DMA8 – DMA Channel 8	126	118	0x000100	IFS7<6>	IEC7<6>	IPC29<10:8>
DMA9 – DMA Channel 9	127	119	0x000102	IFS7<7>	IEC7<7>	IPC29<14:12>
DMA10 – DMA Channel 10	128	120	0x000104	IFS7<8>	IEC7<8>	IPC30<2:0>
DMA11 – DMA Channel 11	129	121	0x000106	IFS7<9>	IEC7<9>	IPC30<6:4>
SPI4E – SPI4 Error	130	122	0x000108	IFS7<10>	IEC7<10>	IPC30<10:8>
SPI4 – SPI4 Transfer Done	131	123	0x00010A	IFS7<11>	IEC7<11>	IPC30<14:12>
OC10 – Output Compare 10	132	124	0x00010C	IFS7<12>	IEC7<12>	IPC31<2:0>
IC10 – Input Capture 10	133	125	0x00010E	IFS7<13>	IEC7<13>	IPC31<6:4>
OC11 – Output Compare 11	134	126	0x000110	IFS7<14>	IEC7<14>	IPC31<10:8>
IC11 – Input Capture 11	135	127	0x000112	IFS7<15>	IEC7<15>	IPC31<14:12>
OC12 – Output Compare 12	136	128	0x000114	IFS8<0>	IEC8<0>	IPC32<2:0>
IC12 – Input Capture 12	137	129	0x000116	IFS8<1>	IEC8<1>	IPC32<6:4>
DMA12 – DMA Channel 12	138	130	0x000118	IFS8<2>	IEC8<2>	IPC32<10:8>
DMA13 – DMA Channel 13	139	131	0x00011A	IFS8<3>	IEC8<3>	IPC32<14:12>
DMA14 – DMA Channel 14	140	132	0x00011C	IFS8<4>	IEC8<4>	IPC33<2:0>
Reserved	141	133	0x00011E	—	—	—
OC13 – Output Compare 13	142	134	0x000120	IFS8<6>	IEC8<6>	IPC33<10:8>
IC13 – Input Capture 13	143	135	0x000122	IFS8<7>	IEC8<7>	IPC33<14:12>
OC14 – Output Compare 14	144	136	0x000124	IFS8<8>	IEC8<8>	IPC34<2:0>
IC14 – Input Capture 14	145	137	0x000126	IFS8<9>	IEC8<9>	IPC34<6:4>
OC15 – Output Compare 15	146	138	0x000128	IFS8<10>	IEC8<10>	IPC34<10:8>
IC15 – Input Capture 15	147	139	0x00012A	IFS8<11>	IEC8<11>	IPC34<14:12>
OC16 – Output Compare 16	148	140	0x00012C	IFS8<12>	IEC8<12>	IPC35<2:0>
IC16 – Input Capture 16	149	141	0x00012E	IFS8<13>	IEC8<13>	IPC35<6:4>
ICD – ICD Application	150	142	0x000130	IFS8<14>	IEC8<14>	IPC35<10:8>
Reserved	151-245	142-237	0x000130-0x0001FE	—	—	—
Lowest Natural Order Priority						

Note 1: This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

Note 2: This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US<1:0>	EDT	DL<2:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3⁽²⁾	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit

1 = Variable exception processing is enabled

0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾

1 = CPU Interrupt Priority Level is greater than 7

0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see **Register 3-2: “CORCON: Core Control Register”**.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receive a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA controller provides these functional capabilities:

- Up to 15 DMA Channels
- Register Indirect With Post-Increment Addressing mode
- Register Indirect Without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two DPSRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from Any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
SPI3 Transfer Done	01011011	0x02A8 (SPI3BUF)	0x02A8 (SPI3BUF)
SPI4 Transfer Done	01111011	0x02C8 (SPI4BUF)	0x02C8 (SPI4BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
UART3RX – UART3 Receiver	01010010	0x0256 (U3RXREG)	—
UART3TX – UART3 Transmitter	01010011	—	0x0254 (U3TXREG)

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL<7:0>							
bit 7							bit 0

Legend:	S = Settable bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Value at POR	'1' = Bit is set	x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾
 1 = Forces a single DMA transfer (Manual mode)
 0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits

00000000 = INT0 – External Interrupt 0
 00000001 = IC1 – Input Capture 1
 00000010 = OC1 – Output Compare 1
 00000101 = IC2 – Input Capture 2
 00000110 = OC2 – Output Compare 2
 00000111 = TMR2 – Timer2
 00001000 = TMR3 – Timer3
 00001010 = SPI1 – Transfer done
 00001011 = UART1RX – UART1 Receiver
 00001100 = UART1TX – UART1 Transmitter
 00001101 = ADC1 – ADC1 convert done
 00010101 = ADC2 – ADC2 convert done
 00011001 = OC3 – Output Compare 3
 00011010 = OC4 – Output Compare 4
 00011011 = TMR4 – Timer4
 00011100 = TMR5 – Timer5
 00011110 = UART2RX – UART2 Receiver
 00011111 = UART2TX – UART2 Transmitter
 00100001 = SPI2 – Transfer done
 00100010 = ECAN1 – RX data ready
 00100101 = IC3 – Input Capture 3
 00100110 = IC4 – Input Capture 4
 00101101 = PMP Data mode
 00110111 = ECAN2 – RX data ready
 00111100 = DCI – DCI transfer done
 01000110 = ECAN1 – TX data request
 01000111 = ECAN2 – TX data request
 01010010 = UART3RX – UART3 Receiver
 01010011 = UART3TX – UART3 Transmitter
 01011000 = UART4RX – UART4 Receiver
 01011001 = UART4TX – UART4 Transmitter
 01011011 = SPI3 – Transfer done
 01111011 = SPI4 – Transfer done

Note 1: The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

10.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the `PWRSV` instruction, or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (`CLKDIV<11>`). The ratio between peripheral and core clock speed is determined by the `DOZE<2:0>` bits (`CLKDIV<14:12>`). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (`CLKDIV<15>`). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

- g) The TRIS registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRIS register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRIS bit must be set to input for pins with only remappable input function(s) assigned.
- h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin is disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRIS register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

11.6 I/O Resources

Many useful resources related to I/O are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554301>

11.6.1 KEY RESOURCES

- **Section 10. “I/O Ports”** (DS70598) in the “*dsPIC33E/PIC24E Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “*dsPIC33E/PIC24E Family Reference Manual*” Sections
- Development Tools

REGISTER 13-2: TyCON: (T3CON, T5CON, T7CON OR T9CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL ⁽²⁾	—	—	—	—	—
bit 15				bit 8			

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE ⁽¹⁾	TCKPS<1:0> ⁽¹⁾		—	—	TCS ^(1,3)	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TON:** Timery On bit⁽¹⁾
 1 = Starts 16-bit Timery
 0 = Stops 16-bit Timery
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timery Stop in Idle Mode bit⁽²⁾
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit⁽¹⁾
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits⁽¹⁾
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timery Clock Source Select bit^(1,3)
 1 = External clock from TyCK pin (on the rising edge)
 0 = Internal clock (FP)
- bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. Refer to the “**Pin Diagrams**” section for the available pins.

15.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. “Output Compare”** (DS70358) of the “dsPIC33E/PIC24E Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

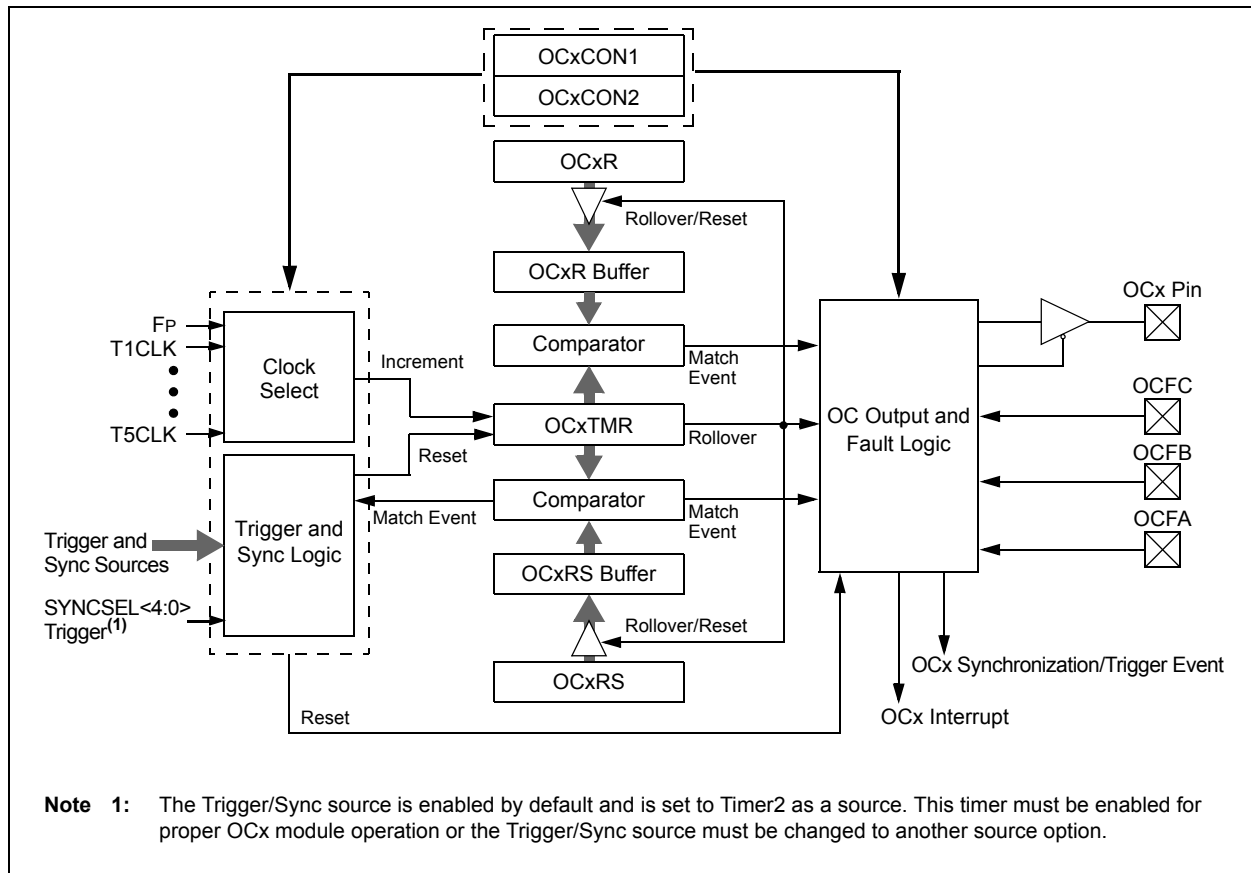
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

Note 1: Only OC1, OC2, OC3 and OC4 can trigger a DMA data transfer.

2: See **Section 13. “Output Compare”** (DS70358) in the “dsPIC33E/PIC24E Family Reference Manual” for OCxR and OCxRS register restrictions.

FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



16.1 PWM Resources

Many useful resources related to the high-speed PWM are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310
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16.1.1 KEY RESOURCES

- **Section 11. “High-Speed PWM”** (DS70645) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bit 15-12)

bit 7-4 **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bit 15-12)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **F11BP<3:0>**: RX Buffer Mask for Filter 11 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>**: RX Buffer Mask for Filter 10 bits (same values as bit 15-12)

bit 7-4 **F9BP<3:0>**: RX Buffer Mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>**: RX Buffer Mask for Filter 8 bits (same values as bit 15-12)

REGISTER 24-4: DCISTAT: DCI STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
r	r	r	r	SLOT<3:0>			
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
r	r	r	r	ROV	RFUL	TUNF	TMPTY
bit 7				bit 0			

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Reserved:** Read as '0'

bit 11-8 **SLOT<3:0>:** DCI Slot Status bits

1111 = Slot 15 is currently active

•
•
•

0010 = Slot 2 is currently active

0001 = Slot 1 is currently active

0000 = Slot 0 is currently active

bit 7-4 **Reserved:** Read as '0'

bit 3 **ROV:** Receive Overflow Status bit

1 = A receive overflow has occurred for at least one Receive register

0 = A receive overflow has not occurred

bit 2 **RFUL:** Receive Buffer Full Status bit

1 = New data is available in the Receive registers

0 = The Receive registers have old data

bit 1 **TUNF:** Transmit Buffer Underflow Status bit

1 = A transmit underflow has occurred for at least one Transmit register

0 = A transmit underflow has not occurred

bit 0 **TMPTY:** Transmit Buffer Empty Status bit

1 = The Transmit registers are empty

0 = The Transmit registers are not empty

TABLE 32-33: SPI1, SPI3 AND SPI4 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 32-33	—	—	0,1	0,1	0,1
9 MHz	—	Table 32-34	—	1	0,1	1
9 MHz	—	Table 32-35	—	0	0,1	1
15 MHz	—	—	Table 32-36	1	0	0
11 MHz	—	—	Table 32-37	1	1	0
15 MHz	—	—	Table 32-38	0	1	0
11 MHz	—	—	Table 32-39	0	0	0

FIGURE 32-15: SPI1, SPI3 AND SPI4 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS

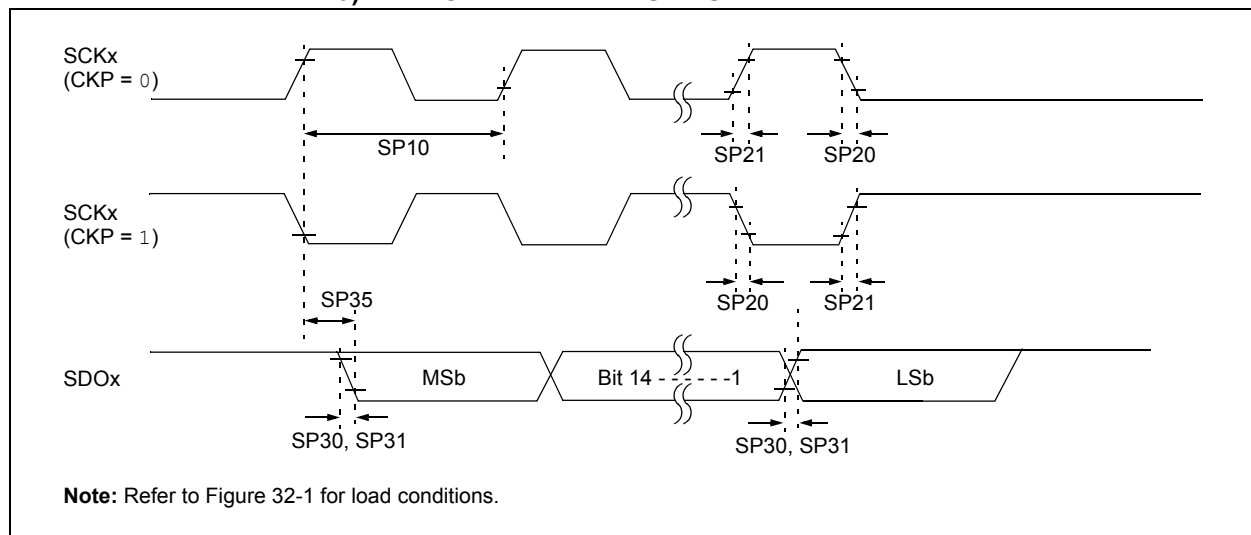
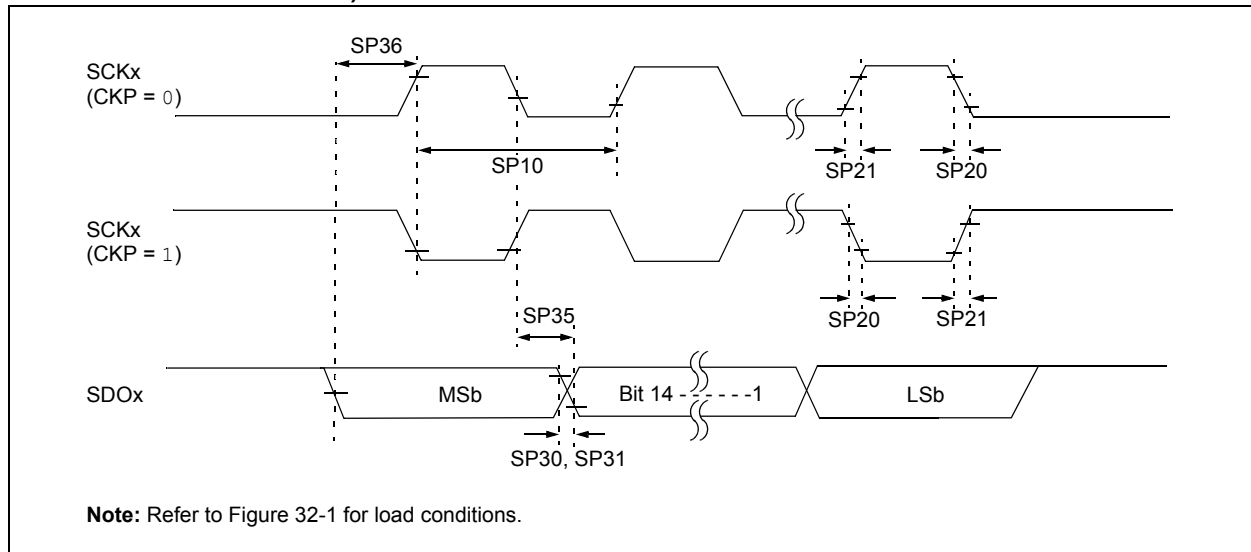


FIGURE 32-16: SPI1, SPI3 AND SPI4 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS**TABLE 32-34: SPI1, SPI3 AND SPI4 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	15	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdiV2sch, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

Note 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

Note 3: The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPIx pins.

Revision F (February 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

Throughout the document, references to the package formerly known as XBGA where changed to TFBGA.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see **Section 18.1 “SPI Helpful Tips”** and **Section 18.2 “SPI Resources”**. The major changes are referenced by their respective section in Table A-4.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
“16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, USB and Advanced Analog”	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an “at-a-glance” format. The following devices were added to the Controller Families table (see Table 1 and the “Pin Diagrams” section): • dsPIC33EP512MC806 • dsPIC33EP512GP806 • PIC24EP512GP806
Section 2.0 “Guidelines for Getting Started with 16-Bit Digital Signal Controllers and Microcontrollers”	Added Section 2.9 “Application Examples”
Section 3.0 “CPU”	Updated the Status Register information in the Programmer’s Model (see Figure 3-2).
Section 4.0 “Memory Organization”	Added Interrupt Controller Register Maps (see Table 4-6 and Table 4-7). Added Peripheral Pin Select Output Register Map (see Table 4-39). Added PMD Register Maps (see Table 4-50 and Table 4-51). Added PORTF Register Map (see Table 4-64). Added PORTG Register Map (see Table 4-67). Updated the second note in Section 4.7 “Bit-Reversed Addressing (dsPIC33EPXXXMU806/810/814 Devices Only)”.
Section 11.0 “I/O Ports”	Added RPOR10: Peripheral Pin Select Output Register 10 (see Register 11-54).
Section 14.0 “Input Capture”	Updated the Input Capture Module Block Diagram (see Figure 14-1).
Section 15.0 “Output Compare”	Updated the Output Compare Module Block Diagram (see Figure 15-1).
Section 25.0 “Comparator Module”	Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-4).
Section 29.0 “Special Features”	Added Note 3 to the Configuration Bits Description (see Table 29-2).
Section 32.0 “Electrical Characteristics”	Updated the I/O pin Absolute Maximum Ratings. Updated Note 1 in the DC Characteristics: Operating Current (see Table 32-5). Updated Note 1 in the DC Characteristics: Idle Current (see Table 32-6). Updated Note 1 in the DC Characteristics: Power-down Current (see Table 32-7). Updated Note 1 in the DC Characteristics: Doze Current (see Table 32-8). Removed parameters DO16 and DO26, added parameter DO26a, updated parameters DO10 and DO20, and added Note 1 in the DC Characteristics: I/O Pin Output Specifications (see Table 32-10).

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