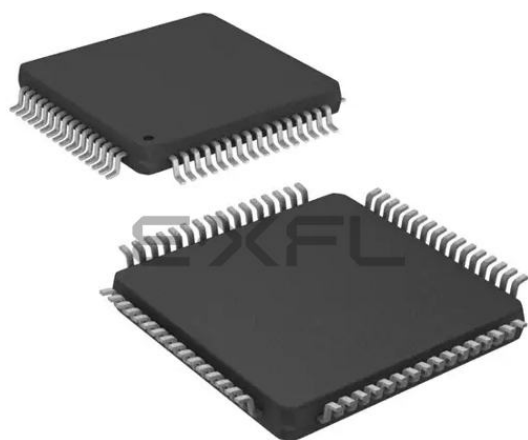




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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp806-e-pt

Pin Diagrams (Continued)

121-Pin TFBGA⁽¹⁾

● = Pins are up to 5V tolerant

dsPIC33EP256MU810
dsPIC33EP512MU810

	1	2	3	4	5	6	7	8	9	10	11
A	○ RE4	○ RE3	● RG13	○ RE0	● RG0	● RF1	○ VDD	● NC	● RD12	● RD2	● RD1
B	● NC	● RG15	○ RE2	○ RE1	○ RA7	● RF0	○ VCAP	● RD5	● RD3	○ VSS	○ RC14
C	○ RE6	○ VDD	● RG12	● RG14	○ RA6	● NC	○ RD7	● RD4	● NC	○ RC13	● RD11
D	○ RC1	○ RE7	○ RE5	● NC	● NC	● NC	○ RD6	● RD13	● RD0	● NC	● RD10
E	○ RC4	○ RC3	○ RG6	○ RC2	● NC	● RG1	● NC	● RA15	● RD8	● RD9	● RA14
F	● MCLR	○ RG8	○ RG9	○ RG7	○ VSS	● NC	● NC	○ VDD	○ RC12	○ VSS	○ RC15
G	○ RE8	○ RE9	● RA0	● NC	○ VDD	○ VSS	○ VSS	● NC	● RA5	● RA3	● RA4
H	○ RB5	○ RB4	● NC	● NC	● NC	○ VDD	● NC	● VBUS	○ VUSB3V3	○ RG2	● RA2
J	○ RB3	○ RB2	○ RB7	○ AVDD	○ RB11	● RA1	○ RB12	● NC	● NC	● RF8	○ RG3
K	○ RB1	○ RB0	○ RA10	○ RB8	● NC	● RF12	○ RB14	○ VDD	● RD15	● RF3	● RF2
L	○ RB6	○ RA9	○ AVSS	○ RB9	○ RB10	● RF13	○ RB13	○ RB15	● RD14	● RF4	● RF5

Note 1: Refer to Table 2 for full pin names.

TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES^(1,2)

Pin Number	Full Pin Name	Pin Number	Full Pin Name
A1	AN28/PMD4/RP84/RE4	E8	RPI31/RA15
A2	AN27/PMD3/RPI83/RE3	E9	RTCC/DMLN/RPI72/RD8
A3	RP125/RG13	E10	ASDA1 ⁽³⁾ /DPLN/RPI73/RD9
A4	AN24/PMD0/RP80/RE0	E11	RPI30/RA14
A5	RP112/RG0	F1	MCLR
A6	VCMPST2/RP97/RF1	F2	C2IN3-/SDO2/PMA3/RP120/RG8
A7	VDD	F3	C2IN1-/PMA2/RPI121/RG9
A8	No Connect	F4	C1IN1-/SDI2/PMA4/RPI119/RG7
A9	RPI76/RD12	F5	Vss
A10	DPH/RP66/RD2	F6	No Connect
A11	VCPCON/RP65/RD1	F7	No Connect
B1	No Connect	F8	VDD
B2	RP127/RG15	F9	OSC1/RPI60/RC12
B3	AN26/PMD2/RP82/RE2	F10	Vss
B4	AN25/PMD1/RPI81/RE1	F11	OSC2/CLKO/RC15
B5	AN23/RPI23/RA7	G1	AN20/RPI88/RE8
B6	VCMPST1/RP96/RF0	G2	AN21/RPI89/RE9
B7	VCAP	G3	TMS/RPI16/RA0
B8	PMRD/RP69/RD5	G4	No Connect
B9	PMBE/RP67/RD3	G5	VDD
B10	Vss	G6	Vss
B11	PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14	G7	Vss
C1	AN30/PMD6/RPI86/RE6	G8	No Connect
C2	VDD	G9	TDO/RPI21/RA5
C3	RPI124/RG12	G10	ASDA2 ⁽³⁾ /RPI19/RA3
C4	RP126/RG14	G11	TDI/RPI20/RA4
C5	AN22/RPI22/RA6	H1	AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5
C6	No Connect	H2	AN4/C1IN2-/USBOEN/RPI36/RB4
C7	C3IN1+/VCMPST3/RP71/RD7	H3	No Connect
C8	PMWR/RP68/RD4	H4	No Connect
C9	No Connect	H5	No Connect
C10	PGED2/SOSCI/C3IN3-/RPI61/RC13	H6	VDD
C11	PMCS1/RPI75/RD11	H7	No Connect
D1	AN16/RPI49/RC1	H8	VBUS
D2	AN31/PMD7/RP87/RE7	H9	VUSB3V3
D3	AN29/PMD5/RP85/RE5	H10	D+/RG2 ⁽⁴⁾
D4	No Connect	H11	ASCL2 ⁽³⁾ /RPI18/RA2
D5	No Connect	J1	AN3/C2IN1+/VP10/RPI35/RB3
D6	No Connect	J2	AN2/C2IN2-/VMIO/RPI34/RB2
D7	C3IN2-/RP70/RD6	J3	PGED1/AN7/RCV/RPI39/RB7
D8	RPI77/RD13	J4	AVDD
D9	INT0/DMH/RP64/RD0	J5	AN11/PMA12/RPI43/RB11
D10	No Connect	J6	TCK/RPI17/RA1
D11	ASCL1 ⁽³⁾ /PMCS2/RPI74/RD10	J7	AN12/PMA11/RPI44/RB12

- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select”** for available peripherals and for information on limitations.
- 2:** Every I/O port pin (RAX-RGx) can be used as change notification (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- 3:** The availability of I²C™ interfaces varies by device. Selection (SDAX/SCLx or ASDAX/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.
- 4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.
- 5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC806 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	C2TXIP<2:0>			—	C1TXIP<2:0>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			4444
IPC18	0864	—	QEI2IP<2:0>			—	—	—	—	—	PSESMIP<2:0>			—	—	—	—	4040
IPC20	0868	—	U3TXIP<2:0>			—	U3RXIP<2:0>			—	U3EIP<2:0>			—	—	—	—	4440
IPC21	086A	—	U4EIP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	4400
IPC22	086C	—	SPI3IP<2:0>			—	SPI3EIP<2:0>			—	U4TXIP<2:0>			—	U4RXIP<2:0>			4444
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	IC9IP<2:0>			—	OC9IP<2:0>			4444
IPC24	0870	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	PWM3IP<2:0>			0044
IPC29	087A	—	DMA9IP<2:0>			—	DMA8IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC30	087C	—	SPI4IP<2:0>			—	SPI4EIP<2:0>			—	DMA11IP<2:0>			—	DMA10IP<2:0>			4444
IPC31	087E	—	IC11IP<2:0>			—	OC11IP<2:0>			—	IC10IP<2:0>			—	OC10IP<2:0>			4444
IPC32	0880	—	DMA13IP<2:0>			—	DMA12IP<2:0>			—	IC12IP<2:0>			—	OC12IP<2:0>			4444
IPC33	0882	—	IC13IP<2:0>			—	OC13IP<2:0>			—	—	—	—	—	DMA14IP<2:0>			4404
IPC34	0884	—	IC15IP<2:0>			—	OC15IP<2:0>			—	IC14IP<2:0>			—	OC14IP<2:0>			4444
IPC35	0886	—	—	—	—	—	ICDIP<2:0>			—	IC16IP<2:0>			—	OC16IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	UAE	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	—	ILR<3:0>			VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC20	0868	—	U3TXIP<2:0>			—	U3RXIP<2:0>			—	U3EIP<2:0>			—	—	—	—	4440
IPC21	086A	—	U4EIP<2:0>			—	USB1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC22	086C	—	SPI3IP<2:0>			—	SPI3EIP<2:0>			—	U4TXIP<2:0>			—	U4RXIP<2:0>			4444
IPC23	086E	—	—	—	—	—	—	—	—	—	IC9IP<2:0>			—	OC9IP<2:0>			0044
IPC29	087A	—	DMA9IP<2:0>			—	DMA8IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC30	087C	—	SPI4IP<2:0>			—	SPI4EIP<2:0>			—	DMA11IP<2:0>			—	DMA10IP<2:0>			4444
IPC31	087E	—	IC11IP<2:0>			—	OC11IP<2:0>			—	IC10IP<2:0>			—	OC10IP<2:0>			4444
IPC32	0880	—	DMA13IP<2:0>			—	DMA12IP<2:0>			—	IC12IP<2:0>			—	OC12IP<2:0>			4444
IPC33	0882	—	IC13IP<2:0>			—	OC13IP<2:0>			—	—	—	—	—	DMA14IP<2:0>			4404
IPC34	0884	—	IC15IP<2:0>			—	OC15IP<2:0>			—	IC14IP<2:0>			—	OC14IP<2:0>			4444
IPC35	0886	—	—	—	—	—	ICDIP<2:0>			—	IC16IP<2:0>			—	OC16IP<2:0>			4444
INTCON1	08C0	NSTDIS	—	—	—	—	—	—	—	—	DIV0ERR	DMA0ERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	UAE	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	—	ILR<3:0>			VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Timer Value 1 Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Timer Value 2 Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Timer Value 3 Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Timer Value 4 Register																xxxx
OC5CON1	0928	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC5CON2	092A	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC5RS	092C	Output Compare 5 Secondary Register																xxxx
OC5R	092D	Output Compare 5 Register																xxxx
OC5TMR	0930	Timer Value 5 Register																xxxx
OC6CON1	0932	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC6CON2	0934	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC6RS	0936	Output Compare 6 Secondary Register																xxxx
OC6R	0938	Output Compare 6 Register																xxxx
OC6TMR	093A	Timer Value 6 Register																xxxx
OC7CON1	093C	—	—	OCSIDL	OCTSEL<2:0>			ENFLTC	ENFLTB	ENFLTA	OCFLTC	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC7CON2	093E	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC7RS	0940	Output Compare 7 Secondary Register																xxxx
OC7R	0942	Output Compare 7 Register																xxxx
OC7TMR	0944	Timer Value 7 Register																xxxx

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: QE1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QE1CON	01C0	QE1EN	—	QE1SIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
QE1IOC	01C2	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QE1STAT	01C4	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6	POSCNT<15:0>																0000
POS1CNTH	01C8	POSCNT<31:16>																0000
POS1HLD	01CA	POSHLD<15:0>																0000
VEL1CNT	01CC	VELCNT<15:0>																0000
INT1TMRL	01CE	INTTMR<15:0>																0000
INT1TMRH	01D0	INTTMR<31:16>																0000
INT1HLDL	01D2	INTHLD<15:0>																0000
INT1HLDH	01D4	INTHLD<31:16>																0000
INDX1CNTL	01D6	INDXCNT<15:0>																0000
INDX1CNTH	01D8	INDXCNT<31:16>																0000
INDX1HLD	01DA	INDXHLD<15:0>																0000
QE1GECL	01DC	QEIGEC<15:0>																0000
QE1ICL	01DC	QEIIC<15:0>																0000
QE1GECH	01DE	QEIGEC<31:16>																0000
QE1ICH	01DE	QEIIC<31:16>																0000
QE1LECL	01E0	QEILEC<15:0>																0000
QE1LECH	01E2	QEILEC<31:16>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: I2C1 and I2C2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2Cx Receive Register									0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2Cx Transmit Register									00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator										0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000	
I2C1ADD	020A	—	—	—	—	—	—	I2Cx Address Register											0000
I2C1MSK	020C	—	—	—	—	—	—	I2Cx Address Mask											0000
I2C2RCV	0210	—	—	—	—	—	—	—	—	I2Cx Receive Register									0000
I2C2TRN	0212	—	—	—	—	—	—	—	—	I2Cx Transmit Register									00FF
I2C2BRG	0214	—	—	—	—	—	—	—	Baud Rate Generator										0000
I2C2CON	0216	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C2STAT	0218	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000	
I2C2ADD	021A	—	—	—	—	—	—	I2Cx Address Register											0000
I2C2MSK	021C	—	—	—	—	—	—	I2Cx Address Mask											0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: SPI1, SPI2, SPI3 and SPI4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SP1x Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SP1x Transmit and Receive Buffer Register																0000
SPI3STAT	02A0	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI3CON1	02A2	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI3CON2	02A4	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI3BUF	02A8	SP1x Transmit and Receive Buffer Register																0000
SPI4STAT	02C0	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI4CON1	02C2	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI4CON2	02C4	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI4BUF	02C8	SP1x Transmit and Receive Buffer Register																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: ADC1 and ADC2 REGISTER MAP (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC2BUF9	0352	ADCx Data Buffer 9																	xxxx
ADC2BUFA	0354	ADCx Data Buffer 10																	xxxx
ADC2BUFB	0356	ADCx Data Buffer 11																	xxxx
ADC2BUFC	0358	ADCx Data Buffer 12																	xxxx
ADC2BUFD	035A	ADCx Data Buffer 13																	xxxx
ADC2BUFE	035C	ADCx Data Buffer 14																	xxxx
ADC2BUFF	035E	ADCx Data Buffer 15																	xxxx
AD2CON1	0360	ADON	—	ADSIDL	ADDMABM	—	—	FORM<1:0>		SSRC<2:0>			SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD2CON2	0362	VCFG<2:0>			—	—	CSCNA	CHPS<1:0>		BUFS	—	SMPI<3:0>				BUFM	ALTS	0000	
AD2CON3	0364	ADRC	—	—	SAMC<4:0>				ADCS<7:0>										0000
AD2CHS123	0366	—	—	—	—	—	CH123NB<1:0>		CH123SB	—	—	—	—	—	CH123NA<1:0>		CH123SA	0000	
AD2CHS0	0368	CH0NB	—	—	CH0SB<4:0>				CH0NA	—	—	CH0SA<4:0>						0000	
AD2CSSL	0270	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000	
AD2CON4	0272	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL<2:0>			0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These bits are not available on dsPIC33EP256MU806 devices.

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0> ⁽²⁾		
bit 15				bit 8			

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	R/W-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7				bit 0			

Legend:	y = Value Set from Configuration bits on POR	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)

- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits⁽²⁾

- 111 = Fast RC Oscillator (FRC) with Divide-by-N
- 110 = Fast RC Oscillator (FRC) with Divide-by-16
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (XT, HS, EC) with PLL
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
- 000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit

- 1 = If (FCKSM0 = 1), then clock and PLL configurations are locked
If (FCKSM0 = 0), then clock and PLL configurations may be modified
- 0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit

- 1 = I/O lock is active
- 0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)

- 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
- 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"* (available from the Microchip web site) for details.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

3: This register resets only on a Power-on Reset (POR).

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T5MD	T4MD	T3MD	T2MD	T1MD	QE11MD ⁽¹⁾	PWMMD ⁽¹⁾	DCIMD
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **T5MD:** Timer5 Module Disable bit
 1 = Timer5 module is disabled
 0 = Timer5 module is enabled
- bit 14 **T4MD:** Timer4 Module Disable bit
 1 = Timer4 module is disabled
 0 = Timer4 module is enabled
- bit 13 **T3MD:** Timer3 Module Disable bit
 1 = Timer3 module is disabled
 0 = Timer3 module is enabled
- bit 12 **T2MD:** Timer2 Module Disable bit
 1 = Timer2 module is disabled
 0 = Timer2 module is enabled
- bit 11 **T1MD:** Timer1 Module Disable bit
 1 = Timer1 module is disabled
 0 = Timer1 module is enabled
- bit 10 **QE11MD:** QE11 Module Disable bit⁽¹⁾
 1 = QE11 module is disabled
 0 = QE11 module is enabled
- bit 9 **PWMMD:** PWM Module Disable bit⁽¹⁾
 1 = PWM module is disabled
 0 = PWM module is enabled
- bit 8 **DCIMD:** DCI Module Disable bit
 1 = DCI module is disabled
 0 = DCI module is enabled
- bit 7 **I2C1MD:** I2C1 Module Disable bit
 1 = I2C1 module is disabled
 0 = I2C1 module is enabled
- bit 6 **U2MD:** UART2 Module Disable bit
 1 = UART2 module is disabled
 0 = UART2 module is enabled
- bit 5 **U1MD:** UART1 Module Disable bit
 1 = UART1 module is disabled
 0 = UART1 module is enabled
- bit 4 **SPI2MD:** SPI2 Module Disable bit
 1 = SPI2 module is disabled
 0 = SPI2 module is enabled

Note 1: This bit is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

bit 1 **I2C2MD:** I2C2 Module Disable bit
 1 = I2C2 module is disabled
 0 = I2C2 module is enabled

bit 0 **AD2MD:** ADC2 Module Disable bit
 1 = ADC2 module is disabled
 0 = ADC2 module is enabled

Note 1: This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

11.4 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation “RPn” or “RPI n” in their full pin designation, where “RP” designates a remappable function for input or output and “RPI” designates a remappable functions for input only, and “n” is the remappable pin number.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

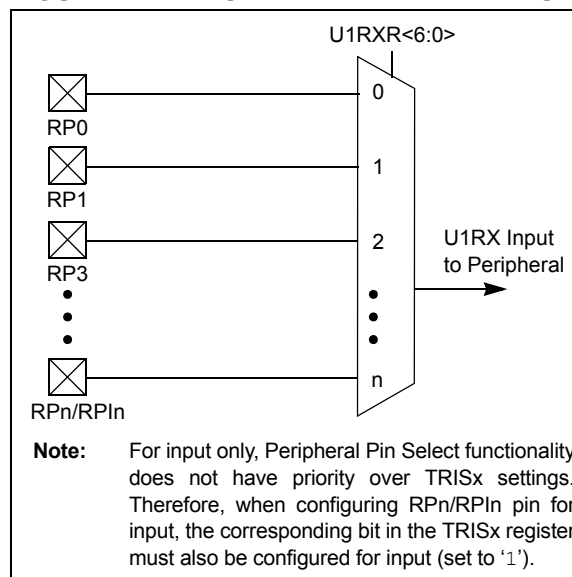
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPI nRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-22). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals (see Table 11-1). Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn/RPI n pin with the corresponding value to that peripheral (see Table 11-2). For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: U1RX REMAPPABLE INPUT



REGISTER 11-34: RPINR34: PERIPHERAL PIN SELECT INPUT REGISTER 34

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC12R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC11R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC12R<6:0>:** Assign Input Capture 12 (IC12) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC11R<6:0>:** Assign Input Capture 11 (IC11) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 22-17: UxIE: USB INTERRUPT ENABLE REGISTER (HOST MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STALLIE	ATTACHIE ⁽¹⁾	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	DETACHIE
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 6 **ATTACHIE:** Peripheral Attach Interrupt bit⁽¹⁾
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 5 **RESUMEIE:** Resume Interrupt bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 4 **IDLEIE:** Idle Detect Interrupt bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 3 **TRNIE:** Token Processing Complete Interrupt bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 2 **SOFIE:** Start-of-Frame Token Interrupt bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 1 **UERRIE:** USB Error Condition Interrupt bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 0 **DETACHIE:** USB Detach Interrupt Enable bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled

Note 1: Unimplemented in OTG mode, read as '0'.

REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate
- bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate
- bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate
- bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate
- bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate
- bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate
- bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate
- bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate
- bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate
- bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

**REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING
CONTROL REGISTER (CONTINUED)**

bit 3	ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate
bit 2	ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate
bit 1	AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate
bit 0	AAENEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

FIGURE 32-25: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

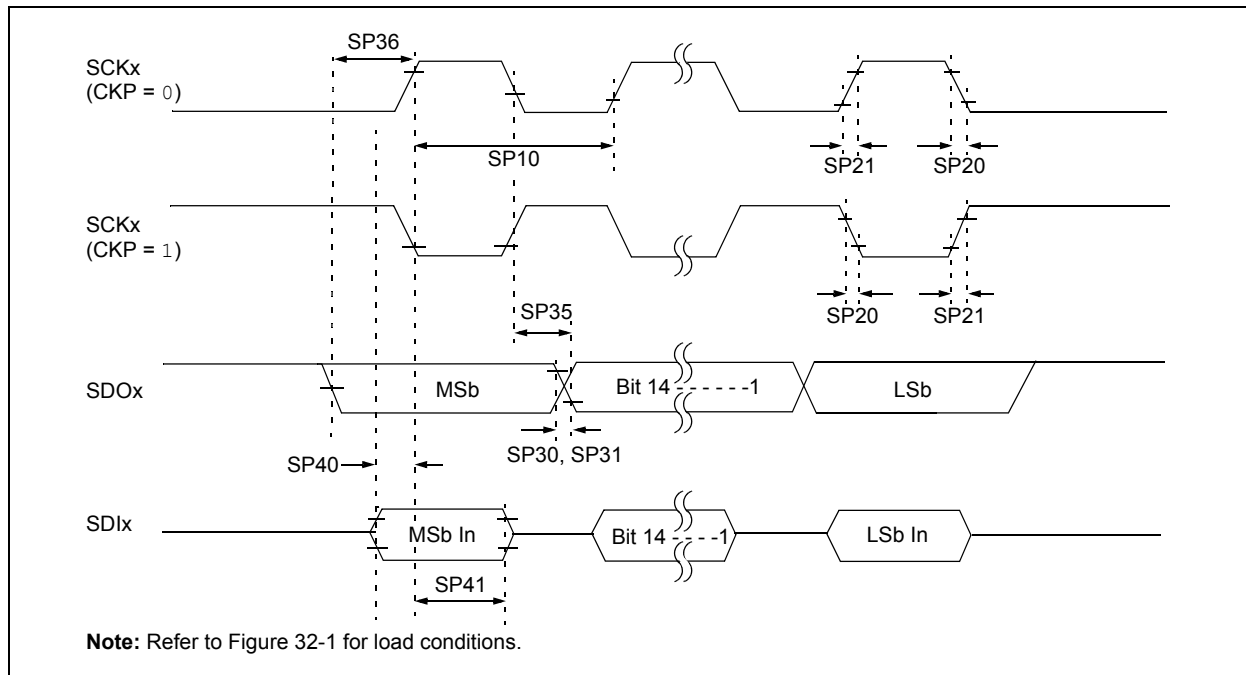


TABLE 32-43: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	10	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

Note 2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

Note 3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPIx pins.

TABLE 32-56: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 1) (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (10-Bit Mode) – Measurements with External VREF+/VREF-							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1	—	+1	LSb	$V_{INL} = AV_{SS} = V_{REFL} = 0V$, $AV_{DD} = V_{REFH} = 3.6V$
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	$V_{INL} = AV_{SS} = V_{REFL} = 0V$, $AV_{DD} = V_{REFH} = 3.6V$
AD23b	GERR	Gain Error	1	3	6	LSb	$V_{INL} = AV_{SS} = V_{REFL} = 0V$, $AV_{DD} = V_{REFH} = 3.6V$
AD24b	EOFF	Offset Error	1	2	3	LSb	$V_{INL} = AV_{SS} = V_{REFL} = 0V$, $AV_{DD} = V_{REFH} = 3.6V$
AD25b	—	Monotonicity	—	—	—	—	Guaranteed ⁽²⁾
ADC Accuracy (10-Bit Mode) – Measurements with Internal VREF+/VREF-							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	$V_{INL} = AV_{SS} = 0V$, $AV_{DD} = 3.6V$
AD22b	DNL	Differential Nonlinearity	>-1	—	<1	LSb	$V_{INL} = AV_{SS} = 0V$, $AV_{DD} = 3.6V$
AD23b	GERR	Gain Error	1	5	6	LSb	$V_{INL} = AV_{SS} = 0V$, $AV_{DD} = 3.6V$
AD24b	EOFF	Offset Error	1	2	5	LSb	$V_{INL} = AV_{SS} = 0V$, $AV_{DD} = 3.6V$
AD25b	—	Monotonicity	—	—	—	—	Guaranteed ⁽²⁾
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB	
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	—	dB	
AD32b	SFDR	Spurious Free Dynamic Range	72	—	—	dB	
AD33b	FNYQ	Input Signal Bandwidth	—	—	550	kHz	
AD34b	ENOB	Effective Number of Bits	9.16	9.4	—	bits	

Note 1: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

2: The Analog-to-Digital conversion result never decreases with an increase in input voltage and has no missing codes.

NOTES: