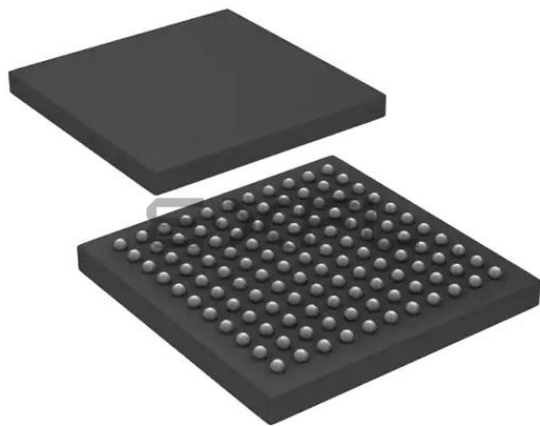




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What is "[Embedded - Microcontrollers](#)"?

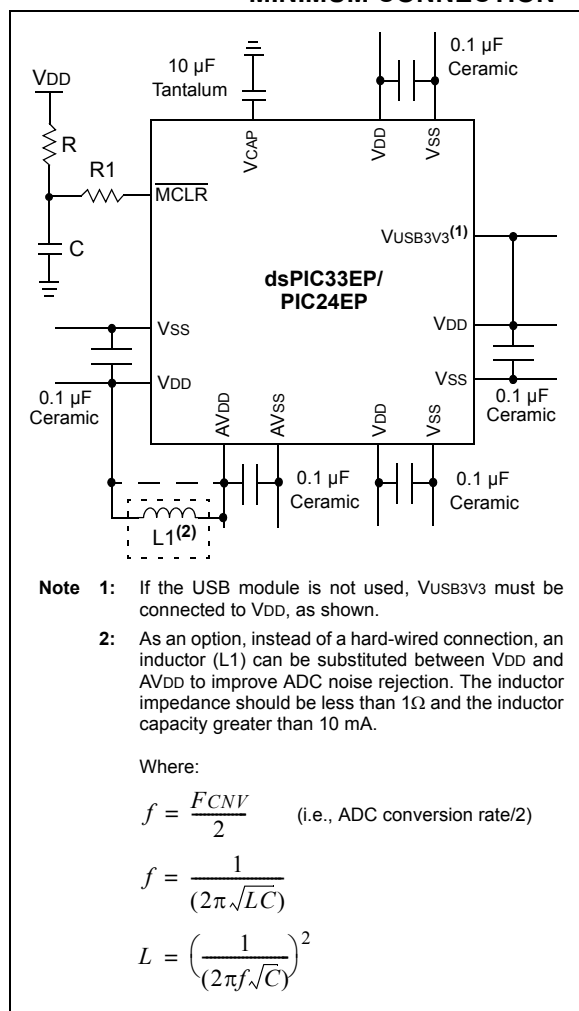
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu810-e-bg

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected

to ground. The type can be ceramic or tantalum. See **Section 32.0 “Electrical Characteristics”** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 29.2 “On-Chip Voltage Regulator”** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

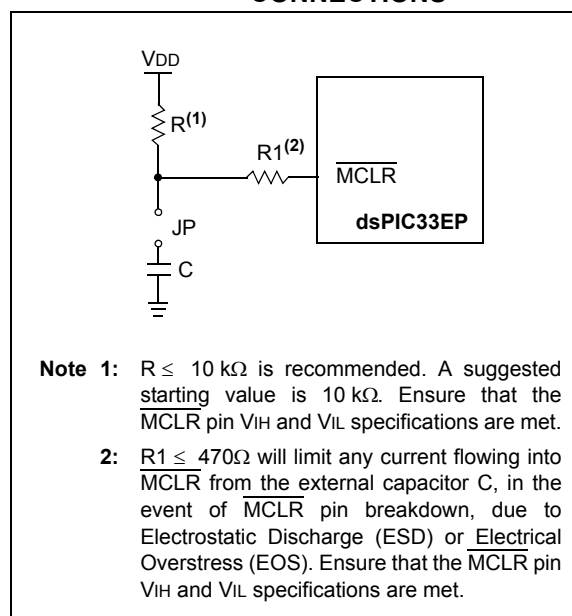
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



3.6 CPU Resources

Many useful resources related to the CPU are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310
--

3.6.1 KEY RESOURCES

- See **Section 16. “CPU”** (DS70359) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

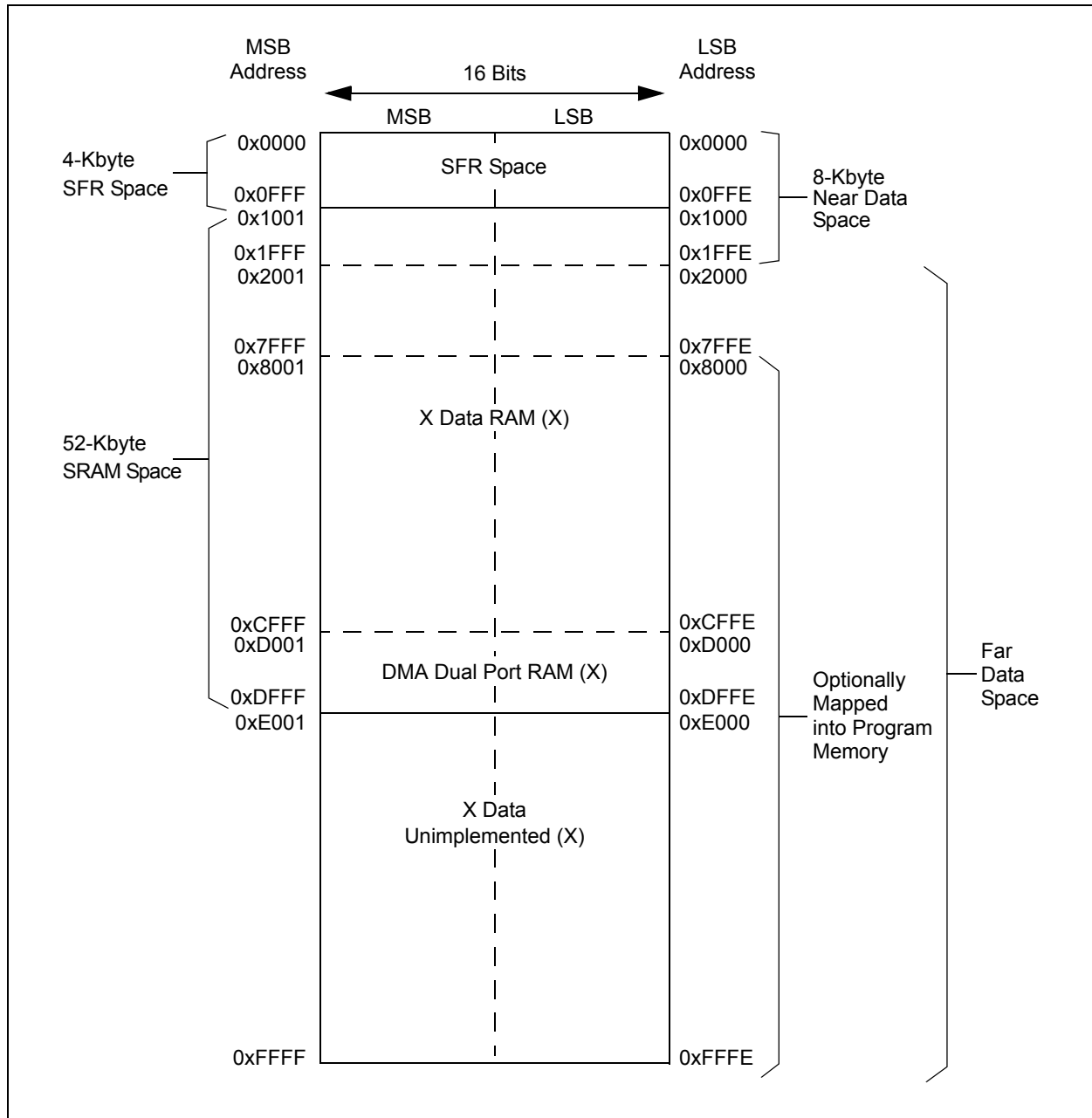
FIGURE 4-4: DATA MEMORY MAP FOR PIC24EP512(GP/GU)806/810/814 DEVICES WITH 52-KBYTE RAM

TABLE 4-64: PORTF REGISTER MAP FOR dsPIC33EPXXX(GP/MC)806 AND PIC24EPXXXGP806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	TRISG6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	003B
PORTF	0E52	—	—	—	—	—	—	—	—	—	RG6	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	LATG6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	ODCF6	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	CNIEG6	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	CNPUG6	CNPUF5	CNPUF4	CNPUF3	CNPUF2	CNPUF1	CNPUF0	0000
CNPDPF	0E5C	—	—	—	—	—	—	—	—	—	CNPDG6	CNPDPF5	CNPDPF4	CNPDPF3	CNPDPF2	CNPDPF1	CNPDPF0	0000
ANSELF	0E5E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-65: PORTF REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	TRISF5	TRISF4	TRISF3	—	TRISF1	TRISF0	003B
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	RF5	RF4	RF3	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	LATF5	LATF4	LATF3	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	ODCF5	ODCF4	ODCF3	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	CNIEF5	CNIEF4	CNIEF3	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	CNPUF5	CNPUF4	CNPUF3	—	CNPUF1	CNPUF0	0000
CNPDPF	0E5C	—	—	—	—	—	—	—	—	—	—	CNPDPF5	CNPDPF4	CNPDPF3	—	CNPDPF1	CNPDPF0	0000
ANSELF	0E5E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-66: PORTG REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	TRISG1	TRISG0	F3C3
PORTG	0E62	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	RG3 ⁽¹⁾	RG2 ⁽¹⁾	RG1	RG0	xxxx
LATG	0E64	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	LATG1	LATG0	xxxx
ODCG	0E66	ODCG15	ODCG14	ODCG13	ODCG12	—	—	—	—	—	—	—	—	—	—	ODCG1	ODCG0	0000
CNENG	0E68	CNIEG15	CNIEG14	CNIEG13	CNIEG12	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	CNIEG3 ⁽¹⁾	CNIEG2 ⁽¹⁾	CNIEG1	CNIEG0	0000
CNPUG	0E6A	CNPUG15	CNPUG14	CNPUG13	CNPUG12	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	CNPUG1	CNPUG0	0000
CNPDPG	0E6C	CNPDPG15	CNPDPG14	CNPDPG13	CNPDPG12	—	—	CNPDPG9	CNPDPG8	CNPDPG7	CNPDPG6	—	—	—	—	CNPDPG1	CNPDPG0	0000
ANSELG	0E6E	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: If RG2 and RG3 are used as general purpose inputs, the VUSB3V3 pin must be connected to VDD.

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PPST14	PPST13	PPST12	PPST11	PPST10	PPST9	PPST8
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14 **PPST14:** Channel 14 Ping-Pong Mode Status Flag bit
 1 = DMASTB14 register selected
 0 = DMASTA14 register selected
- bit 13 **PPST13:** Channel 13 Ping-Pong Mode Status Flag bit
 1 = DMASTB13 register selected
 0 = DMASTA13 register selected
- bit 12 **PPST12:** Channel 12 Ping-Pong Mode Status Flag bit
 1 = DMASTB12 register selected
 0 = DMASTA12 register selected
- bit 11 **PPST11:** Channel 11 Ping-Pong Mode Status Flag bit
 1 = DMASTB11 register selected
 0 = DMASTA11 register selected
- bit 10 **PPST10:** Channel 10 Ping-Pong Mode Status Flag bit
 1 = DMASTB10 register selected
 0 = DMASTA10 register selected
- bit 9 **PPST9:** Channel 9 Ping-Pong Mode Status Flag bit
 1 = DMASTB9 register selected
 0 = DMASTA9 register selected
- bit 8 **PPST8:** Channel 8 Ping-Pong Mode Status Flag bit
 1 = DMASTB8 register selected
 0 = DMASTA8 register selected
- bit 7 **PPST7:** Channel 7 Ping-Pong Mode Status Flag bit
 1 = DMASTB7 register selected
 0 = DMASTA7 register selected
- bit 6 **PPST6:** Channel 6 Ping-Pong Mode Status Flag bit
 1 = DMASTB6 register selected
 0 = DMASTA6 register selected
- bit 5 **PPST5:** Channel 5 Ping-Pong Mode Status Flag bit
 1 = DMASTB5 register selected
 0 = DMASTA5 register selected
- bit 4 **PPST4:** Channel 4 Ping-Pong Mode Status Flag bit
 1 = DMASTB4 register selected
 0 = DMASTA4 register selected
- bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
 1 = DMASTB3 register selected
 0 = DMASTA3 register selected

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CONTINUED)

bit 3	OC4MD: Output Compare 4 Module Disable bit 1 = Output Compare 4 module is disabled 0 = Output Compare 4 module is enabled
bit 2	OC3MD: Output Compare 3 Module Disable bit 1 = Output Compare 3 module is disabled 0 = Output Compare 3 module is enabled
bit 1	OC2MD: Output Compare 2 Module Disable bit 1 = Output Compare 2 module is disabled 0 = Output Compare 2 module is enabled
bit 0	OC1MD: Output Compare 1 Module Disable bit 1 = Output Compare 1 module is disabled 0 = Output Compare 1 module is enabled

bit 1 **I2C2MD:** I2C2 Module Disable bit
 1 = I2C2 module is disabled
 0 = I2C2 module is enabled

bit 0 **AD2MD:** ADC2 Module Disable bit
 1 = ADC2 module is disabled
 0 = ADC2 module is enabled

Note 1: This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1101	I	RPI45
000 0001	I	C1OUT ⁽¹⁾	010 1110	I	RPI46
000 0010	I	C2OUT ⁽¹⁾	010 1111	I	RPI47
000 0011	I	C3OUT ⁽¹⁾	011 0000	—	Reserved
000 0100	—	Reserved	011 0001	I	RPI49
000 0101	—	Reserved	011 0010	I	RPI50
000 0110	—	Reserved	011 0011	I	RPI51
000 0111	—	Reserved	011 0100	I	RPI52
000 1000	I	FINDX1 ⁽¹⁾	011 0101	—	Reserved
000 1001	I	FHOME1 ⁽¹⁾	011 0110	—	Reserved
000 1010	I	FINDX2 ⁽¹⁾	011 0111	—	Reserved
000 1011	I	FHOME2 ⁽¹⁾	011 1000	—	Reserved
000 1100	—	Reserved	011 1001	—	Reserved
000 1101	—	Reserved	011 1010	—	Reserved
000 1110	—	Reserved	011 1011	—	Reserved
000 1111	—	Reserved	011 1100	I	RPI60
001 0000	I	RPI16	011 1101	I	RPI61
001 0001	I	RPI17	011 1110	I	RPI62
001 0010	I	RPI18	011 1111	—	Reserved
001 0011	I	RPI19	100 0000	I/O	RP64
001 0100	I	RPI20	100 0001	I/O	RP65
001 0101	I	RPI21	100 0010	I/O	RP66
001 0110	I	RPI22	100 0011	I/O	RP67
001 0111	I	RPI23	100 0100	I/O	RP68
001 1000	—	Reserved	100 0101	I/O	RP69
001 1001	—	Reserved	100 0110	I/O	RP70
001 1010	—	Reserved	100 0111	I/O	RP71
001 1011	—	Reserved	100 1000	I	RPI72
001 1100	—	Reserved	100 1001	I	RPI73
001 1101	—	Reserved	100 1010	I	RPI74
001 1110	I	RPI30	100 1011	I	RPI75
001 1111	I	RPI31	100 1100	I	RPI76
010 0000	I	RPI32	100 1101	I	RPI77
010 0001	I	RPI33	100 1110	I	RPI78
010 0010	I	RPI34	100 1111	I/O	RP79
010 0011	I	RPI35	101 0000	I/O	RP80
010 0100	I	RPI36	101 0001	I	RPI81
010 0101	I	RPI37	101 0010	I/O	RP82
010 0110	I	RPI38	101 0011	I	RPI83
010 0111	I	RPI39	101 0100	I/O	RP84
010 1000	I	RPI40	101 0101	I/O	RP85
010 1001	I	RPI41	101 0110	I	RPI86
010 1010	I	RPI42	101 0111	I/O	RP87

Note 1: See Section 11.4.4.2 “Virtual Connections” for more information on selecting this pin assignment.

**REGISTER 11-15: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14
(dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEB1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEA1R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB1R<6:0>:** Assign B (QEB) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R<6:0>:** Assign A (QEA) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-20: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U2CTSR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U2RXR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14-8 **U2CTSR<6:0>:** Assign UART2 Clear-to-Send (U2CTS) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

12.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. “Timers”** (DS70362) of the “dsPIC33E/PIC24E Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the real-time clock, or operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated from the low-power 32 kHz crystal oscillator available on the device.
- Can be operated in Asynchronous Counter mode from an external clock source.
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and clock synchronization is performed after the prescaler.

The unique features of Timer1 allow it to be used for Real-Time Clock (RTC) applications. A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (Fcy). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

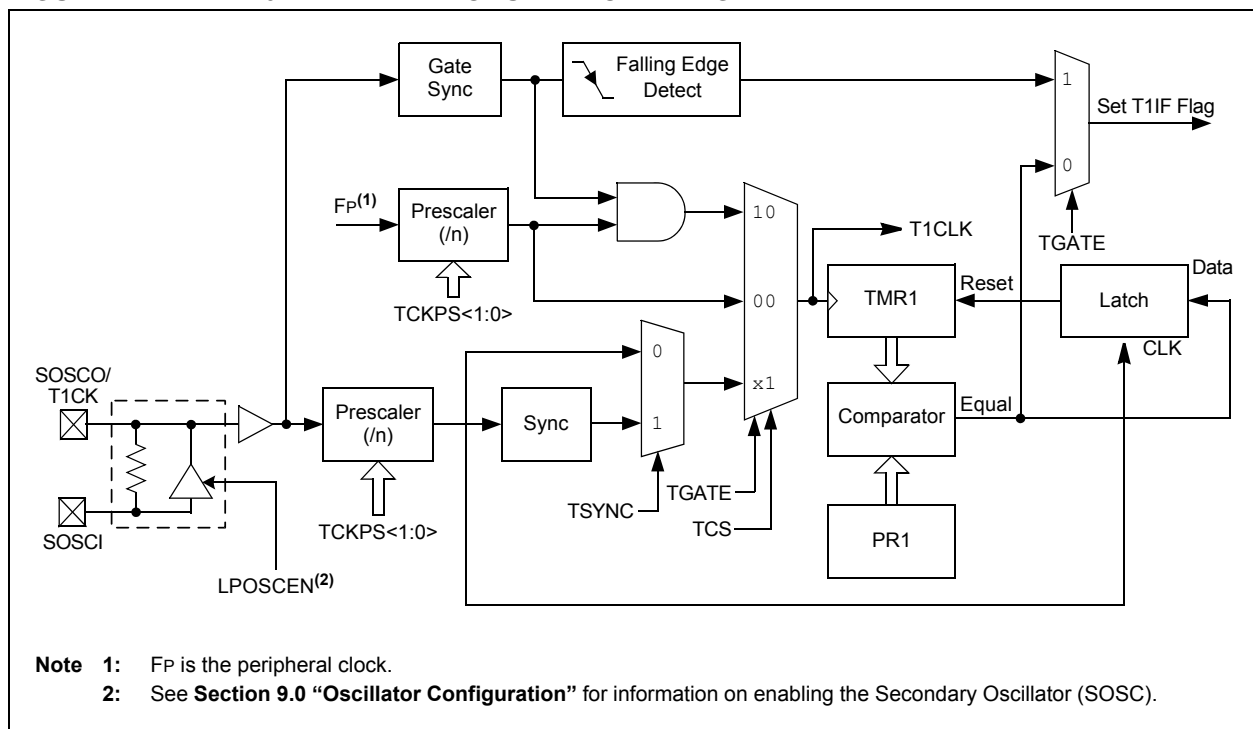
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



14.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "Input Capture"** (DS70352) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

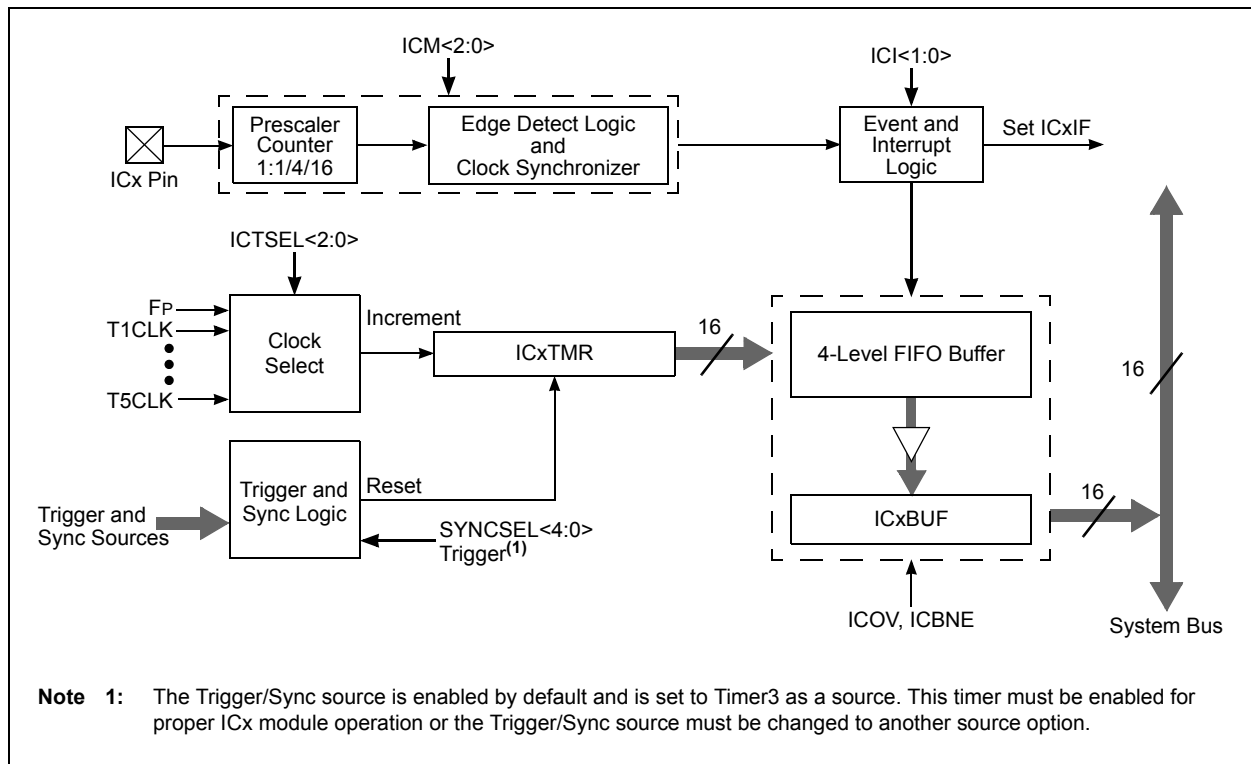
The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices support up to 16 input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 30 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

Note: Only IC1, IC2, IC3 and IC4 can trigger a DMA data transfer. If DMA data transfers are required, the FIFO buffer size must be set to '1' (IC1<1:0> = 00).

FIGURE 14-1: INPUT CAPTURE MODULE BLOCK DIAGRAM



REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0		U-0		U-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0	
—		—		—		DISSCK		DISSDO		MODE16		SMP ⁽⁴⁾		CKE ⁽¹⁾	
bit 15															bit 8
R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0	
SSEN ⁽²⁾		CKP		MSTEN		SPRE<2:0> ⁽³⁾						PPRE<1:0> ⁽³⁾			
bit 7															bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)

1 = Internal SPIx clock is disabled, pin functions as I/O

0 = Internal SPIx clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit

1 = SDOx pin is not used by the module; pin functions as I/O

0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit

1 = Communication is word-wide (16 bits)

0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit⁽⁴⁾Master mode:

1 = Input data is sampled at end of data output time

0 = Input data is sampled at middle of data output time

Slave mode:

The SMP bit must be cleared when SPIx module is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit⁽¹⁾

1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)

0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)⁽²⁾1 = SSx pin is used for Slave mode

0 = SSx pin is not used by module, pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level; active state is a low level

0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit

1 = Master mode

0 = Slave mode

Note 1: The CKE bit is not used in the Framed SPIx modes. Program this bit to '0' for Framed SPIx modes (FRMEN = 1).**2:** This bit must be cleared when FRMEN = 1.**3:** Do not set both primary and secondary prescalers to a value of 1:1.**4:** The SMP bit must be set only after setting the MSTEN bit. The SMP bit remains cleared if MSTEN = 0.

22.4 USB Control Registers

REGISTER 22-1: UxOTGSTAT: USB OTG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	U-0	R-0, HSC	U-0	R-0, HSC	R-0, HSC	U-0	R-0, HSC
ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD
bit 7							bit 0

Legend:

U = Unimplemented bit, read as '0'

R = Readable bit

W = Writable bit

HSC = Hardware Settable/Clearable bit

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'bit 7 **ID:** ID Pin State Indicator bit

1 = No cable is attached or a Type B plug has been plugged into the USB receptacle

0 = A Type A plug has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as '0'bit 5 **LSTATE:** Line State Stable Indicator bit

1 = The USB line state (as defined by SE0 and JSTATE) has been stable for the previous 1 ms

0 = The USB line state has NOT been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'bit 3 **SESVD:** Session Valid Indicator bit

1 = The VBUS voltage is above VA_SESS_VLD (as defined in the USB OTG Specification) on the A or B device

0 = The VBUS voltage is below VA_SESS_VLD on the A or B device

bit 2 **SESEND:** B-Session End Indicator bit

1 = The VBUS voltage is below VB_SESS_END (as defined in the USB OTG Specification) on the B device

0 = The VBUS voltage is above VB_SESS_END on the B device

bit 1 **Unimplemented:** Read as '0'bit 0 **VBUSVD:** A-VBUS Valid Indicator bit

1 = The VBUS voltage is above VA_VBUS_VLD (as defined in the USB OTG Specification) on the A device

0 = The VBUS voltage is below VA_VBUS_VLD on the A device

**REGISTER 28-3: PMADDR: PARALLEL MASTER PORT ADDRESS REGISTER
(MASTER MODES ONLY)⁽¹⁾**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS2	CS1	ADDR<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDR<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at Reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **CS2:** Chip Select 2 bit
 If PMCON<7:6> = 10 or 01:
 1 = Chip Select 2 is active
 0 = Chip Select 2 is inactive
 If PMCON<7:6> = 11 or 00:
 Bit functions as ADDR<15>.

bit 14 **CS1:** Chip Select 1 bit
 If PMCON<7:6> = 10:
 1 = Chip Select 1 is active
 0 = Chip Select 1 is inactive
 If PMCON<7:6> = 11 or 0x:
 Bit functions as ADDR<14>.

bit 13-0 **ADDR<13:0>:** Destination Address bits

Note 1: In Enhanced Slave mode, PMADDR functions as PMDOUT1, one of the two Data Buffer registers.

**TABLE 32-39: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

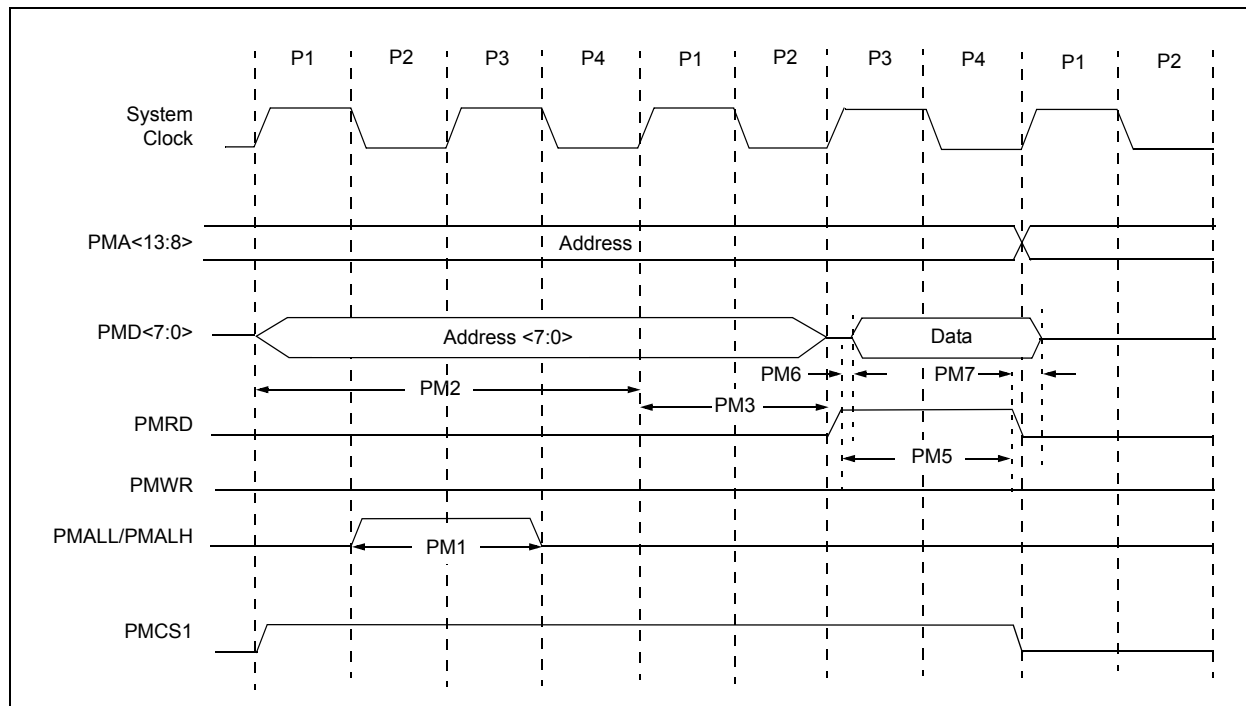
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH TscL2ssH	$\overline{SSx} \uparrow$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

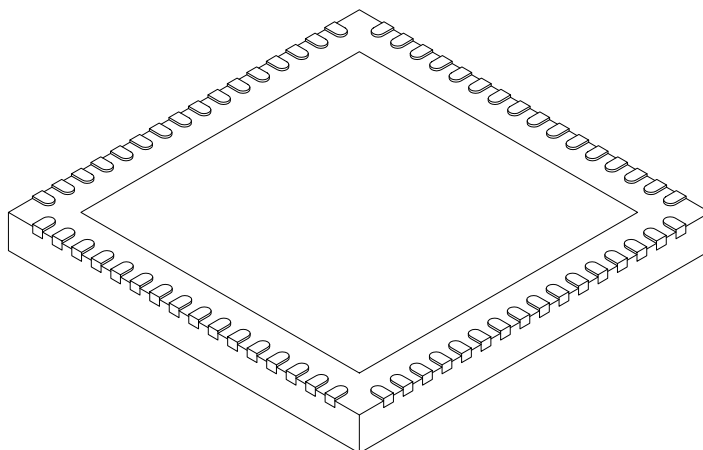
FIGURE 32-43: PARALLEL MASTER PORT READ TIMING DIAGRAM**TABLE 32-66: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
		Min.	Typ.	Max.	Units	Conditions
PM1	PMALL/PMALH Pulse Width	—	0.5 Tcy	—	ns	
PM2	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	1 Tcy	—	ns	
PM3	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	0.5 Tcy	—	ns	
PM5	PMRD Pulse Width	—	0.5 Tcy	—	ns	
PM6	PMRD or PMENB Active to Data In Valid (data setup time)	150	—	—	ns	
PM7	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	—	5	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.15 x 7.15 Exposed Pad [QFN]**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

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