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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu810-e-pf

Pin Diagrams (Continued)

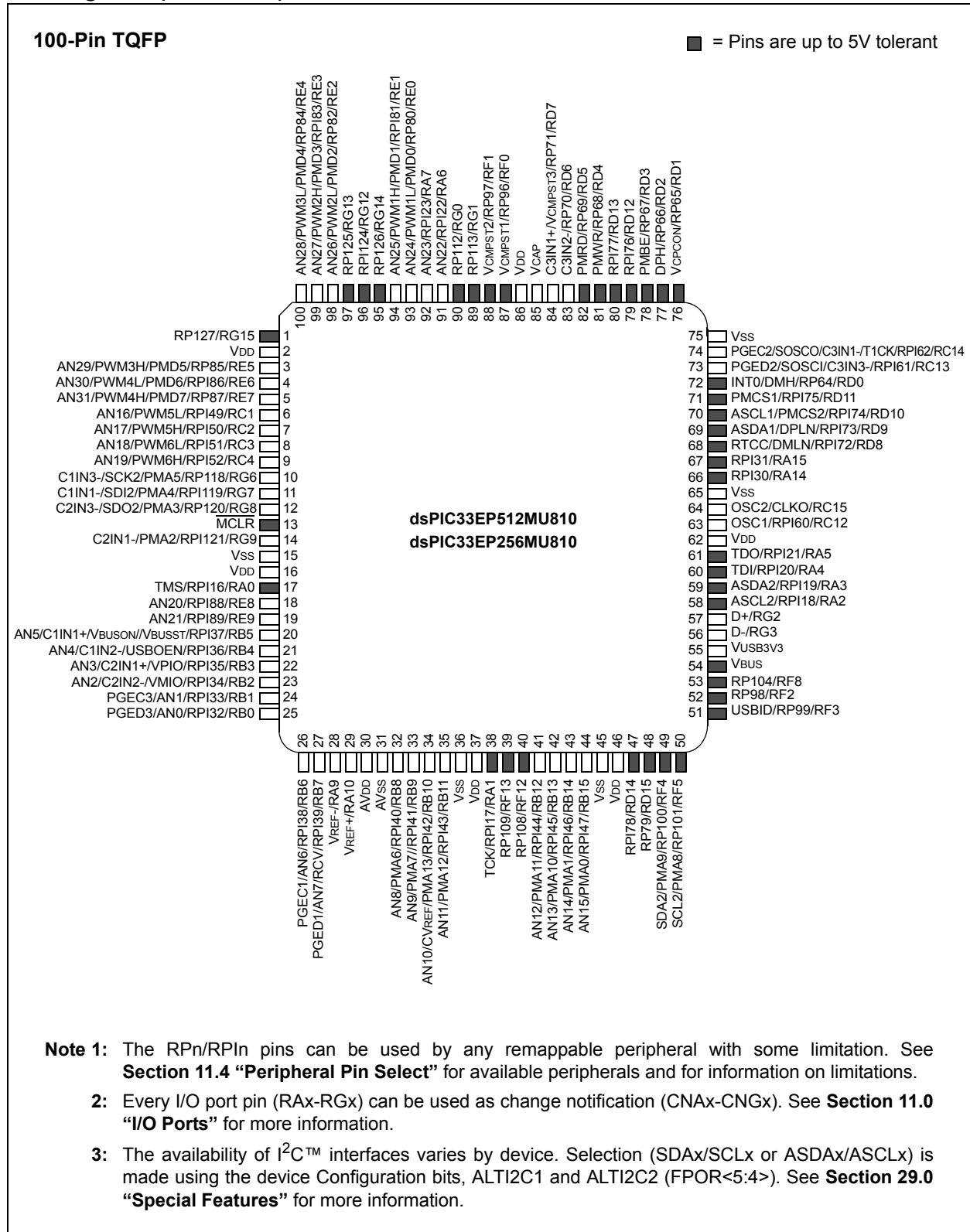


TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCL1 ⁽⁵⁾	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1 ⁽⁵⁾	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1 ⁽⁵⁾	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1 ⁽⁵⁾	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2 ⁽⁵⁾	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2 ⁽⁵⁾	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2 ⁽⁵⁾	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2 ⁽⁵⁾	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
INDX1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external clock input in Timer mode.
QEB1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP1 ⁽¹⁾	O	—	Yes	Quadrature Encoder Compare Output 1.
INDX2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Index2 pulse input.
HOME2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home2 pulse input.
QEA2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE12 mode. Auxiliary timer external clock input in Timer mode.
QEB2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase B input in QE12 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP2 ⁽¹⁾	O	—	Yes	Quadrature Encoder Compare Output 2.
COFS	I/O	ST	Yes	Data Converter Interface frame synchronization pin.
CCLK	I/O	ST	Yes	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Yes	Data Converter Interface serial data input pin.
CSDO	O	—	Yes	Data Converter Interface serial data output pin.
C1RX	I	ST	Yes	ECAN1 bus receive pin.
C1TX	O	—	Yes	ECAN1 bus transmit pin.
C2RX	I	ST	Yes	ECAN2 bus receive pin.
C2TX	O	—	Yes	ECAN2 bus transmit pin.
RTCC	O	—	No	Real-Time Clock alarm output.
CVREF	O	Analog	No	Comparator voltage reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs
C1OUT	O	—	Yes	Comparator 1 output.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.
- 2:** AVDD must be connected at all times.
- 3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.
- 4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.
- 5:** The availability of I²C™ interfaces varies by device. Refer to the “**Pin Diagrams**” section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.
- 6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

The diagram illustrates a power converter system controlled by a **dsPIC33EP** microcontroller. The system includes the following components and connections:

- dsPIC33EP Microcontroller:** The central control unit, featuring a **Comparator**, two **PWM** modules, another **Comparator**, and an **ADC Channel**.
- Power Stage:**
 - AC Input:** An AC source V_{AC} with magnitude $|V_{AC}|$ is connected through a transformer (inductor) to a full-bridge rectifier.
 - DC Link:** A capacitor is connected across the rectifier output.
 - Inverter:** Two IGBTs (circled) are driven by **FET Drivers** (labeled **k1** and **k2**) to produce a three-phase output. The output is connected to a three-phase load (inductor).
 - Output:** The three-phase output is connected to a three-phase load (inductor) and a three-phase output filter (inductor).
- Control and Feedback:**
 - Feedback:** The output voltage V_{OUT} is measured and fed back to the **ADC Channel** of the **dsPIC33EP**.
 - Reference:** A reference voltage V_{REF} is provided to the **Comparator** of the **dsPIC33EP**.
 - Control:** The **dsPIC33EP** generates **PWM** signals to control the **FET Drivers** and the **Comparator**.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0> : CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15, user interrupts are disabled) 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA : REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress
bit 3	N : MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	OV : MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	Z : MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C : MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

- Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.
- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.
- 3:** The IPL<2:0> bits are read-only when NSTDIS = 1 (INTCON1<15>).
- 4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	C2TXIP<2:0>			—	C1TXIP<2:0>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			4444
IPC18	0864	—	QEI2IP<2:0>			—	—	—	—	—	PSESMIP<2:0>			—	—	—	—	4040
IPC20	0868	—	U3TXIP<2:0>			—	U3RXIP<2:0>			—	U3EIP<2:0>			—	—	—	—	4440
IPC21	086A	—	U4EIP<2:0>			—	USB1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC22	086C	—	SPI3IP<2:0>			—	SPI3EIP<2:0>			—	U4TXIP<2:0>			—	U4RXIP<2:0>			4444
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	IC9IP<2:0>			—	OC9IP<2:0>			4444
IPC24	0870	—	—	—	—	—	—	—	—	—	PWM4IP<2:0>			—	PWM3IP<2:0>			0044
IPC29	087A	—	DMA9IP<2:0>			—	DMA8IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC30	087C	—	SPI4IP<2:0>			—	SPI4EIP<2:0>			—	DMA11IP<2:0>			—	DMA10IP<2:0>			4444
IPC31	087E	—	IC11IP<2:0>			—	OC11IP<2:0>			—	IC10IP<2:0>			—	OC10IP<2:0>			4444
IPC32	0880	—	DMA13IP<2:0>			—	DMA12IP<2:0>			—	IC12IP<2:0>			—	OC12IP<2:0>			4444
IPC33	0882	—	IC13IP<2:0>			—	OC13IP<2:0>			—	—	—	—	—	DMA14IP<2:0>			4404
IPC34	0884	—	IC15IP<2:0>			—	OC15IP<2:0>			—	IC14IP<2:0>			—	OC14IP<2:0>			4444
IPC35	0886	—	—	—	—	—	ICDIP<2:0>			—	IC16IP<2:0>			—	OC16IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	UAE	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	—	ILR<3:0>			VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15						bit 8	

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0> ⁽²⁾			RA	N	OV	Z	C
bit 7						bit 0	

Legend:	C = Clearable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 7-5 **IPL<2:0>**: CPU Interrupt Priority Level Status bits^(2,3)

- 111 = CPU Interrupt Priority Level is 7 (15, user interrupts are disabled)
- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13)
- 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see **Register 3-1: "SR: CPU Status Register"**.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>					
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Center frequency + 11.625% (8.23 MHz)

011110 = Center frequency + 11.25% (8.20 MHz)

•

•

•

000001 = Center frequency + 0.375% (7.40 MHz)

000000 = Center frequency (7.37 MHz nominal)

111111 = Center frequency – 0.375% (7.345 MHz)

•

•

•

100001 = Center frequency – 11.625% (6.52 MHz)

100000 = Center frequency – 12% (6.49 MHz)

Note 1: This register resets only on a Power-on Reset (POR).

REGISTER 9-6: ACLKDIV3: AUXILIARY CLOCK DIVISOR REGISTER 3^(1,2)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	APLLDIV<2:0>		
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **APLLDIV<2:0>:** PLL Feedback Divisor bits (PLL Multiplier Ratio)

111 = 24

110 = 21

101 = 20

100 = 19

011 = 18

010 = 17

001 = 16

000 = 15 (default)

Note 1: This register resets only on a Power-on Reset (POR).

2: This register is only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 3	SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled 0 = SPI1 module is enabled
bit 2	C2MD: ECAN2 Module Disable bit 1 = ECAN2 module is disabled 0 = ECAN2 module is enabled
bit 1	C1MD: ECAN1 Module Disable bit 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
bit 0	AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled

Note 1: This bit is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 10-7: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0		R/W-0		R/W-0		R/W-0		U-0		U-0		U-0		U-0			
DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	—	—	—	—	—	—	—	—		
DMA13MD	DMA9MD	DMA5MD	DMA1MD														
DMA14MD	DMA10MD	DMA6MD	DMA2MD														
—	DMA11MD	DMA7MD	DMA3MD														
bit 7																bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-8 **Unimplemented:** Read as '0'
- bit 7 **DMA12MD:** DMA12 Module Disable bit
 1 = DMA12 module is disabled
 0 = DMA12 module is enabled
- DMA13MD:** DMA13 Module Disable bit
 1 = DMA13 module is disabled
 0 = DMA13 module is enabled
- DMA14MD:** DMA14 Module Disable bit
 1 = DMA14 module is disabled
 0 = DMA14 module is enabled
- bit 6 **DMA8MD:** DMA3 Module Disable bit
 1 = DMA8 module is disabled
 0 = DMA8 module is enabled
- DMA9MD:** DMA2 Module Disable bit
 1 = DMA9 module is disabled
 0 = DMA9 module is enabled
- DMA10MD:** DMA10 Module Disable bit
 1 = DMA10 module is disabled
 0 = DMA10 module is enabled
- DMA11MD:** DMA11 Module Disable bit
 1 = DMA11 module is disabled
 0 = DMA11 module is enabled
- bit 5 **DMA4MD:** DMA4 Module Disable bit
 1 = DMA4 module is disabled
 0 = DMA4 module is enabled
- DMA5MD:** DMA5 Module Disable bit
 1 = DMA5 module is disabled
 0 = DMA5 module is enabled
- DMA6MD:** DMA6 Module Disable bit
 1 = DMA6 module is disabled
 0 = DMA6 module is enabled
- DMA7MD:** DMA7 Module Disable bit
 1 = DMA7 module is disabled
 0 = DMA7 module is enabled

REGISTER 16-14: PHASEx: PWMx PRIMARY PHASE SHIFT REGISTER^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PHASEx<15:0>**: PWM Phase Shift Value or Independent Time Base Period for the PWM Generator bits**Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase shift value for PWMxH and PWMxL outputs.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Phase shift value for PWMxH only.

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Independent time base period value for PWMxH only.

REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT<4:0>				
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE<6:0>						
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits

10000-11111 = Reserved

01111 = Filter 15

•

•

•

00001 = Filter 1

00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved

1000100 = FIFO almost full interrupt

1000011 = Receiver overflow interrupt

1000010 = Wake-up interrupt

1000001 = Error interrupt

1000000 = No interrupt

•

•

•

0010000-0111111 = Reserved

0001111 = RB15 buffer interrupt

•

•

•

0001001 = RB9 buffer interrupt

0001000 = RB8 buffer interrupt

0000111 = TRB7 buffer interrupt

0000110 = TRB6 buffer interrupt

0000101 = TRB5 buffer interrupt

0000100 = TRB4 buffer interrupt

0000011 = TRB3 buffer interrupt

0000010 = TRB2 buffer interrupt

0000001 = TRB1 buffer interrupt

0000000 = TRB0 Buffer interrupt

REGISTER 22-11: UxCNFG2: USB CONFIGURATION REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	UVCMPSEL	PUVBUS	EXTI2CEN	UVBUSDIS ⁽¹⁾	UVCMPDIS ⁽¹⁾	UTRDIS ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **UVCMPSEL:** USB External Comparator Input Mode Select bit

When UVCMPDIS is Set:

1 = Use 3-pin input for external comparators

0 = Use 2-pin input for external comparators

bit 4 **PUVBUS:** VBUS Pull-up Enable bit

1 = Pull-up on VBUS pin is enabled

0 = Pull-up on VBUS pin is disabled

bit 3 **EXTI2CEN:** I²C™ Interface for External Module Control Enable bit

1 = External module(s) controlled via I²C interface

0 = External module(s) controlled via dedicated pins

bit 2 **UVBUSDIS:** USB On-Chip 5V Boost Regulator Builder Disable bit⁽¹⁾

1 = On-chip boost regulator builder is disabled; digital output control interface is enabled

0 = On-chip boost regulator builder is active

bit 1 **UVCMPDIS:** USB On-Chip VBUS Comparator Disable bit⁽¹⁾

1 = On-chip charge VBUS comparator is disabled; digital input status interface is enabled

0 = On-chip charge VBUS comparator is active

bit 0 **UTRDIS:** USB On-Chip Transceiver Disable bit⁽¹⁾

1 = On-chip transceiver is disabled; digital transceiver interface is enabled

0 = On-chip transceiver is active

Note 1: Do not change this bit while the USBPWR bit is set (UxPWRC<0> = 1).

REGISTER 22-12: UxOTGIR: USB OTG INTERRUPT STATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	U-0	R/K-0, HS
IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDF	SESENDIF	—	VBUSVDIF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	K = Write '1' to clear bit	HS = Hardware Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit

1 = Change in ID state is detected

0 = No ID state change

bit 6 **T1MSECIF:** 1 Millisecond Timer bit

1 = The 1 millisecond timer has expired

0 = The 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit

1 = USB line state (as defined by the SE0 and JSTATE bits) has been stable for 1 ms, but different from last time

0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit

1 = Activity on the D+/D- lines or VBUS is detected

0 = No activity on the D+/D- lines or VBUS is detected

bit 3 **SESVDF:** Session Valid Change Indicator bit

1 = VBUS has crossed VA_SESS_VLD (as defined in the USB OTG Specification)⁽¹⁾

0 = VBUS has not crossed VA_SESS_VLD

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit

1 = VBUS change on B-device is detected; VBUS has crossed VB_SESS_END (as defined in the USB OTG Specification)⁽¹⁾

0 = VBUS has not crossed VA_SESS_END

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit

1 = VBUS change on A-device is detected; VBUS has crossed VA_VBUS_VLD (as defined in the USB OTG Specification)⁽¹⁾

0 = No VBUS change on A-device is detected

Note 1: VBUS threshold crossings may be either rising or falling.

**REGISTER 25-3: CMxMSKSRCA: COMPARATOR x MASK SOURCE SELECT
CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

REGISTER 26-6: RTCVAL (WHEN RTCPTR<1:0> = 01): WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY<2:0>		
bit 15					bit 8		

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN<1:0>		HRONE<3:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 26-7: RTCVAL (WHEN RTCPTR<1:0> = 00): MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN<2:0>			MINONE<3:0>			
bit 15				bit 8			

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN<2:0>			SECONE<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **Unimplemented:** Read as '0'
- bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.
- bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.
- bit 7 **Unimplemented:** Read as '0'
- bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.
- bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

**TABLE 32-40: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{SSx} \uparrow$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param.	Symbol	Characteristic ⁽³⁾		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽¹⁾	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽¹⁾	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.6	—	μs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	See Note 2

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: The typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 7.0 “Interrupt Controller”	Added the VAR bit (CORCON<15>) to the Core Control Register (see Register 7-2). Changed the default POR value for the GIE bit (INTCON2<15>) to R/W-1 (see Register 7-4). Changed the VECNUM<7:0> = 11111111 pending interrupt vector number to 263 in the Interrupt Control and Status Register (see Register 7-7).
Section 8.0 “Direct Memory Access (DMA)”	Updated Section 8.1 “DMAC Registers”. Updated DMA Controller in Figure 8-1. Added Note 1 to the DMA Channel x Peripheral Address Register (see Register 8-7). Added Note 1 and Note 2 to the DMA Channel x Transfer Count Register (see Register 8-8). Updated all RQCOLx bit definitions, changing Peripheral Write to Transfer Request in the DMA Request Collision Status Register (see Register 8-12).
Section 9.0 “Oscillator Configuration”	Added the Reference Oscillator Control Register (see Register 9-7). Added Note 3 and 4 to the CLKDIV Register (see Register 9-2)
Section 10.0 “Power-Saving Features”	Added the DCIMD and C2MD bits to the Peripheral Module Disable Control Register 1 (see Register 10-1) Added the IC6MD, IC5MD, IC4MD, IC3MD, OC8MD, OC7MD, OC6MD, and OC5MD bits to the Peripheral Module Disable Control Register 2 (see Register 10-2) Added the T9MD, T8MD, T7MD, and T6MD bits and removed the DSC1MD bit in the Peripheral Module Disable Control Register 3 (see Register 10-3). Added the REFOMD bit (PMD4<3>) to the Peripheral Module Disable Control Register 4 (see Register 10-4).
Section 11.0 “I/O Ports”	Updated the first paragraph of Section 11.2 “Configuring Analog and Digital Port Pins”. Updated the PWM Fault, Dead-Time Compensation, and Synch Input register numbers of the Selectable Input Sources (see Table 11-2). Removed RPINR22 register. Bit names and definitions were modified in the following registers: - Peripheral Pin Select Input Register 37 (see Register 11-37) - Peripheral Pin Select Input Register 38 (see Register 11-38) - Peripheral Pin Select Input Register 39 (see Register 11-39) - Peripheral Pin Select Input Register 40 (see Register 11-40) - Peripheral Pin Select Input Register 41 (see Register 11-41) - Peripheral Pin Select Input Register 42 (see Register 11-42) - Peripheral Pin Select Input Register 43 (see Register 11-43)
Section 12.0 “Timer1”	Added Note in Register 12-1.
Section 14.0 “Input Capture”	Added Note 1 to the Input Capture Block Diagram (see Figure 14-1).
Section 15.0 “Output Compare”	Added Note 1 to the Output Compare Module Block Diagram (see Figure 15-1). Added Note 2 to the Output Compare x Control Register 2 (see Register 15-2).
Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMU806/810/814 Devices Only)”	Added Comparator bit values for the CLSRC<4:0> and FLTSRC<4:0> bits in the PWM Fault Current-Limit Control Register (see Register 16-21).

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 21.0 “Enhanced CAN (ECAN™) Module”	Added the CANCKS bit to the ECAN Control Register 1 (CiCTRL1) (see Register 21-1).
Section 22.0 “USB On-The-Go (OTG) Module”	Removed the USB 3.3V Regulator logic from the USB Interface Diagram (see Figure 22-1).
Section 23.0 “10-bit/12-bit Analog-to-Digital Converter (ADC)”	Updated the ADC Conversion Clock Period Block Diagram (see Figure 23-2).
Section 29.0 “Special Features”	Updated the last paragraph of Section 29.1 “Configuration Bits” Added a note box after the last paragraph of Section 29.3 “BOR: Brown-out Reset (BOR)”. Added the RTSP Effect column to the Configuration Bits Description (see Table 29-2).
Section 30.0 “Instruction Set Summary”	Updated all Status Flags Affected to None for the MOV instruction and added Note 2 (see Table 30-2).
Section 32.0 “Electrical Characteristics”	Updated the Absolute Maximum Ratings (see page 457). Added Note 1 to the Operating MIPS vs. Voltage (see Table 32-1). Added parameter DI31 (ICNPD) to the I/O Pin Input Specifications (see Table 32-9). Updated the Minimum value for parameter DO26 in the I/O Pin Output Specifications (see Table 32-10). Updated the Minimum value for parameter D132b and the Minimum and Maximum values for parameters D136a, D136b, D137a, D137b, D138a, and D138b in the Program Memory specification (see Table 32-12). Updated the Minimum, Typical, and Maximum values for parameter OS10 (Oscillator Crystal Frequency: SOSC) in the External Clock Timing Requirements (see Table 32-16). Added Note 2 to the PLL Clock Timing Specifications (see Table 32-17). Updated all Timer1 External Clock Timing Requirements (see Table 32-23). Replaced Table 32-34 with Timer2, Timer4, Timer6, Timer8 External Clock Timing Requirements and Timer3, Timer5, Timer7, Timer9 External Clock Timing Requirements (see Table 32-24 and Table 32-25, respectively). Updated the Maximum value for parameter OC15 and the Minimum value for parameter OC20 in the OC/PWM Mode Timing Requirements (see Table 32-29). Updated the Operating Temperature in the ECAN Module I/O Timing Requirements and USB OTG Timing Requirements (see Table 32-51 and Table 32-53, respectively). Updated all SPI specifications (see Figure 32-15 through Figure 32-30 and Table 32-33 through Table 32-48). Removed Note 4 from the DCI Module Timing Requirements (see Table 32-59). Updated the Standard Operating Conditions voltage for the Comparator Specifications (see Table 32-61 through Table 32-64).