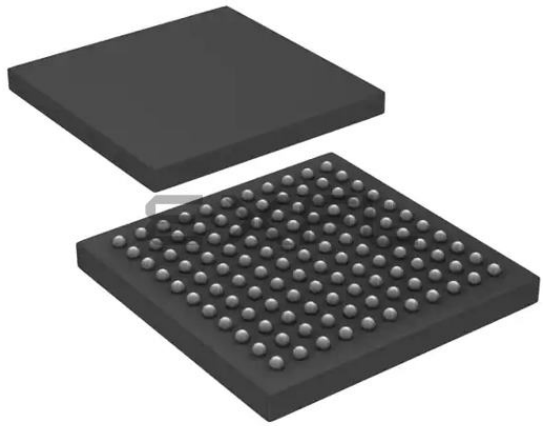


Welcome to E-XFL.COM

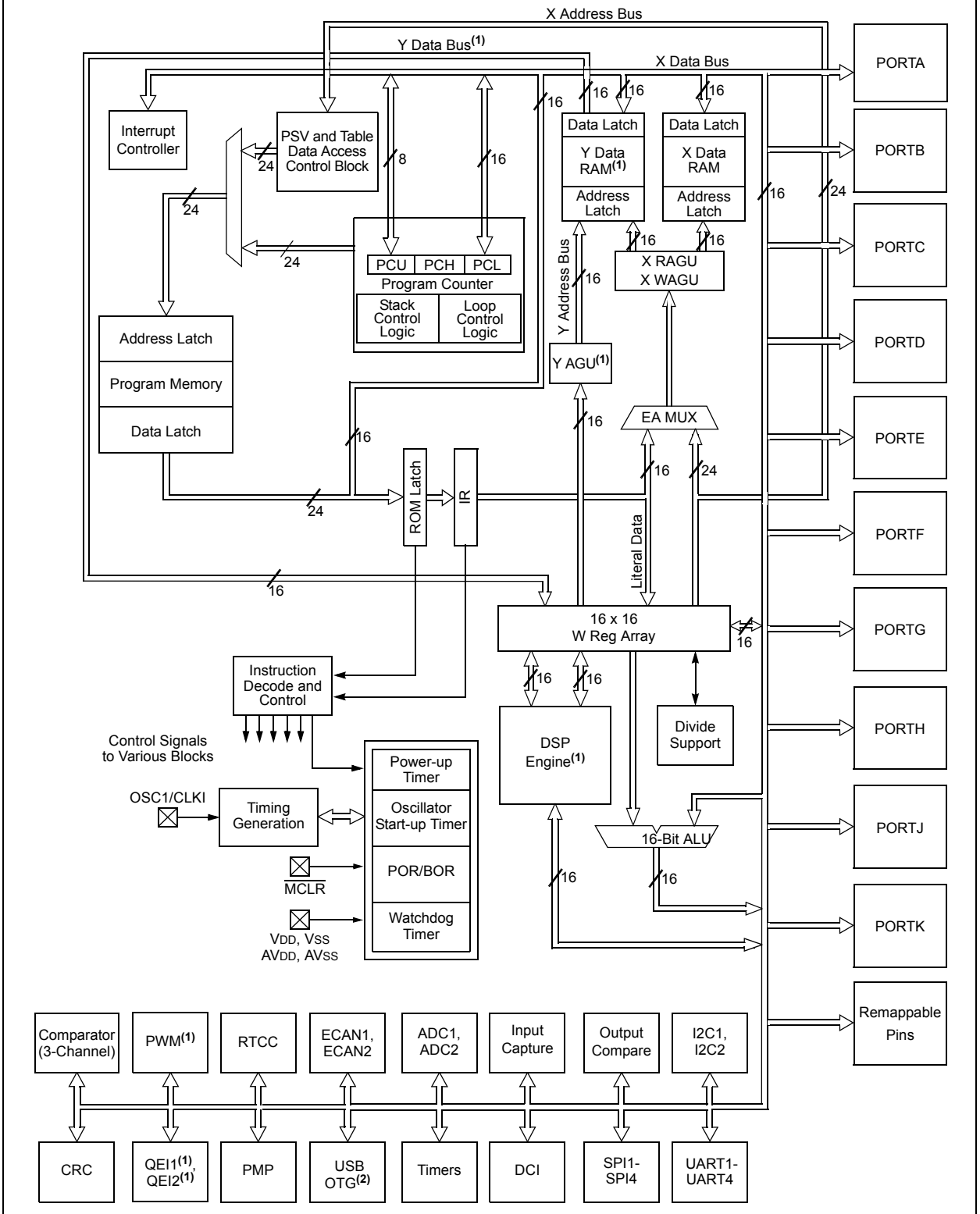
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu810-i-bg

FIGURE 3-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

2: This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.

3.5 Programmer's Model

The programmer's model is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, all devices in this family contain control registers for interrupts, while the dsPIC33EPXXX(GP/MC/MU)806/810/814 devices contain control registers for Modulo and Bit-reversed Addressing. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine Status register
SPLIM	Stack Pointer Limit Value register
TBLPAG	Table Memory Page Address register
DSRPAG	Extended Data Space (EDS) Read Page register
DSWPAG	Extended Data Space (EDS) Write Page register
RCOUNT	REPEAT Loop Count register
DCOUNT(1)	DO Loop Count register
DOSTARTH(1,2), DOSTARTL(1,2)	DO Loop Start Address register (High and Low)
DOENDH(1), DOENDL(1)	DO Loop End Address register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: This register is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-55: PORTA REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
PORTA	0E02	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
LATA	0E04	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
ODCA	0E06	ODCA15	ODCA14	—	—	—	—	—	—	—	—	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	CNIEA15	CNIEA14	—	—	—	CNIEA10	CNIEA9	—	CNIEA7	CNIEA6	CNIEA5	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	CNPUA15	CNPUA14	—	—	—	CNPUA10	CNPUA9	—	CNPUA7	CNPUA6	CNPUA5	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	CNPDA15	CNPDA14	—	—	—	CNPDA10	CNPDA9	—	CNPDA7	CNPDA6	CNPDA5	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	—	—	—	—	—	ANSA10	ANSA9	—	ANSA7	ANSA6	—	—	—	—	—	—	06C0

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-56: PORTB REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB9	ANSB8	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	FFFF

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-57: PORTC REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	TRISC14	TRISC13	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	F01E
PORTC	0E22	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
LATC	0E24	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
ODCC	0E26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENC	0E28	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	—	—	—	—	—	CNIEC4	CNIEC3	CNIEC2	CNIEC1	—	0000
CNPUC	0E2A	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	CNPUC4	CNPUC3	CNPUC2	CNPUC1	—	0000
CNPDC	0E2C	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	CNPDC4	CNPDC3	CNPDC2	CNPDC1	—	0000
ANSELC	0E2E	—	ANSC14	ANSC13	—	—	—	—	—	—	—	—	ANSC4	ANSC3	ANSC2	ANSC1	—	601E

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER (CONTINUED)

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

Input Name(1)	Function Name	Register	Configuration Bits
DCI Data Input	CSDI	RPINR24	CSDIR<6:0>
DCI Clock Input	CSCKIN	RPINR24	CSCKR<6:0>
DCI FSYNC Input	COFSIN	RPINR25	COFSR<6:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	$\overline{\text{U4CTS}}$	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	$\overline{\text{SS3}}$	RPINR30	SS3R<6:0>
SPI4 Data Input	SDI4	RPINR31	SDI4R<6:0>
SPI4 Clock Input	SCK4	RPINR31	SCK4R<6:0>
SPI4 Slave Select	$\overline{\text{SS4}}$	RPINR32	SS4R<6:0>
Input Capture 9	IC9	RPINR33	IC9R<6:0>
Input Capture 10	IC10	RPINR33	IC10R<6:0>
Input Capture 11	IC11	RPINR34	IC11R<6:0>
Input Capture 12	IC12	RPINR34	IC12R<6:0>
Input Capture 13	IC13	RPINR35	IC13R<6:0>
Input Capture 14	IC14	RPINR35	IC14R<6:0>
Input Capture 15	IC15	RPINR36	IC15R<6:0>
Input Capture 16	IC16	RPINR36	IC16R<6:0>
Output Compare Fault C	OCFC	RPINR37	OCFCR<6:0>
PWM Fault 5(2)	FLT5	RPINR42	FLT5R<6:0>
PWM Fault 6(2)	FLT6	RPINR42	FLT6R<6:0>
PWM Fault 7(2)	FLT7	RPINR43	FLT7R<6:0>
PWM Dead-Time Compensation 1(2)	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2(2)	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3(2)	DTCMP3	RPINR39	DTCMP3R<6:0>
PWM Dead-Time Compensation 4(2)	DTCMP4	RPINR40	DTCMP4R<6:0>
PWM Dead-Time Compensation 5(2)	DTCMP5	RPINR40	DTCMP5R<6:0>
PWM Dead-Time Compensation 6(2)	DTCMP6	RPINR41	DTCMP6R<6:0>
PWM Dead-Time Compensation 7(2)	DTCMP7	RPINR41	DTCMP7R<6:0>
PWM Synch Input 1(2)	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Synch Input 2(2)	SYNCI2	RPINR38	SYNCI2R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
010 1011	I	RPI43
010 1100	I	RPI44
101 1010	—	Reserved
101 1011	—	Reserved
101 1100	—	Reserved
101 1101	—	Reserved
101 1110	—	Reserved
101 1111	—	Reserved
110 0000	I/O	RP96
110 0001	I/O	RP97
110 0010	I/O	RP98
110 0011	I/O	RP99
110 0100	I/O	RP100
110 0101	I/O	RP101
110 0110	I/O	RP102
110 0111	—	Reserved
110 1000	I/O	RP104
110 1001	—	Reserved
110 1010	—	Reserved
110 1011	—	Reserved
110 1100	I/O	RP108

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
101 1000	I	RPI88
101 1001	I	RPI89
110 1101	I/O	RP109
110 1110	—	Reserved
110 1111	—	Reserved
111 0000	I/O	RP112
111 0001	I/O	RP113
111 0010	—	Reserved
111 0011	—	Reserved
111 0100	—	Reserved
111 0101	—	Reserved
111 0110	I/O	RP118
111 0111	I	RPI119
111 1000	I/O	RP120
111 1001	I	RPI121
111 1010	—	Reserved
111 1011	—	Reserved
111 1100	I	RPI124
111 1101	I/O	RP125
111 1110	I/O	RP126
111 1111	I/O	RP127

Note 1: See **Section 11.4.4.2 “Virtual Connections”** for more information on selecting this pin assignment.

11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 32-9 in **Section 32.0 "Electrical Characteristics"** under "Injection Current", have internal protection diodes to VDD and VSS; the term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin, (i.e., ANx, see Table 1-1 in **Section 1.0 "Device Overview"**), are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin, automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared analog pin (see Table 1-1 in **Section 1.0 "Device Overview"**), the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

Note:	Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left to right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin. Dedicated peripheral functions are always higher priority than remappable functions. I/O pins are always the lowest priority.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD-0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of the data sheet. For example:

   VOH = 2.4v @ IOH = -8 mA and VDD = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 32.0 "Electrical Characteristics"** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one "output" function can be active on a given pin at any time regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
   c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
   d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
   e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self test.
   f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including any pin with a single output from either a dedicated or remappable "output".

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT3R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT3R<6:0>:** Assign External Interrupt 3 (INT3) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0 HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>				
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWM output is driven high on a Fault
- 0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on Fault condition
- 0 = OCx pin I/O state defined by FLTOUT bit on Fault condition

bit 12 **OCINV:** OCMP Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
- 1 = Triggers OCx from source designated by SYNCSELx bits
- 0 = Synchronizes OCx with source designated by SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit
- 1 = OCx is tri-stated
- 0 = Output compare module drives the OCx pin

Note 1: Do not use the OCx module as its own Sync or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER (CONTINUED)

bit 3-2 **CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits

IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
If current limit is active, PWMxH is driven to the state specified by CLDAT<1>.
If current limit is active, PWMxL is driven to the state specified by CLDAT<0>.

IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
The CLDAT<1:0> bits are ignored.

bit 1 **SWAP:** Swap PWMxH and PWMxL Pins bit

1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit

1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base
0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWM module is enabled (PTEN = 1).

REGISTER 17-10: INDXxHLD: INDEX COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **INDXHLD<15:0>:** Hold Register for Reading and Writing INDXxCNTH bits

REGISTER 17-11: QEIxICH: QEIx INITIALIZATION/CAPTURE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **QEIIC<31:16>:** QEIx High Word Used to Form 32-Bit Initialization/Capture Register (QEIxIC) bits

REGISTER 17-12: QEIxICL: QEIx INITIALIZATION/CAPTURE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **QEIIC<15:0>:** QEIx Low Word Used to Form 32-Bit Initialization/Capture Register (QEIxIC) bits

REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bit 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bit 15-12)

REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bit 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bit 15-12)

REGISTER 22-22: UxEPn: USB ENDPOINT n CONTROL REGISTERS (n = 0 TO 15)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LSPD(1)	RETRYDIS(1)	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (UEP0 only)(1)
1 = Direct connection to a low-speed device is enabled
0 = Direct connection to a low-speed device is disabled

bit 6 **RETRYDIS:** Retry Disable bit (UEP0 only)(1)
1 = Retry NAK transactions is disabled
0 = Retry NAK transactions is enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN and EPRXEN = 1:
1 = Disable Endpoint n from control transfers; only TX and RX transfers are allowed
0 = Enable Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed
For all other combinations of EPTXEN and EPRXEN:
This bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive is enabled
0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit is enabled
0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint handshake is enabled
0 = Endpoint handshake is disabled (typically used for isochronous endpoints)

Note 1: These bits are available only for UxEP0 and only in Host mode. For all other UxEPn registers, these bits are always unimplemented and read as '0'.

REGISTER 23-7: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	CH0SB<4:0>(1)				
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	CH0SA<4:0>(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample B bit
Same definition as bit 7.

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample B bits(1)
Same definition as bits<4:0>.

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample A bit
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 6-5 **Unimplemented:** Read as '0'

bit 4-0 **CH0SA<4:0>:** Channel 0 Positive Input Select for Sample A bits(1)
11111 = Channel 0 positive input is AN31
11110 = Channel 0 positive input is AN30
•
•
•
00010 = Channel 0 positive input is AN2
00001 = Channel 0 positive input is AN1
00000 = Channel 0 positive input is AN0

Note 1: The AN16 through AN31 pins are not available for the ADC2 module. The AN16 through AN23 pins are not available for dsPIC33EP256MU806 (64-pin) devices.

REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 **ABEN:** AND Gate B Input Enable bit
1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

bit 2 **ABNEN:** AND Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1 **AAEN:** AND Gate A Input Enable bit
1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0 **AANEN:** AND Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate

TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(2)	Status Flags Affected
46	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit9,DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, DSWPAG	Move Ws<8:0> to DSWPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Prefetch and store accumulator	1	1	None
49	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1)	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1)	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
50	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1)	-(Multiply Wm by Wn) to Accumulator	1	1	None
51	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB(1)	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
52	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc(1)	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc(1)	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc(1)	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc(1)	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc(1)	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc(1)	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: This instruction is available in dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 32-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Pins 5V Tolerant(4)	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant(4)	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +85°C
DI51a		I/O Pins Not 5V Tolerant(4)	—	—	±1	μA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +85°C
DI51b		I/O Pins Not 5V Tolerant(4)	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +125°C
DI51c		I/O Pins Not 5V Tolerant(4)	—	—	±1	μA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +125°C
DI55		$\overline{\text{MCLR}}$	—	—	±1	μA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See **“Pin Diagrams”** for the 5V tolerant I/O pins.

5: VIL source < (VSS – 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

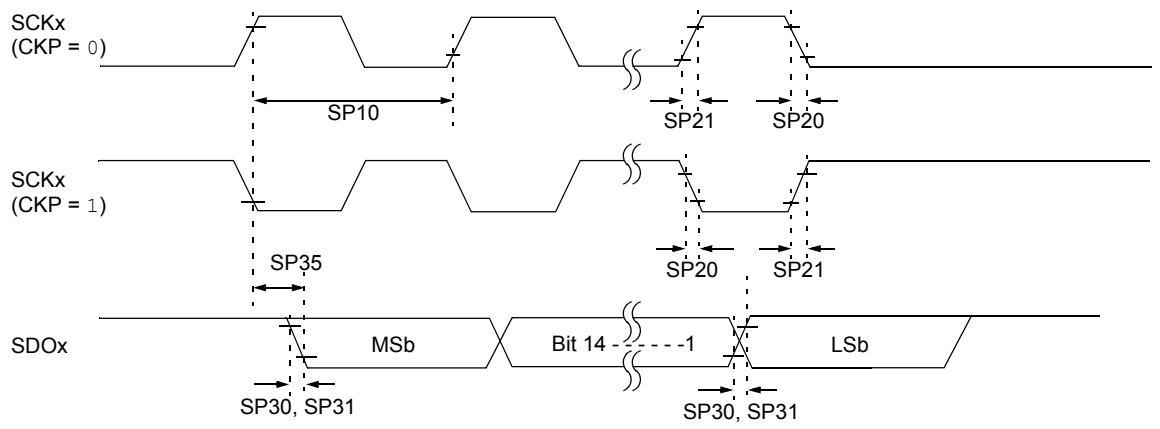
9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

10: These parameters are characterized, but not tested.

TABLE 32-41: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 32-42	—	—	0,1	0,1	0,1
10 MHz	—	Table 32-43	—	1	0,1	1
10 MHz	—	Table 32-44	—	0	0,1	1
15 MHz	—	—	Table 32-45	1	0	0
11 MHz	—	—	Table 32-46	1	1	0
15 MHz	—	—	Table 32-47	0	1	0
11 MHz	—	—	Table 32-48	0	0	0

FIGURE 32-23: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-61: COMPARATOR TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
300	TRESP	Response Time(2)	—	150	400	ns	
301	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	μs	

Note 1: Parameters are characterized but not tested.

2: Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

3: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

TABLE 32-62: COMPARATOR MODULE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D300	VIOFF	Input Offset Voltage	—	±10	—	mV	
D301	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
D302	CMRR	Common-Mode Rejection Ratio	-54	—	—	dB	
D305	IVREF	Internal Voltage Reference	0.19	0.20	0.21	V	BGSEL<1:0> = 10
			0.57	0.60	0.63	V	BGSEL<1:0> = 01
			1.14	1.20	1.26	V	BGSEL<1:0> = 00

Note 1: Parameters are characterized but not tested.

2: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.