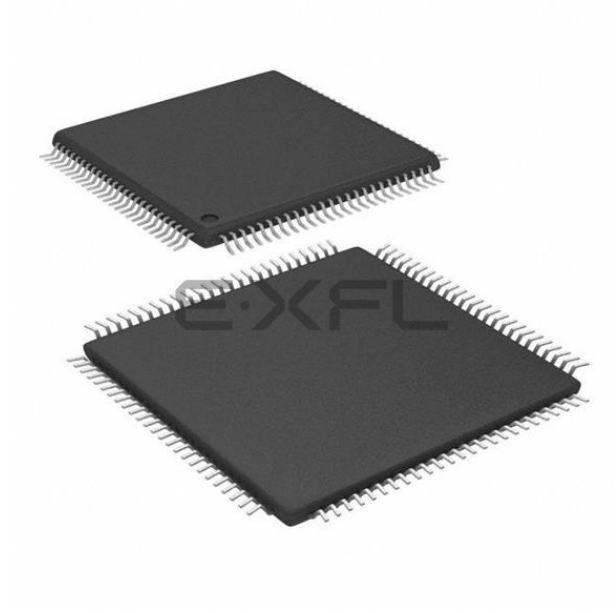
Microchip Technology - PIC24EP512GU810-I/PT Datasheet



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Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu810-i-pt

TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PTPER<15:0>																FFF8
SEVTCMP	0C06	SEVTCMP<15:0>																0000
MDC	0C0A	MDC<15:0>																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	STPER<15:0>																FFF8
SSEVTCMP	0C14	SSEVTCMP<15:0>																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON1	0C24	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC1	0C26	PDC1<15:0>																0000
PHASE1	0C28	PHASE1<15:0>																0000
DTR1	0C2A	—	—	DTR1<13:0>														0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>														0000
SDC1	0C2E	SDC1<15:0>																0000
SPHASE1	0C30	SPHASE1<15:0>																0000
TRIG1	0C32	TRGCMP<15:0>																0000
TRGCON1	0C34	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>						0000
PWMCAP1	0C38	PWMCAP1<15:0>																0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB<11:0>												0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: UART1, UART2, UART3 and UART4 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UARTx Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UARTxReceive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UARTx Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UARTx Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler																0000
U3MODE	0250	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U3STA	0252	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U3TXREG	0254	—	—	—	—	—	—	—	UARTx Transmit Register									xxxx
U3RXREG	0256	—	—	—	—	—	—	—	UARTx Receive Register									0000
U3BRG	0258	Baud Rate Generator Prescaler																0000
U4MODE	02B0	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U4STA	02B2	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U4TXREG	02B4	—	—	—	—	—	—	—	UARTx Transmit Register									xxxx
U4RXREG	02B6	—	—	—	—	—	—	—	UARTx Receive Register									0000
U4BRG	02B8	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADRU<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMADRU<7:0>:** Nonvolatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-3: NVMADR: NONVOLATILE MEMORY ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Write Address bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

6.1 Resets Resources

Many useful resources related to Resets are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

6.1.1 KEY RESOURCES

- **Section 8. "Reset"** (DS70602) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

6.2 RCON Control Register

All types of device Resets set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT3R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT3R<6:0>:** Assign External Interrupt 3 (INT3) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

17.2 QEI Control Registers

REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIEN	—	QEISIDL	PIMOD<2:0>(1)			IMV<1:0>(2)	
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV<2:0>(3)			CNTPOL	GATEN	CCM<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **QEIEN:** Quadrature Encoder Interface Module Counter Enable bit
1 = Module counters are enabled
0 = Module counters are disabled, but SFRs can be read or written to

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** QEI Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits(1)
111 = Reserved
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals the QEIxGEC register
100 = Second index event after home event initializes position counter with contents of the QEIxIC register
011 = First index event after home event initializes position counter with contents of the QEIxIC register
010 = Next index input event initializes the position counter with contents of the QEIxIC register
001 = Every index input event resets the position counter
000 = Index input event does not affect position counter

bit 9-8 **IMV<1:0>:** Index Match Value bits(2)
11 = Index match occurs when QEB = 1 and QEA = 1
10 = Index match occurs when QEB = 1 and QEA = 0
01 = Index match occurs when QEB = 0 and QEA = 1
00 = Index input event does not affect position counter

bit 7 **Unimplemented:** Read as '0'

Note 1: When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM = 00, and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

21.0 ENHANCED CAN (ECAN™) MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

21.1 Overview

The Enhanced Controller Area Network (ECAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices contain two ECAN modules.

The ECANx module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN Specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN Specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The ECANx module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0-8 Bytes Data Length
- Programmable Bit Rate up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to 8 Transmit Buffers with Application-Specific Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (standard/extended identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet™ Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback mode Supports Self-Test Operation
- Signaling via Interrupt Capabilities for all CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture Module (IC2 for the ECAN1 and ECAN2 modules) for Time-Stamping and Network Synchronization
- Low-Power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

REGISTER 22-15: UxIR: USB INTERRUPT STATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R-0	R/K-0, HS
STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	DETACHIF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	K = Write '1' to clear bit	HS = Hardware Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = A STALL handshake was sent by the peripheral device during the handshake phase of the transaction in Device mode
- 0 = A STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit
- 1 = A peripheral attachment has been detected by the module; set if the bus state is not SE0 and there has been no bus activity for 2.5 μs
- 0 = No peripheral attachment is detected

bit 5 **RESUMEIF:** Resume Interrupt bit
- 1 = A K-State is observed on the D+ or D- pin for 2.5 μs (differential '1' for low speed, differential '0' for full speed)
- 0 = No K-State is observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition is detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition is detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit
- 1 = Processing of current token is complete; read USTAT register for endpoint BDT information
- 0 = Processing of current token is not complete; clear USTAT register or load next token from STAT

bit 2 **SOFIF:** Start-of-Frame Token Interrupt bit
- 1 = Start-of-Frame threshold is reached by the host
- 0 = No Start-of-Frame token threshold is reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit
- 1 = An unmasked error condition has occurred; only error states enabled in the UxEIE register can set this bit
- 0 = No unmasked error condition has occurred

bit 0 **DETACHIF:** Detach Interrupt bit
- 1 = A peripheral detachment has been detected by the module
- 0 = No peripheral detachment has been detected

24.0 DATA CONVERTER INTERFACE (DCI) MODULE

Note 1: This data sheet is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Section 20. Data Converter Interface (DCI)"** (DS70356) of the *"dsPIC33E/PIC24E Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

24.1 Module Introduction

The Data Converter Interface (DCI) module allows simple interfacing of devices, such as audio coder/decoders (Codecs), ADC and D/A Converters. The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I^2S) Interface
- AC-Link Compliant mode

General features include:

- Programmable word size up to 16 bits
- Supports up to 16 time slots, for a maximum frame size of 256 bits
- Data buffering for up to 4 samples without CPU overhead

FIGURE 24-1: DCI MODULE BLOCK DIAGRAM

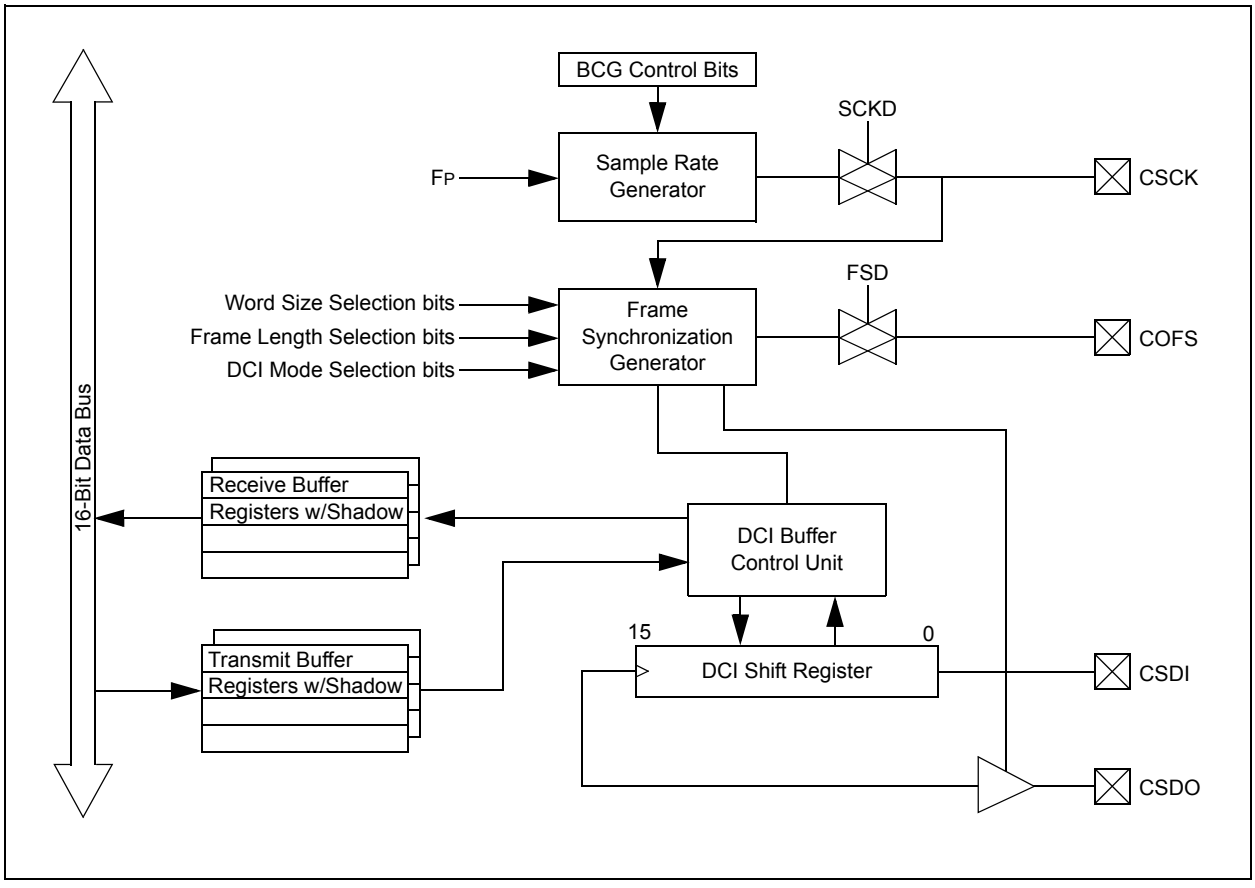
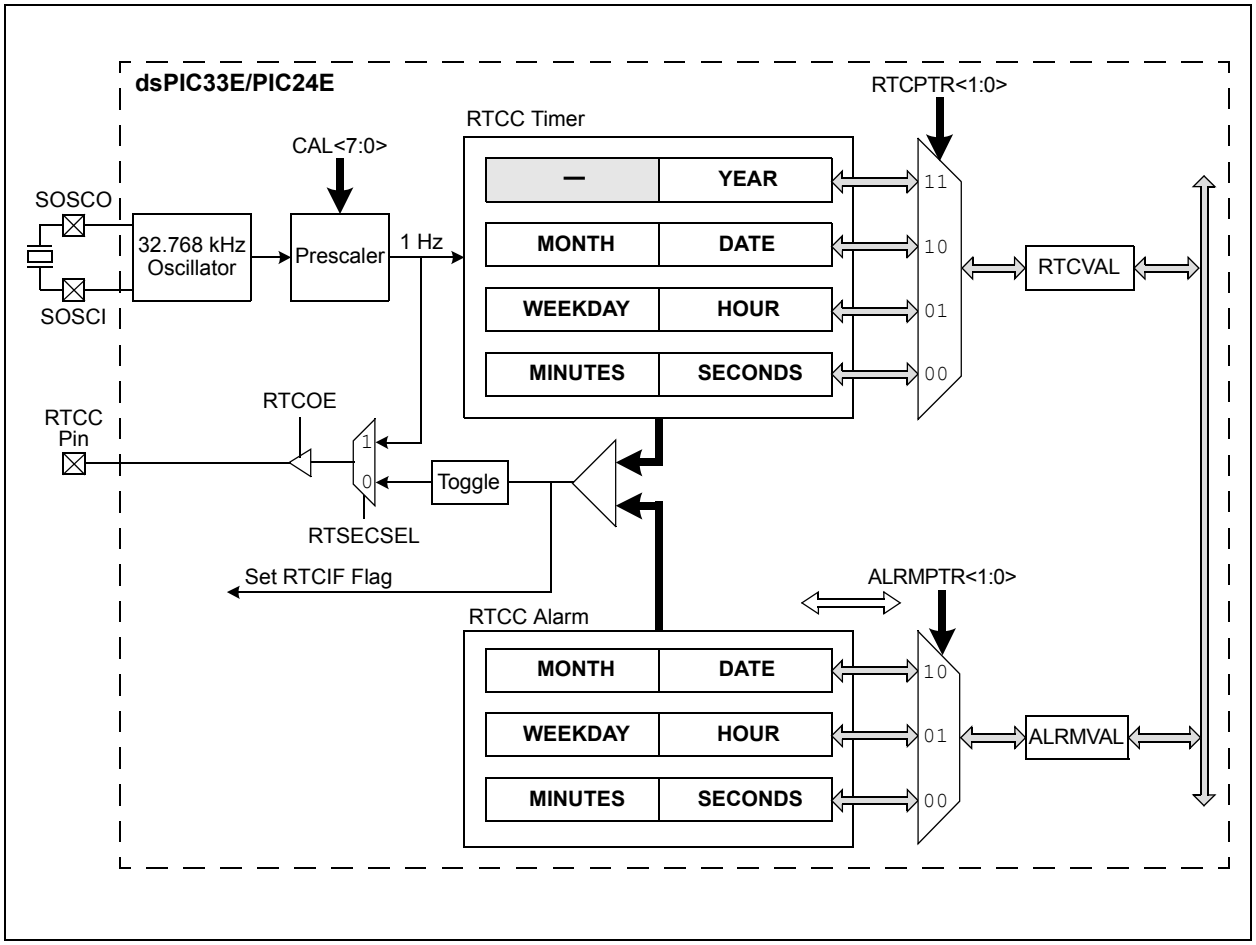


FIGURE 26-1: RTCC BLOCK DIAGRAM



26.1 Writing to the RTCC Timer

Note: To allow the RTCC module to be clocked by the secondary crystal oscillator, the Secondary Oscillator Enable (LPOSCEN) bit in the Oscillator Control (OSCCON<1>) register must be set. For further details, refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

The user application can configure the time and calendar by writing the desired seconds, minutes, hours, weekday, date, month and year to the RTCC registers. Under normal operation, writes to the RTCC Timer registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To write to the RTCC register, the RTCWREN bit (RCFGCAL<13>) must be set. Setting the RTCWREN bit allows writes to the RTCC registers. Conversely, clearing the RTCWREN bit prevents writes.

To set the RTCWREN bit, the following procedure must be executed. The RTCWREN bit can be cleared at any time:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Set the RTCWREN bit using a single-cycle instruction.

The RTCC module is enabled by setting the RTCEN bit (RCFGCAL<15>). To set or clear the RTCEN bit, the RTCWREN bit (RCFGCAL<13>) must be set.

If the entire clock (hours, minutes and seconds) needs to be corrected, it is recommended that the RTCC module should be disabled to avoid coincidental write operation when the timer increments. Therefore, it stops the clock from counting while writing to the RTCC Timer register.

26.2 RTCC Resources

Many useful resources related to RTCC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

26.2.1 KEY RESOURCES

- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

REGISTER 26-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL(1)	PMPTTL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit(1)
1 = RTCC seconds clock is selected for the RTCC pin
0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 Not used by the RTCC module.

Note 1: To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) must be set.

TABLE 32-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	VOL	**Output Low Voltage** I/O Pins: 4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO	—	—	0.4	V	IOL ≤ 10 mA, VDD = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins – OSC2 and SOSCO	—	—	0.4	V	IOL ≤ 15 mA, VDD = 3.3V
DO20	VOH	**Output High Voltage** I/O Pins: 4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins – OSC2 and SOSCO	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	**Output High Voltage** I/O Pins: 4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO	1.5(1)	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0(1)	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0(1)	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins – OSC2 and SOSCO	1.5(1)	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0(1)	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0(1)	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 32-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(2) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.7	—	2.9	V	VDD

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized.

FIGURE 32-7: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS

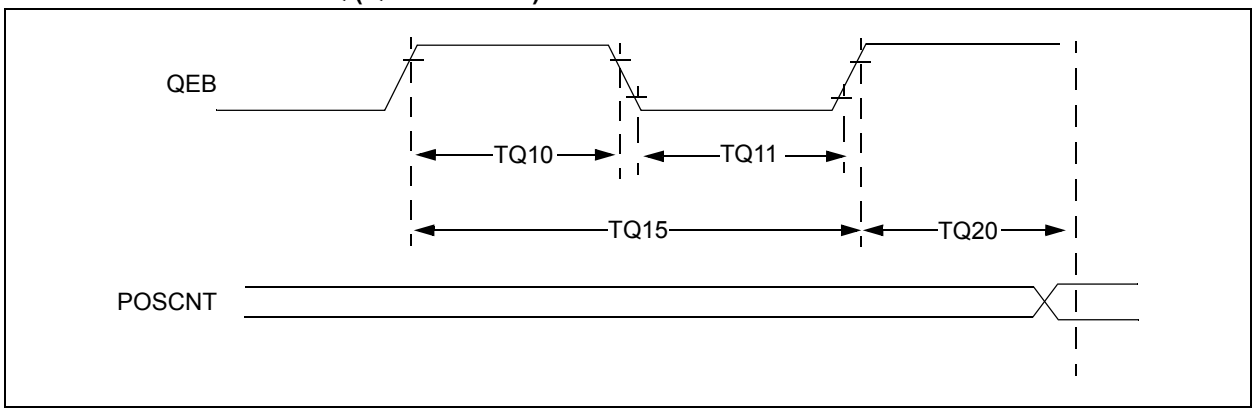
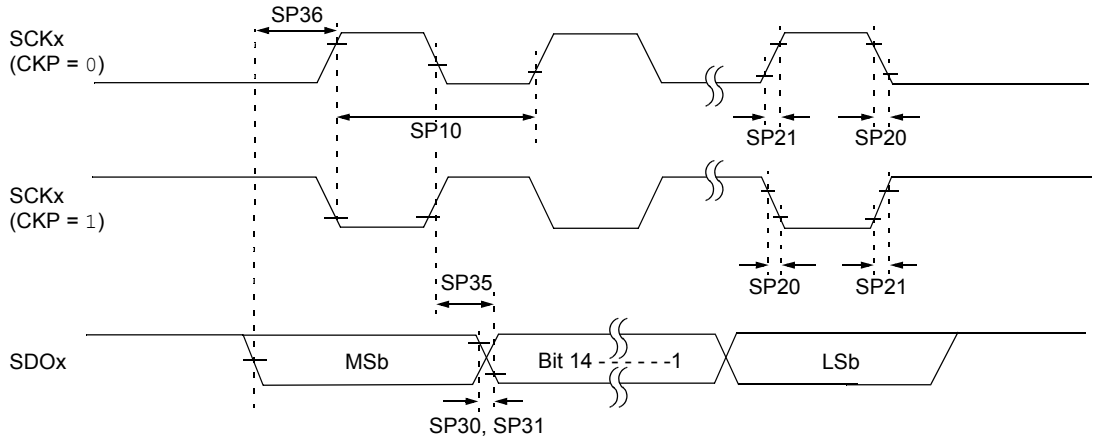


TABLE 32-26: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TQ10	TtQH	TQCK High Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with Prescaler	[Greater of (25 or TCY)/N] + 50	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TCY	—	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 32-24: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-42: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	TscP	Maximum SCKx Frequency	—	—	15	MHz	See **Note 3**
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-46: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output, High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	$\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

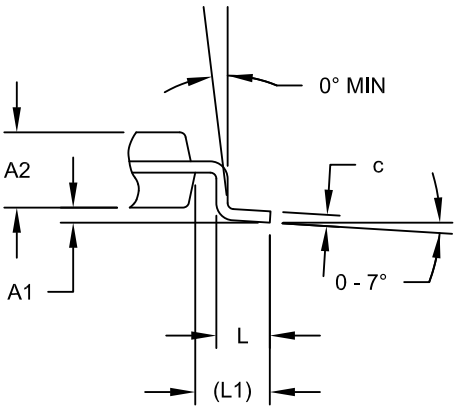
3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

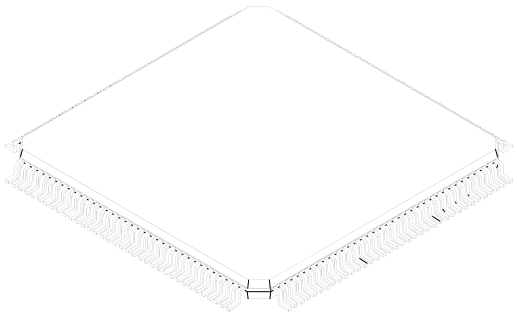
4: Assumes 50 pF load on all SPIx pins.

NOTES:

144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		144	
Lead Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Molded PackageThickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Overall Width	D		18.00 BSC	
Overall Length	E		18.00 BSC	
Molded Body Width	D1		16.00 BSC	
Molded Body Length	E1		16.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.13	-	0.23

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMU806/810/814 Devices Only)"	Reordered the bit values for the OUTFNC<1:0> bits and updated the default POR bit value to 'x' for the HOME, INDEX, QEB, and QEA bits in the QEI I/O Control Register (see Register 17-2).
Section 23.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated VREFL in the ADC1 and ADC2 Module Block Diagram (see Figure 23-1).
Section 25.0 "Comparator Module"	Added Note 1 to the Comparator I/O Operating Modes (see Figure 25-1). Removed the CLPWR bit (CMxCON<12>) (see Register 25-2).
Section 29.0 "Special Features"	Added a new first paragraph to **Section 29.1 "Configuration Bits"**
Section 30.0 "Instruction Set Summary"	The following instructions have been updated (see Table 30-2): • BRA • CALL • CPBEQ • CPBGT • CPBLT • CPBNE • GOTO • MOVPAG • MUL • RCALL • RETFIE • RETLW • RETURN • TBLRDH • TBLRDL
Section 32.0 "Electrical Characteristics"	Updated the Typical and Maximum values for DC Characteristics: Operating Current (IDD) (see Table 32-5). Updated the Typical and Maximum values for DC Characteristics: Idle Current (IIDLE) (see Table 32-6). Updated the Maximum values for DC Characteristics: Power-down Current (IPD) (see Table 32-7). Updated the Maximum values for DC Characteristics: Doze Current (IDOZE) (see Table 32-8). Updated the parameter numbers for Internal FRC Accuracy (see Table 32-19). Updated the parameter numbers and the Typical value for parameter F21b for Internal RC Accuracy (see Table 32-20). Updated the Minimum value for PM6 and the Typical and Maximum values for PM7 in Parallel Master Port Read Requirements (see Table 32-52). Added DMA Module Timing Requirements (see Table 32-54).

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