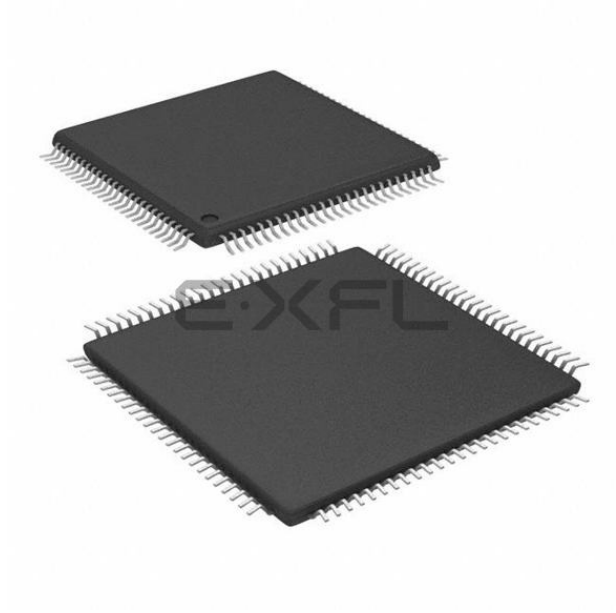
Microchip Technology - PIC24EP512GU810T-I/PT Datasheet



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Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu810t-i-pt

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CONTROLLER FAMILIES

Device	Pins	Packages	Program Flash Memory (Kbyte)(1)	RAM (Kbyte)(2)	Remappable Peripherals												RTCC	I^2C™	CRC Generator	10-Bit/12-Bit ADC(8)	USB	Parallel Master Port	I/O Pins
					16-Bit Timer(3,4)	Input Capture	Output Compare (with PWM)	Motor Control PWM (Channels)(5)	QEI	UART with IrDA®	SPI	ECAN™	External Interrupts(6)	DMA Controller (Channels)	DCI	Analog Comparators/ Inputs Per Comparator(7)							
dsPIC33EP256MU806	64	QFN, TQFP	280	28	9	16	16	8	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	1	Y	51
dsPIC33EP256MU810	100	TQFP	280	28	9	16	16	12	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
dsPIC33EP256MU814	144	TQFP, LQFP	280	28	9	16	16	14	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122
dsPIC33EP512GP806	64	QFN, TQFP	536	52	9	16	16	—	—	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	—	Y	53
dsPIC33EP512MC806	64	QFN, TQFP	536	52	9	16	16	8	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	—	Y	53
dsPIC33EP512MU810	100	TQFP	536	52	9	16	16	12	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
dsPIC33EP512MU814	144	TQFP, LQFP	536	52	9	16	16	14	2	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122
PIC24EP256GU810	100	TQFP	280	28	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
PIC24EP256GU814	144	TQFP, LQFP	280	28	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122
PIC24EP512GP806	64	QFN, TQFP	586	52	9	16	16	—	—	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 24 ch	—	Y	53
PIC24EP512GU810	100	TQFP	536	52	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	83
	121	TFBGA																					
PIC24EP512GU814	144	TQFP,LQFP	536	52	9	16	16	0	0	4	4	2	5	15	1	3/4	1	2	1	2 ADC, 32 ch	1	Y	122

Note 1: Flash size is inclusive of 24 Kbytes of auxiliary Flash. Auxiliary Flash supports simultaneous code execution and self-erase/programming. Refer to **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

2: RAM size is inclusive of 4 Kbytes of DMA RAM (DPSRAM) for all devices.

3: Up to eight of these timers can be combined into four 32-bit timers.

4: Eight out of nine timers are remappable.

5: PWM Faults and Sync signals are remappable.

6: Four out of five interrupts are remappable.

7: Comparator output is remappable.

8: The ADC2 module supports 10-bit mode only.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

● = Pins are up to 5V tolerant

dsPIC33EP256MU810
dsPIC33EP512MU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{MCLR}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 2 for full pin names.

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70359) in the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 24 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1 Registers

Devices have sixteen 16-bit working registers in the programmer's model. Each of the working registers can act as a Data, Address or Address Offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls. The working registers, W0 through W3, and selected bits from the STATUS register, have shadow registers for fast context saves and restores using a single `POP.S` or `PUSH.S` instruction.

3.2 Instruction Set

The dsPIC33EPXXXMU806/810/814 instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The PIC24EPXXX(GP/GU)810/814 instruction set has the MCU class of instructions and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear data space. On dsPIC33EPXXX(GP/MC/MU)806/810/814 devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

The upper 32 Kbytes of the data space memory map can optionally be mapped into Program Space at any 16K program word boundary. The program-to-data space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were data space. Moreover, the Base Data Space address is used in conjunction with a read or write page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to **Section 3. "Data Memory"** (DS70595) and **Section 4. "Program Memory"** (DS70613) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more details on EDS, PSV and table accesses.

On dsPIC33EPXXX(GP/MC/MU)806/810/814 devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. PIC24EPXXX(GP/GU)810/814 devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2 **SFA:** Stack Frame Active Status bit
- 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
- 0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit(1)
- 1 = Biased (conventional) rounding is enabled
- 0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit(1)
- 1 = Integer mode is enabled for DSP multiply
- 0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: This bit is always read as '0'.

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-41: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR35	06E6	—	IC14R<6:0>							—	IC13R<6:0>							0000
RPINR36	06E8	—	IC16R<6:0>							—	IC15R<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	OCFCR<6:0>							0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	SYNCI2R<6:0>							0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000
RPINR40	06F0	—	DTCMP5R<6:0>							—	DTCMP4R<6:0>							0000
RPINR41	06F2	—	—	—	—	—	—	—	—	—	DTCMP6R<6:0>							0000
RPINR42	06F4	—	FLT6R<6:0>							—	FLT5R<6:0>							0000
RPINR43	06F6	—	—	—	—	—	—	—	—	—	FLT7R<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PMD REGISTER MAP FOR dsPIC33EPXXXGP8XX AND PIC24EPXXXGP8XX DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	—	—	U3MD	—	I2C2MD	AD2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	—	—	—	0000
PMD5	0768	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	0000
PMD6	076A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPI4MD	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA13MD	DMA9MD	DMA5MD	DMA1MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA14MD	DMA10MD	DMA6MD	DMA2MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	—	DMA11MD	DMA7MD	DMA3MD	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-52: PMD REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD	PMPMD	CRCMD	—	—	—	U3MD	—	I2C2MD	AD2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	—	—	USB1MD	0000
PMD5	0768	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	0000
PMD6	076A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPI4MD	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	DMA12MD	DMA8MD	DMA4MD	DMA0MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA13MD	DMA9MD	DMA5MD	DMA1MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	DMA14MD	DMA10MD	DMA6MD	DMA2MD	—	—	—	—	0000
		—	—	—	—	—	—	—	—	—	DMA11MD	DMA7MD	DMA3MD	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6 Modulo Addressing (dsPIC33EPXXXMU806/810/814 Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y data spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

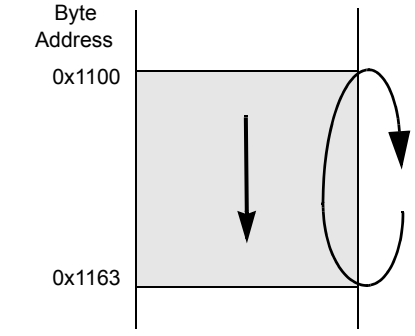
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = `1111`, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = `1111`, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '`1111`' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '`1111`' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-10: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```

REGISTER 7-1: SR: CPU STATUS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>(2)			RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)

111 = CPU Interrupt Priority Level is 7 (15, user interrupts are disabled)
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see **Register 3-1: "SR: CPU Status Register"**.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn) (CONTINUED)

Function	RPnR<5:0>	Output Name
U4TX	011101	RPn tied to UART4 Transmit
$\overline{\text{U4RTS}}$	011110	RPn tied to UART4 Ready-to-Send
SDO3	011111	RPn tied to SPI3 Data Output
SCK3	100000	RPn tied to SPI3 Clock Output
$\overline{\text{SS3}}$	100001	RPn tied to SPI3 Slave Select
SDO4	100010	RPn tied to SPI4 Data Output
SCK4	100011	RPn tied to SPI4 Clock Output
$\overline{\text{SS4}}$	100100	RPn tied to SPI4 Slave Select
OC9	100101	RPn tied to Output Compare 9 Output
OC10	100110	RPn tied to Output Compare 10 Output
OC11	100111	RPn tied to Output Compare 11 Output
OC12	101000	RPn tied to Output Compare 12 Output
OC13	101001	RPn tied to Output Compare 13 Output
OC14	101010	RPn tied to Output Compare 14 Output
OC15	101011	RPn tied to Output Compare 15 Output
OC16	101100	RPn tied to Output Compare 16 Output
SYNCO1(1)	101101	RPn tied to PWM Primary Time Base Sync Output
SYNCO2(1)	101110	RPn tied to PWM Secondary Time Base Sync Output
QEI1CCMP(1)	101111	RPn tied to QEI 1 Counter Comparator Output
QEI2CCMP(1)	110000	RPn tied to QEI 2 Counter Comparator Output
REFCLK	110001	RPn tied to Reference Clock Output

Note 1: This function is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

16.1 PWM Resources

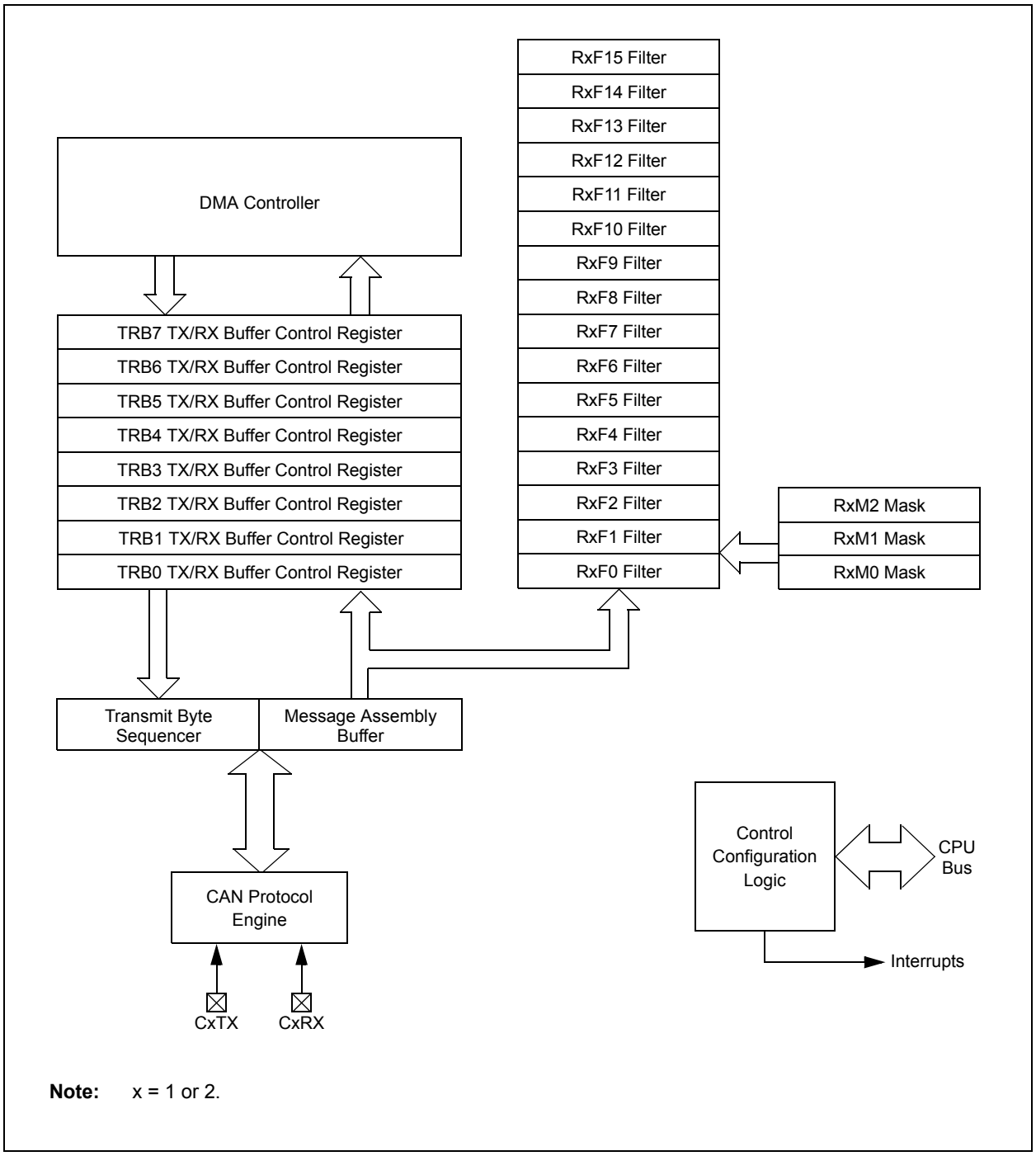
Many useful resources related to the high-speed PWM are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

16.1.1 KEY RESOURCES

- **Section 11. "High-Speed PWM"** (DS70645) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

FIGURE 21-1: ECANx MODULE BLOCK DIAGRAM



Note: x = 1 or 2.

21.2 Modes of Operation

The ECANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODE bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources related to ECAN are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

21.3.1 KEY RESOURCES

- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

REGISTER 22-20: UxEIE: USB ERROR INTERRUPT ENABLE REGISTER (DEVICE MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BTSEE	BUSACCEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **BUSACCEE:** Bus Access Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

REGISTER 22-29: UxFRML: USB FRAME NUMBER LOW REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
FRM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **FRM<7:0>:** 11-Bit Frame Number Lower 8 bits
These register bits are updated with the current frame number whenever a SOF token is received.

NOTES:

31.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

31.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

31.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

31.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

31.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

FIGURE 32-7: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS

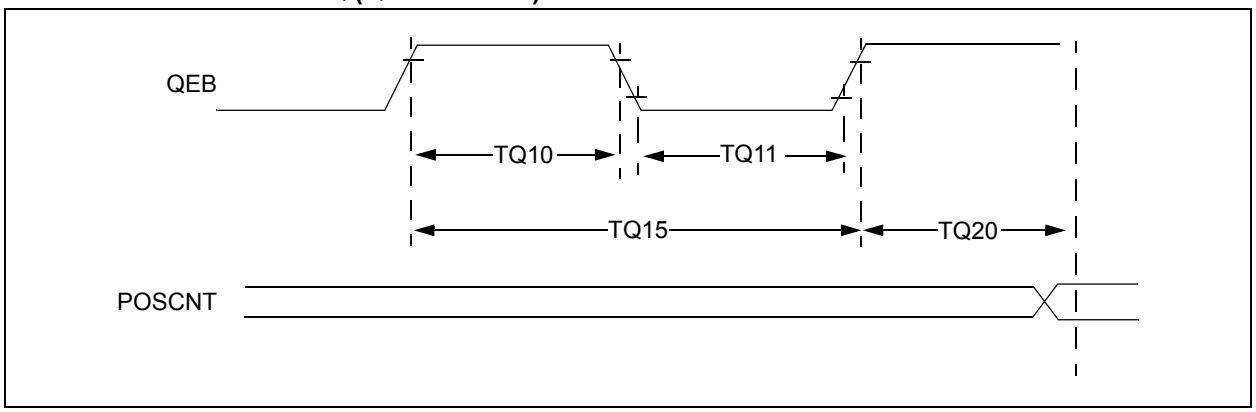


TABLE 32-26: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

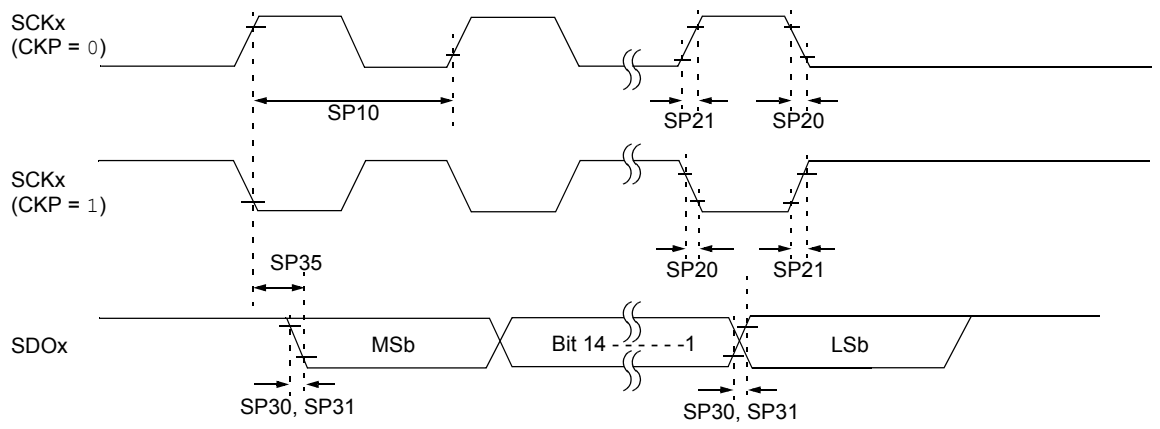
AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TQ10	TtQH	TQCK High Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with Prescaler	[Greater of (12.5 or 0.5 TCY)/N] + 25	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with Prescaler	[Greater of (25 or TCY)/N] + 50	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TCY	—	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 32-41: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 32-42	—	—	0,1	0,1	0,1
10 MHz	—	Table 32-43	—	1	0,1	1
10 MHz	—	Table 32-44	—	0	0,1	1
15 MHz	—	—	Table 32-45	1	0	0
11 MHz	—	—	Table 32-46	1	1	0
15 MHz	—	—	Table 32-47	0	1	0
11 MHz	—	—	Table 32-48	0	0	0

FIGURE 32-23: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 32-1 for load conditions.

TABLE 32-58: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 4) (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	76	—	—	ns	
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	12 TAD	—	—	
AD56	FCNV	Throughput Rate	—	—	1.1	Msps	Using sequential sampling
AD57	TSAMP	Sample Time	2 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(2)	2 TAD	—	3 TAD	—	Auto-Convert Trigger not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(2)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(2)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(2)	—	—	20	μs	See **Note 3**

Note 1: These parameters are characterized but not tested in manufacturing.

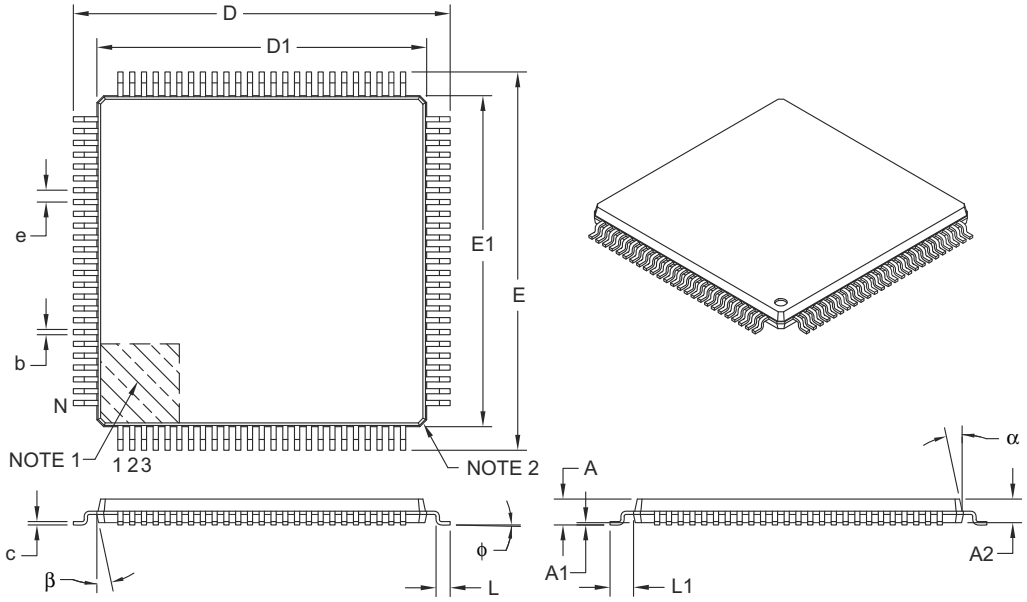
2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

3: The tDPU parameter is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.

4: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B