Microchip Technology - PIC24EP512GU814-I/PL Datasheet

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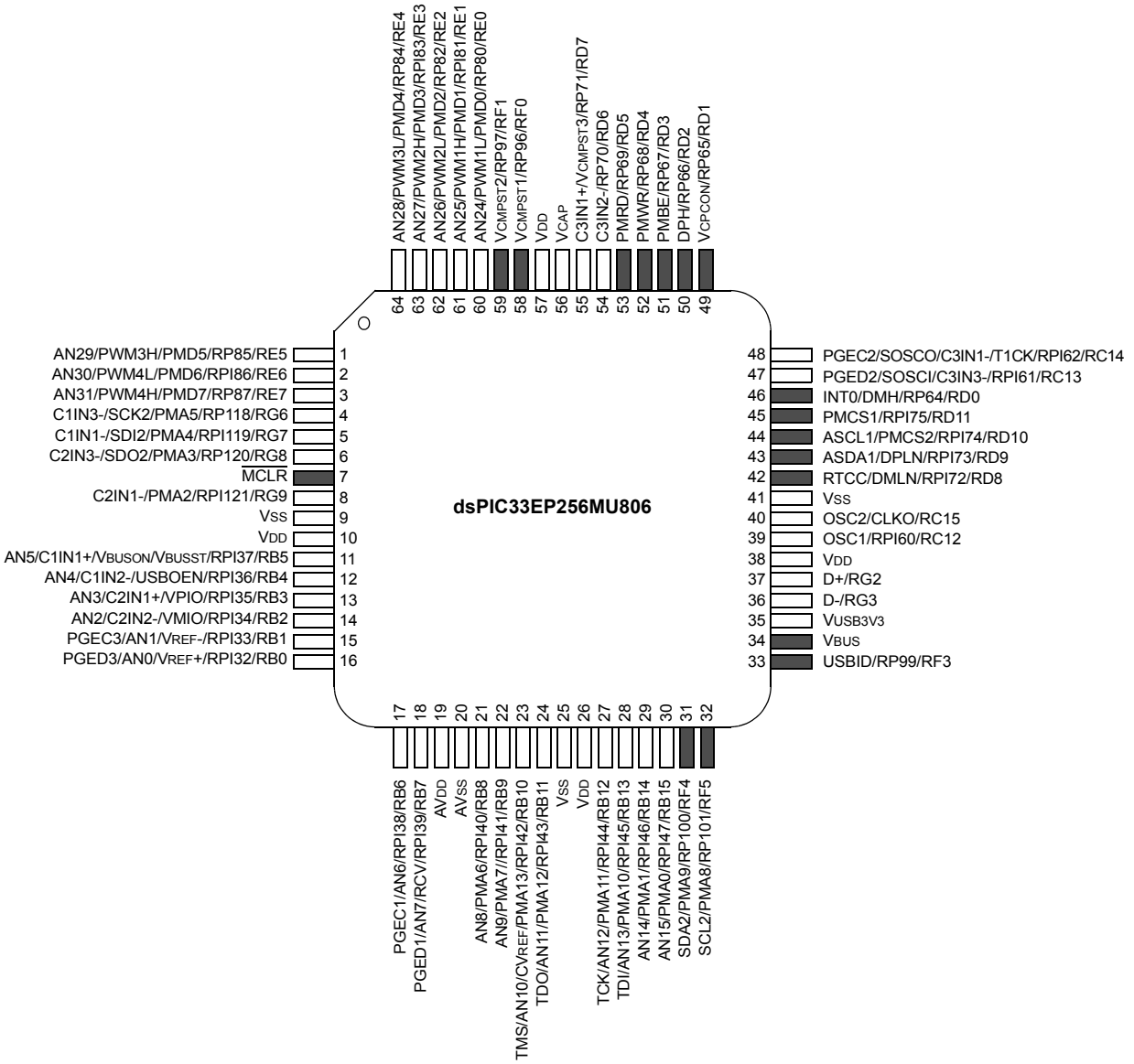
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu814-i-pl

Pin Diagrams (Continued)

64-Pin TQFP

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The availability of I^2C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

Pin Diagrams (Continued)

121-Pin TFBGA(1)

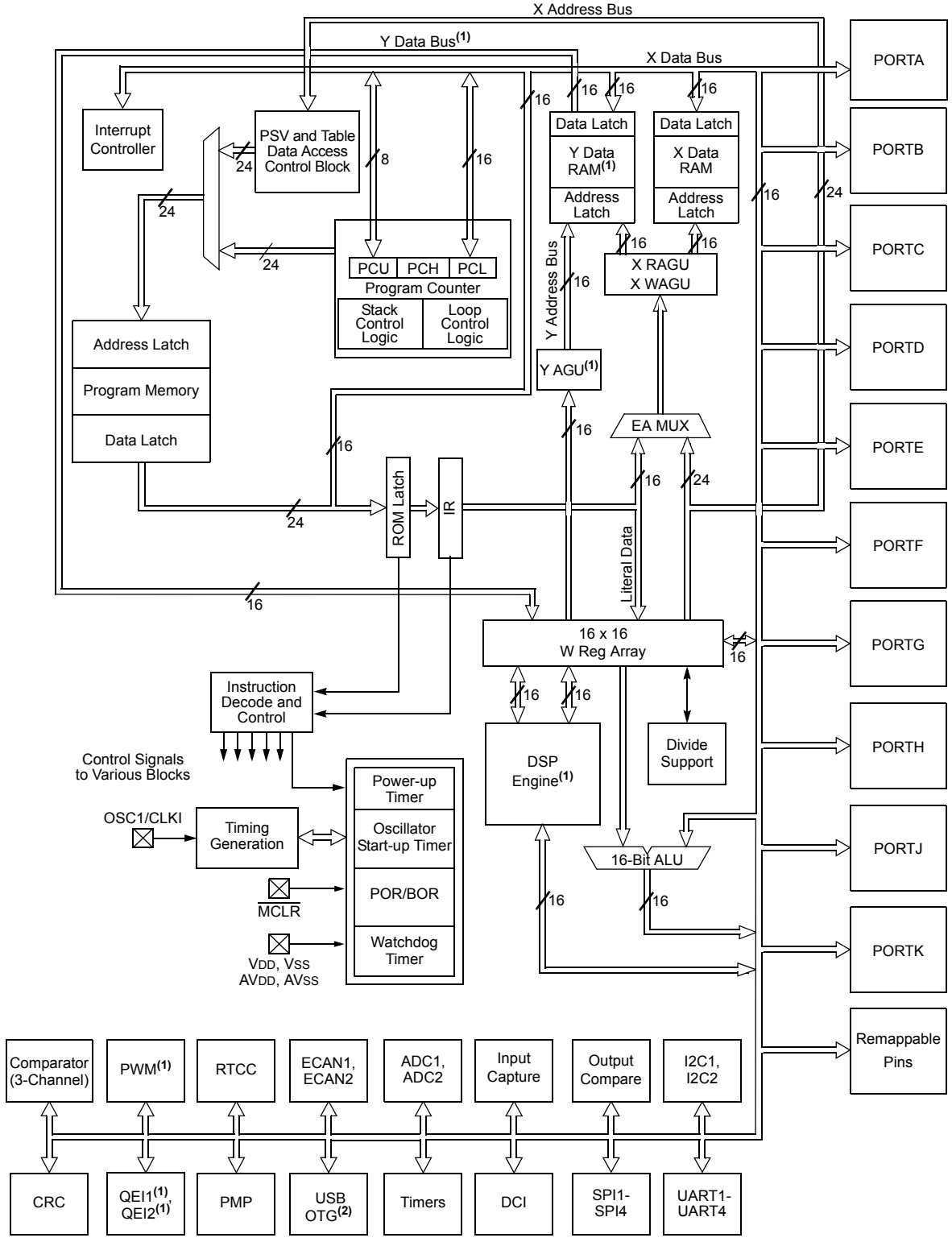
● = Pins are up to 5V tolerant

PIC24EP256GU810
PIC24EP512GU810

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	VDD	NC	RD12	RD2	RD1
B	NC	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	NC	RD7	RD4	NC	RC13	RD11
D	RC1	RE7	RE5	NC	NC	NC	RD6	RD13	RD0	NC	RD10
E	RC4	RC3	RG6	RC2	NC	RG1	NC	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	NC	NC	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	NC	VDD	VSS	VSS	NC	RA5	RA3	RA4
H	RB5	RB4	NC	NC	NC	VDD	NC	VBUS	VUSB3V3	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	NC	NC	RF8	RG3
K	RB1	RB0	RA10	RB8	NC	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Note 1: Refer to Table 3 for full pin names.

FIGURE 1-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

2: This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.

TABLE 4-18: PWM GENERATOR 6 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON6	0CC0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON6	0CC2	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON6	0CC4	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC6	0CC6	PDC6<15:0>																0000
PHASE6	0CC8	PHASE6<15:0>																0000
DTR6	0CCA	—	—	DTR6<13:0>														0000
ALTDTR6	0CCC	—	—	ALTDTR6<13:0>														0000
SDC6	0CCE	SDC6<15:0>																0000
SPHASE6	0CD0	SPHASE6<15:0>																0000
TRIG6	0CD2	TRGCMP<15:0>																0000
TRGCON6	0CD4	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>						0000
PWMCAP6	0CD8	PWMCAP6<15:0>																0000
LEBCON6	0CDA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY6	0CDC	—	—	—	—	LEB<11:0>												0000
AUXCON6	0CDE	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-19: PWM GENERATOR 7 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON7	0CE0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON7	0CE2	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON7	0CE4	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC7	0CE6	PDC7<15:0>																0000
PHASE7	0CE8	PHASE7<15:0>																0000
DTR7	0CEA	—	—	DTR7<13:0>														0000
ALTDTR7	0CEC	—	—	ALTDTR7<13:0>														0000
SDC7	0CEE	SDC7<15:0>																0000
SPHASE7	0CF0	SPHASE7<15:0>																0000
TRIG7	0CF2	TRGCMP<15:0>																0000
TRGCON7	0CF4	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>						0000
PWMCAP7	0CF8	PWMCAP7<15:0>																0000
LEBCON7	0CFA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY7	0CFC	—	—	—	—	LEB<11:0>												0000
AUXCON7	0CFE	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0400-041E	See Table 4-28																—
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM0EID	0432	EID<15:8>								EID<7:0>								xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM1EID	0436	EID<15:8>								EID<7:0>								xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM2EID	043A	EID<15:8>								EID<7:0>								xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF0EID	0442	EID<15:8>								EID<7:0>								xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx
C1RXF2SID	0448	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx
C1RXF3SID	044C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx
C1RXF4SID	0450	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx
C1RXF5SID	0454	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx
C1RXF6SID	0458	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx
C1RXF7SID	045C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx
C1RXF8SID	0460	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx
C1RXF9SID	0464	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx
C1RXF10SID	0468	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 architecture uses a 24-bit wide Program Space and a 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 architecture provides two methods by which Program Space can be accessed during operation:

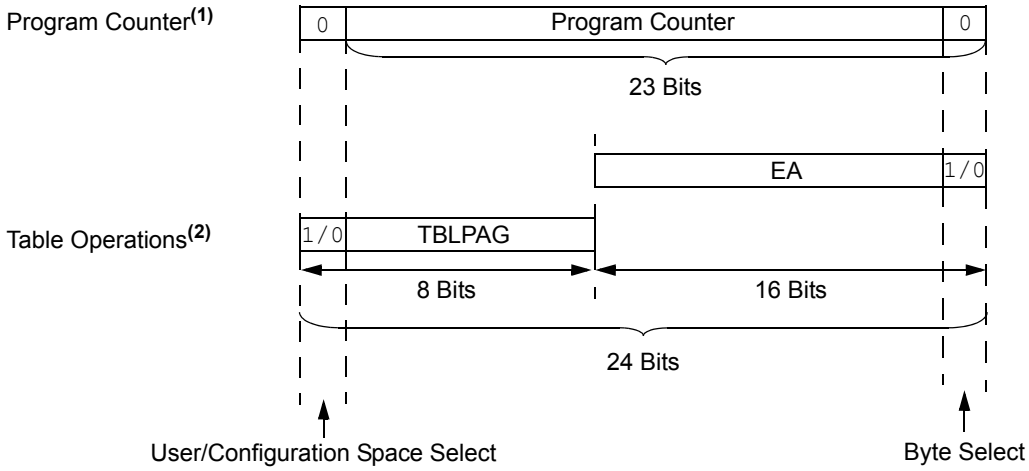
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-77: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		

FIGURE 4-12: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.

2: Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

5.2 RTSP Operation

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Flash program memory array is organized into rows of 128 instructions or 384 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (1024 instructions) at a time, and to program one row or one word at a time. Table 32-12 lists typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 3072 bytes and 384 bytes, respectively.

The program memory implements holding buffers, which are located in the write latch area, that can contain 128 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 128 `TBLWTL` and `TBLWTH` instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row. For more information on erasing and programming Flash memory, refer to **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 32-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time and Word Write Cycle Time parameters (see Table 32-12).

EQUATION 5-1: PROGRAMMING TIME

$$\frac{T}{7.37\ MHz \times (FRC\ Accuracy)\% \times (FRC\ Tuning)\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±5%. If the TUN<5:0> bits (see Register 9-4) are set to `'b111111`, the minimum row write time is equal to Equation 5-2.

EQUATION 5-2: MINIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 ms$$

The maximum row write time is equal to Equation 5-3.

EQUATION 5-3: MAXIMUM ROW WRITE TIME

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 ms$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

7.4 Interrupt Resources

Many useful resources related to Interrupts are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

7.4.1 KEY RESOURCES

- **Section 6. "Interrupts"** (DS70600) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

7.5 Interrupt Control and Status Registers

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices implement the following registers for the interrupt controller:

- INTCON1-INTCON4
- INTTREG

7.5.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS) as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and software trap enable. This register also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the USB, DMA and DO stack overflow status trap sources.

The INTCON4 register contains the software generated Hard Trap Status bit (SGHT).

7.5.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.5.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.5.4 IPCx

The IPC registers are used to set the Interrupt Priority Level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.5.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the vector number (VECNUM<7:0>) and Interrupt level bit (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.5.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **Section 2. "CPU"** (DS70359) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

11.4 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation “RPn” or “RPIn” in their full pin designation, where “RP” designates a remappable function for input or output and “RPI” designates a remappable functions for input only, and “n” is the remappable pin number.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

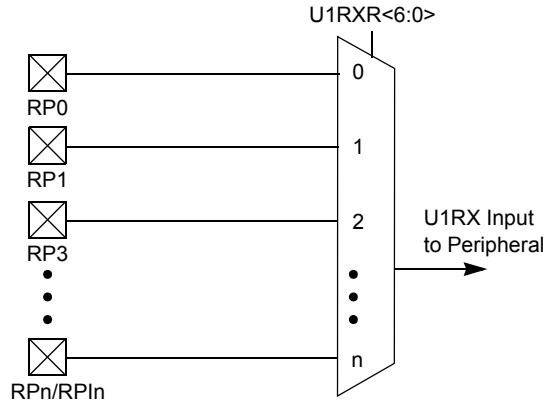
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-22). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals (see Table 11-1). Programming a given peripheral’s bit field with an appropriate 7-bit value maps the RPn/RPIn pin with the corresponding value to that peripheral (see Table 11-2). For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: U1RX REMAPPABLE INPUT



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring RPn/RPIn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to ‘1’).

REGISTER 11-12: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	OCFBR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	OCFAR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **OCFBR<6:0>:** Assign Output Compare Fault B (OCFB) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-16: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	HOME1R<6:0>(1)						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INDX1R<6:0>(1)						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME1R<6:0>:** Assign QEI1 HOME1 (HOME1) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IND1XR<6:0>:** Assign QEI1 INDEX1 (INDX1) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

Note 1: These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER (CONTINUED)

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)(3)
111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position and Index Counter/Timer Direction Select bit
1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2 **GATEN:** External Count Gate Enable bit
1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit 1-0 **CCM<1:0>:** Counter Control Mode Selection bits
11 = Internal Timer mode with optional external count is selected
10 = External clock count with optional external count is selected
01 = External clock count with external up/down direction is selected
00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

Note 1: When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM = 00, and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bit (same values as bit 15-14)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bit (same values as bit 15-14)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bit (same values as bit 15-14)

bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bit (same values as bit 15-14)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bit (same values as bit 15-14)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bit (same values as bit 15-14)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bit (same values as bit 15-14)

REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER n (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = Bit, SIDx, is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in filter
0 = Matches either standard or extended address message if filters match
(i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER n (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2 (CONTINUED)

bit 1 **BUFM:** Buffer Fill Mode Select bit

1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt

0 = Always starts filling the buffer from the Start address

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses channel input selects for Sample A on first sample and Sample B on next sample

0 = Always uses channel input selects for Sample A

REGISTER 25-3: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB<3:0>				SELSRCA<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Typ.(2)**	**Max.**	**Units**	**Conditions**		
Power-Down Current (IPD)(1)						
DC60d	50	100	µA	-40°C	3.3V	Base Power-Down Current(1,4)
DC60a	60	200	µA	+25°C		
DC60b	250	500	µA	+85°C		
DC60c	1600	3000	µA	+125°C		
DC61d	8	10	µA	-40°C	3.3V	Watchdog Timer Current: ΔIWDT(3)
DC61a	10	15	µA	+25°C		
DC61b	12	20	µA	+85°C		
DC61c	13	25	µA	+125°C		

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled, all peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- RTCC is disabled
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to stand-by while the device is in Sleep mode)
- JTAG is disabled

2: Data in the "Typ" column is at 3.3V, +25ºC unless otherwise stated.

3: The Watchdog Timer current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.

4: These currents are measured on the device containing the most memory in this family.

TABLE 32-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Symbol**	**Characteristic(3)**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25		µs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	See **Note 2**

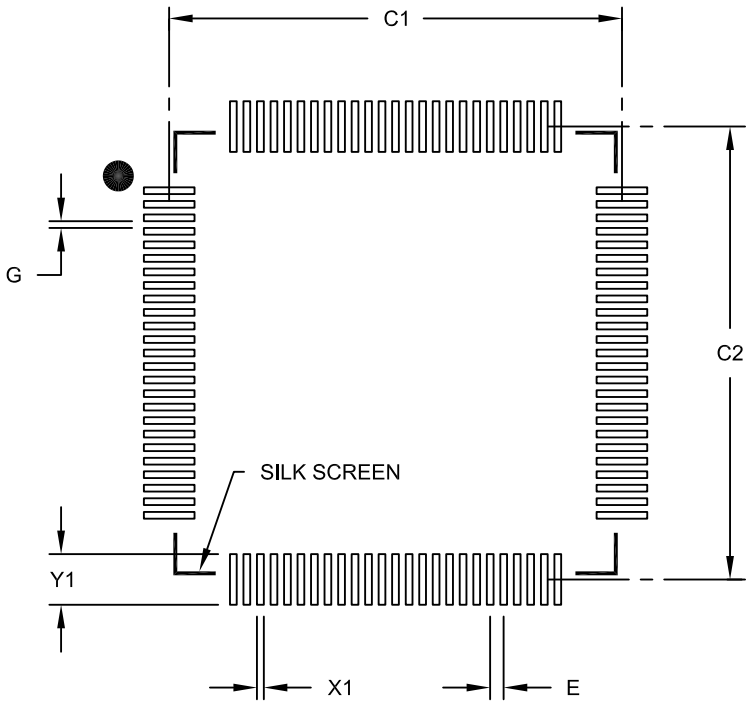
Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: The typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 7.0 "Interrupt Controller"	Added the VAR bit (CORCON<15>) to the Core Control Register (see Register 7-2) Changed the default POR value for the GIE bit (INTCON2<15) to R/W-1 (see Register 7-4). Changed the VECNUM<7:0> = 11111111 pending interrupt vector number to 263 in the Interrupt Control and Status Register (see Register 7-7).
Section 8.0 "Direct Memory Access (DMA)"	Updated **Section 8.1 "DMAC Registers"**. Updated DMA Controller in Figure 8-1. Added Note 1 to the DMA Channel x Peripheral Address Register (see Register 8-7). Added Note 1 and Note 2 to the DMA Channel x Transfer Count Register (see Register 8-8). Updated all RQCOLx bit definitions, changing Peripheral Write to Transfer Request in the DMA Request Collision Status Register (see Register 8-12).
Section 9.0 "Oscillator Configuration"	Added the Reference Oscillator Control Register (see Register 9-7). Added Note 3 and 4 to the CLKDIV Register (see Register 9-2)
Section 10.0 "Power-Saving Features"	Added the DCIMD and C2MD bits to the Peripheral Module Disable Control Register 1 (see Register 10-1) Added the IC6MD, IC5MD, IC4MD, IC3MD, OC8MD, OC7MD, OC6MD, and OC5MD bits to the Peripheral Module Disable Control Register 2 (see Register 10-2) Added the T9MD, T8MD, T7MD, and T6MD bits and removed the DSC1MD bit in the Peripheral Module Disable Control Register 3 (see Register 10-3). Added the REFOMD bit (PMD4<3>) to the Peripheral Module Disable Control Register 4 (see Register 10-4).
Section 11.0 "I/O Ports"	Updated the first paragraph of **Section 11.2 "Configuring Analog and Digital Port Pins"**. Updated the PWM Fault, Dead-Time Compensation, and Synch Input register numbers of the Selectable Input Sources (see Table 11-2). Removed RPINR22 register. Bit names and definitions were modified in the following registers: • Peripheral Pin Select Input Register 37 (see Register 11-37) • Peripheral Pin Select Input Register 38 (see Register 11-38) • Peripheral Pin Select Input Register 39 (see Register 11-39) • Peripheral Pin Select Input Register 40 (see Register 11-40) • Peripheral Pin Select Input Register 41 (see Register 11-41) • Peripheral Pin Select Input Register 42 (see Register 11-42) • Peripheral Pin Select Input Register 43 (see Register 11-43)
Section 12.0 "Timer1"	Added Note in Register 12-1.
Section 14.0 "Input Capture"	Added Note 1 to the Input Capture Block Diagram (see Figure 14-1).
Section 15.0 "Output Compare"	Added Note 1 to the Output Compare Module Block Diagram (see Figure 15-1). Added Note 2 to the Output Compare x Control Register 2 (see Register 15-2).
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMU806/810/814 Devices Only)"	Added Comparator bit values for the CLSRC<4:0> and FLTSRC<4:0> bits in the PWM Fault Current-Limit Control Register (see Register 16-21).