Microchip Technology - PIC24EP512GU814T-I/PH Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu814t-i-ph

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70359) in the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 24 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1 Registers

Devices have sixteen 16-bit working registers in the programmer's model. Each of the working registers can act as a Data, Address or Address Offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls. The working registers, W0 through W3, and selected bits from the STATUS register, have shadow registers for fast context saves and restores using a single `POP.S` or `PUSH.S` instruction.

3.2 Instruction Set

The dsPIC33EPXXXMU806/810/814 instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The PIC24EPXXX(GP/GU)810/814 instruction set has the MCU class of instructions and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear data space. On dsPIC33EPXXX(GP/MC/MU)806/810/814 devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

The upper 32 Kbytes of the data space memory map can optionally be mapped into Program Space at any 16K program word boundary. The program-to-data space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were data space. Moreover, the Base Data Space address is used in conjunction with a read or write page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to **Section 3. "Data Memory"** (DS70595) and **Section 4. "Program Memory"** (DS70613) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more details on EDS, PSV and table accesses.

On dsPIC33EPXXX(GP/MC/MU)806/810/814 devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. PIC24EPXXX(GP/GU)810/814 devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2 **SFA:** Stack Frame Active Status bit
- 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
- 0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit(1)
- 1 = Biased (conventional) rounding is enabled
- 0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit(1)
- 1 = Integer mode is enabled for DSP multiply
- 0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

2: This bit is always read as '0'.

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	C2TXIP<2:0>			—	C1TXIP<2:0>			—	DMA7IP<2:0>			—	DMA6IP<2:0>			4444
IPC18	0864	—	QEI2IP<2:0>			—	—	—	—	—	PSESMIP<2:0>			—	—	—	—	4040
IPC20	0868	—	U3TXIP<2:0>			—	U3RXIP<2:0>			—	U3EIP<2:0>			—	—	—	—	4440
IPC21	086A	—	U4EIP<2:0>			—	USB1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC22	086C	—	SPI3IP<2:0>			—	SPI3EIP<2:0>			—	U4TXIP<2:0>			—	U4RXIP<2:0>			4444
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	IC9IP<2:0>			—	OC9IP<2:0>			4444
IPC24	0870	—	PWM6IP<2:0>			—	PWM5IP<2:0>			—	PWM4IP<2:0>			—	PWM3IP<2:0>			4444
IPC25	0872	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM7IP<2:0>			0004
IPC29	087A	—	DMA9IP<2:0>			—	DMA8IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC30	087C	—	SPI4IP<2:0>			—	SPI4EIP<2:0>			—	DMA11IP<2:0>			—	DMA10IP<2:0>			4444
IPC31	087E	—	IC11IP<2:0>			—	OC11IP<2:0>			—	IC10IP<2:0>			—	OC10IP<2:0>			4444
IPC32	0880	—	DMA13IP<2:0>			—	DMA12IP<2:0>			—	IC12IP<2:0>			—	OC12IP<2:0>			4444
IPC33	0882	—	IC13IP<2:0>			—	OC13IP<2:0>			—	—	—	—	—	DMA14IP<2:0>			4404
IPC34	0884	—	IC15IP<2:0>			—	OC15IP<2:0>			—	IC14IP<2:0>			—	OC14IP<2:0>			4444
IPC35	0886	—	—	—	—	—	ICDIP<2:0>			—	IC16IP<2:0>			—	OC16IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	UAE	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PTPER<15:0>																FFF8
SEVTCMP	0C06	SEVTCMP<15:0>																0000
MDC	0C0A	MDC<15:0>																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC<2:0>			SEVTPS<3:0>				0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	STPER<15:0>																FFF8
SSEVTCMP	0C14	SSEVTCMP<15:0>																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:0>										0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
FCLCON1	0C24	IFLTMOD	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		0000
PDC1	0C26	PDC1<15:0>																0000
PHASE1	0C28	PHASE1<15:0>																0000
DTR1	0C2A	—	—	DTR1<13:0>														0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>														0000
SDC1	0C2E	SDC1<15:0>																0000
SPHASE1	0C30	SPHASE1<15:0>																0000
TRIG1	0C32	TRGCMP<15:0>																0000
TRGCON1	0C34	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>						0000
PWMCAP1	0C38	PWMCAP1<15:0>																0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB<11:0>												0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 1 (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2RXF11EID	056E	EID<15:8>								EID<7:0>								xxxx
C2RXF12SID	0570	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF12EID	0572	EID<15:8>								EID<7:0>								xxxx
C2RXF13SID	0574	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF13EID	0576	EID<15:8>								EID<7:0>								xxxx
C2RXF14SID	0578	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF14EID	057A	EID<15:8>								EID<7:0>								xxxx
C2RXF15SID	057C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C2RXF15EID	057E	EID<15:8>								EID<7:0>								xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR35	06E6	—	IC14R<6:0>							—	IC13R<6:0>							0000
RPINR36	06E8	—	IC16R<6:0>							—	IC15R<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	OCFCR<6:0>							0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	SYNCI2R<6:0>							0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000
RPINR40	06F0	—	DTCMP5R<6:0>							—	DTCMP4R<6:0>							0000
RPINR41	06F2	—	DTCMP7R<6:0>							—	DTCMP6R<6:0>							0000
RPINR42	06F4	—	FLT6R<6:0>							—	FLT5R<6:0>							0000
RPINR43	06F6	—	—	—	—	—	—	—	—	—	FLT7R<6:0>							0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR(1)	OVBERR(1)	COVAERR(1)	COVBERR(1)	OVATE(1)	OVBTE(1)	COVTE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR(1)	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit(1)
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit(1)
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMAC Trap Flag bit
1 = DMAC trap has occurred
0 = DMAC trap has not occurred

Note 1: This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

Input Name(1)	Function Name	Register	Configuration Bits
DCI Data Input	CSDI	RPINR24	CSDIR<6:0>
DCI Clock Input	CSCKIN	RPINR24	CSCKR<6:0>
DCI FSYNC Input	COFSIN	RPINR25	COFSR<6:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	$\overline{\text{U4CTS}}$	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	$\overline{\text{SS3}}$	RPINR30	SS3R<6:0>
SPI4 Data Input	SDI4	RPINR31	SDI4R<6:0>
SPI4 Clock Input	SCK4	RPINR31	SCK4R<6:0>
SPI4 Slave Select	$\overline{\text{SS4}}$	RPINR32	SS4R<6:0>
Input Capture 9	IC9	RPINR33	IC9R<6:0>
Input Capture 10	IC10	RPINR33	IC10R<6:0>
Input Capture 11	IC11	RPINR34	IC11R<6:0>
Input Capture 12	IC12	RPINR34	IC12R<6:0>
Input Capture 13	IC13	RPINR35	IC13R<6:0>
Input Capture 14	IC14	RPINR35	IC14R<6:0>
Input Capture 15	IC15	RPINR36	IC15R<6:0>
Input Capture 16	IC16	RPINR36	IC16R<6:0>
Output Compare Fault C	OCFC	RPINR37	OCFCR<6:0>
PWM Fault 5(2)	FLT5	RPINR42	FLT5R<6:0>
PWM Fault 6(2)	FLT6	RPINR42	FLT6R<6:0>
PWM Fault 7(2)	FLT7	RPINR43	FLT7R<6:0>
PWM Dead-Time Compensation 1(2)	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2(2)	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3(2)	DTCMP3	RPINR39	DTCMP3R<6:0>
PWM Dead-Time Compensation 4(2)	DTCMP4	RPINR40	DTCMP4R<6:0>
PWM Dead-Time Compensation 5(2)	DTCMP5	RPINR40	DTCMP5R<6:0>
PWM Dead-Time Compensation 6(2)	DTCMP6	RPINR41	DTCMP6R<6:0>
PWM Dead-Time Compensation 7(2)	DTCMP7	RPINR41	DTCMP7R<6:0>
PWM Synch Input 1(2)	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Synch Input 2(2)	SYNCI2	RPINR38	SYNCI2R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 13-2: TyCON: (T3CON, T5CON, T7CON OR T9CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS<1:0>(1)		—	—	TCS(1,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock from TyCK pin (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. Refer to the **"Pin Diagrams"** section for the available pins.

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32
bit 15							bit 8

R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG(2)	TRIGSTAT(3)	—	SYNCSEL<4:0>(4)				
bit 7							bit 0

Legend:		
R = Readable bit	HS = Set by Hardware	'0' = Bit is cleared
-n = Value at POR	W = Writable bit	U = Unimplemented bit, read as '0'

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC32:** 32-Bit Timer Mode Select bit (Cascade mode)
- 1 = ODD IC and EVEN IC form a single 32-bit input capture module(1)
- 0 = Cascade module operation is disabled

bit 7 **ICTRIG:** Trigger Operation Select bit(2)
- 1 = Input source is used to trigger the input capture timer (Trigger mode)
- 0 = Input source is used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit(3)
- 1 = ICxTMR has been triggered and is running
- 0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.

4: Do not use the ICx module as its own Sync or Trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN(1)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
- 0 = IrDA encoded, UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin controlled by port

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

NOTES:

TABLE 32-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
	Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)						
F20a	FRC	-2	—	+2	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-5	—	+5	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 32-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
	LPRC @ 32.768 kHz(1)						
F21a	LPRC	-20	±6	+20	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F21b	LPRC	-50	—	+50	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 32-14: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)

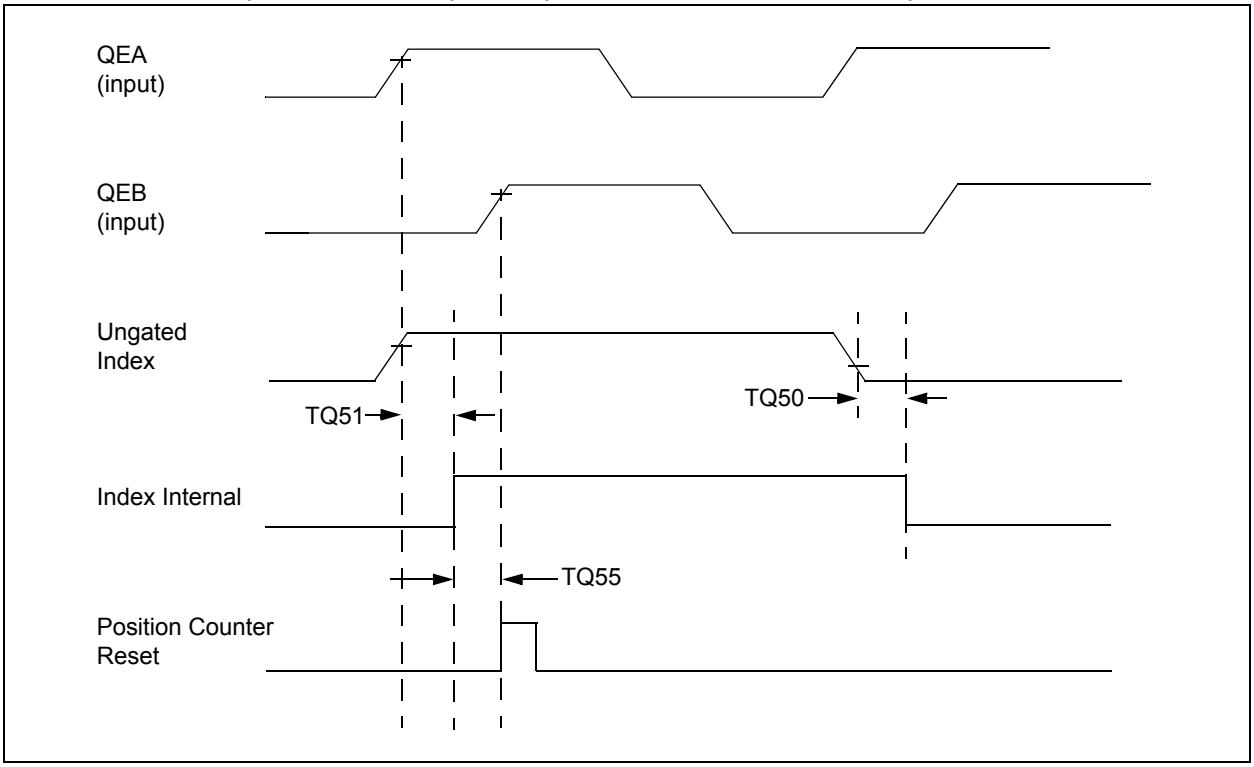


TABLE 32-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXX(MC/MU)MU806/810/814 DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Max.**	**Units**	**Conditions**
TQ50	TqIL	Filter Time to Recognize Low with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ51	TqiH	Filter Time to Recognize High with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

TABLE 32-47: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output, High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-48: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscP	Maximum SCKx Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output, High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

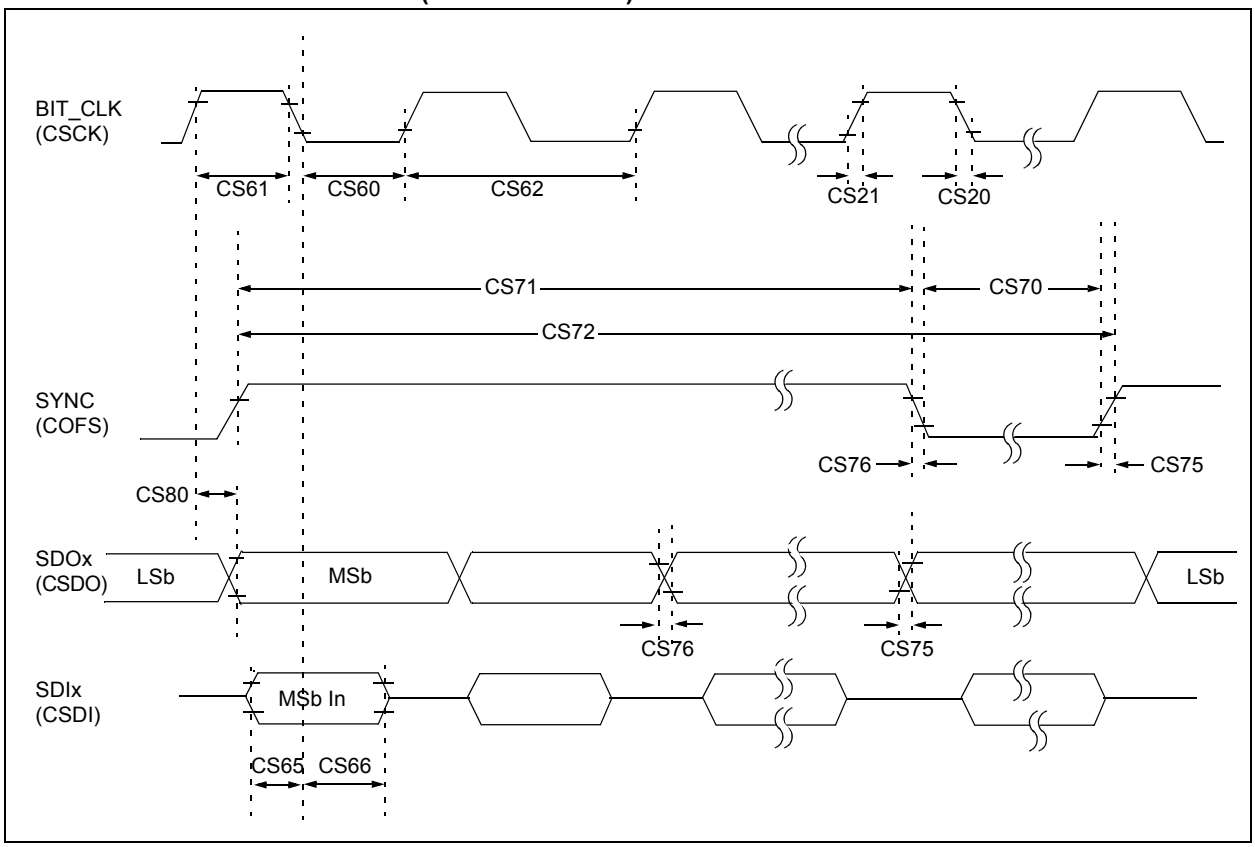
Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

FIGURE 32-41: DCI MODULE (AC-LINK MODE) TIMING CHARACTERISTICS



33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 33-1: VOH – 4x DRIVER PINS @ +85ºC

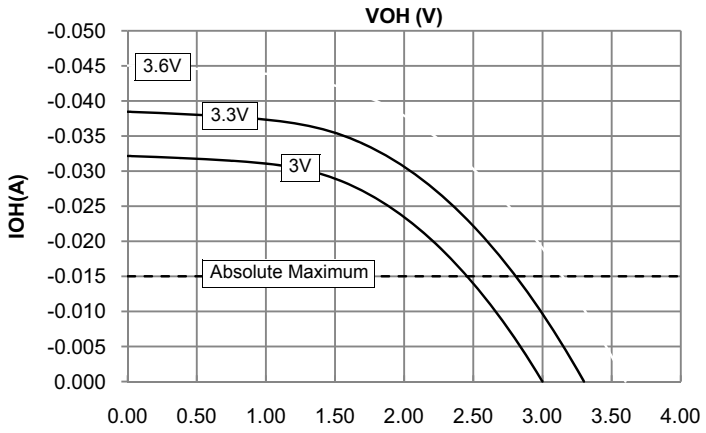


FIGURE 33-2: VOH – 8x DRIVER PINS @ +85ºC

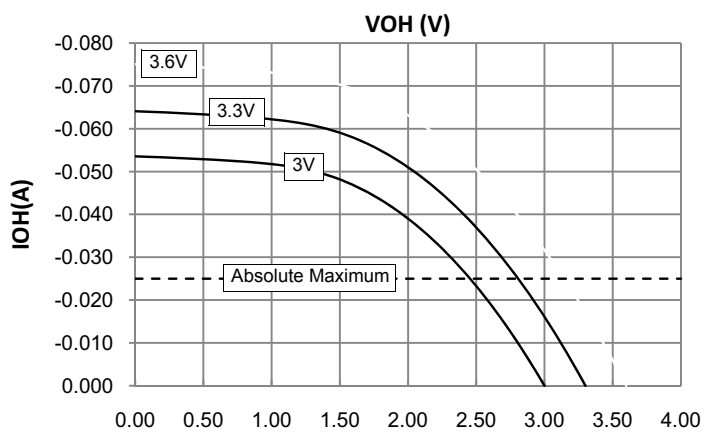


FIGURE 33-3: VOL – 4x DRIVER PINS @ +85ºC

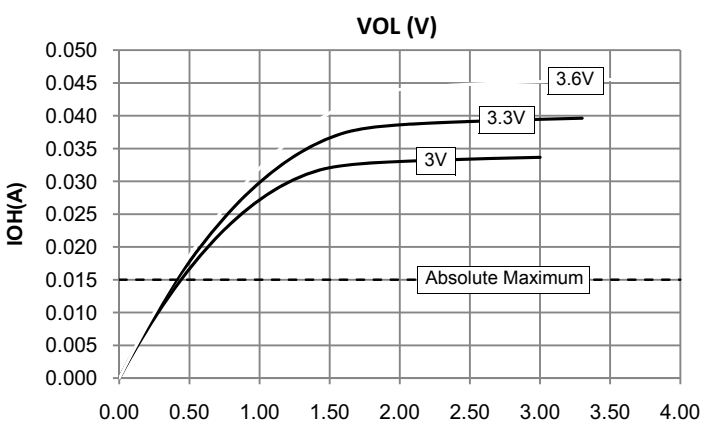
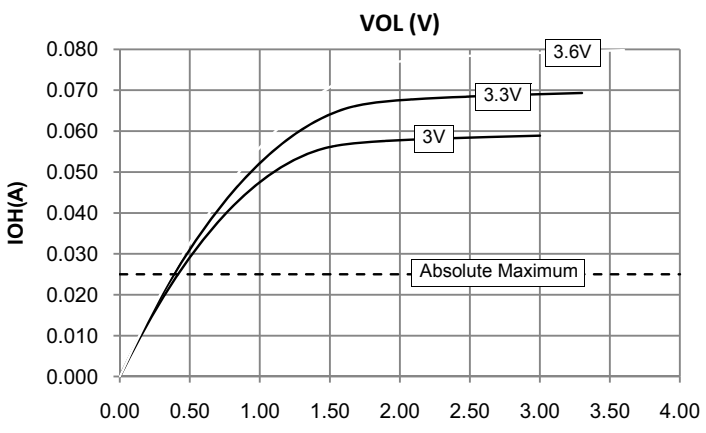
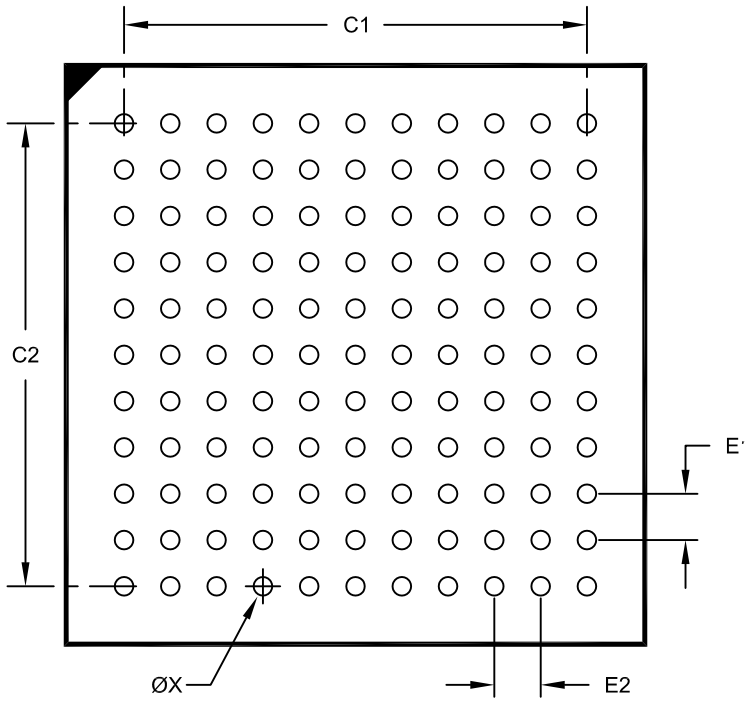


FIGURE 33-4: VOL – 8x DRIVER PINS @ +85ºC



121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E1		0.80 BSC	
Contact Pitch	E2		0.80 BSC	
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D