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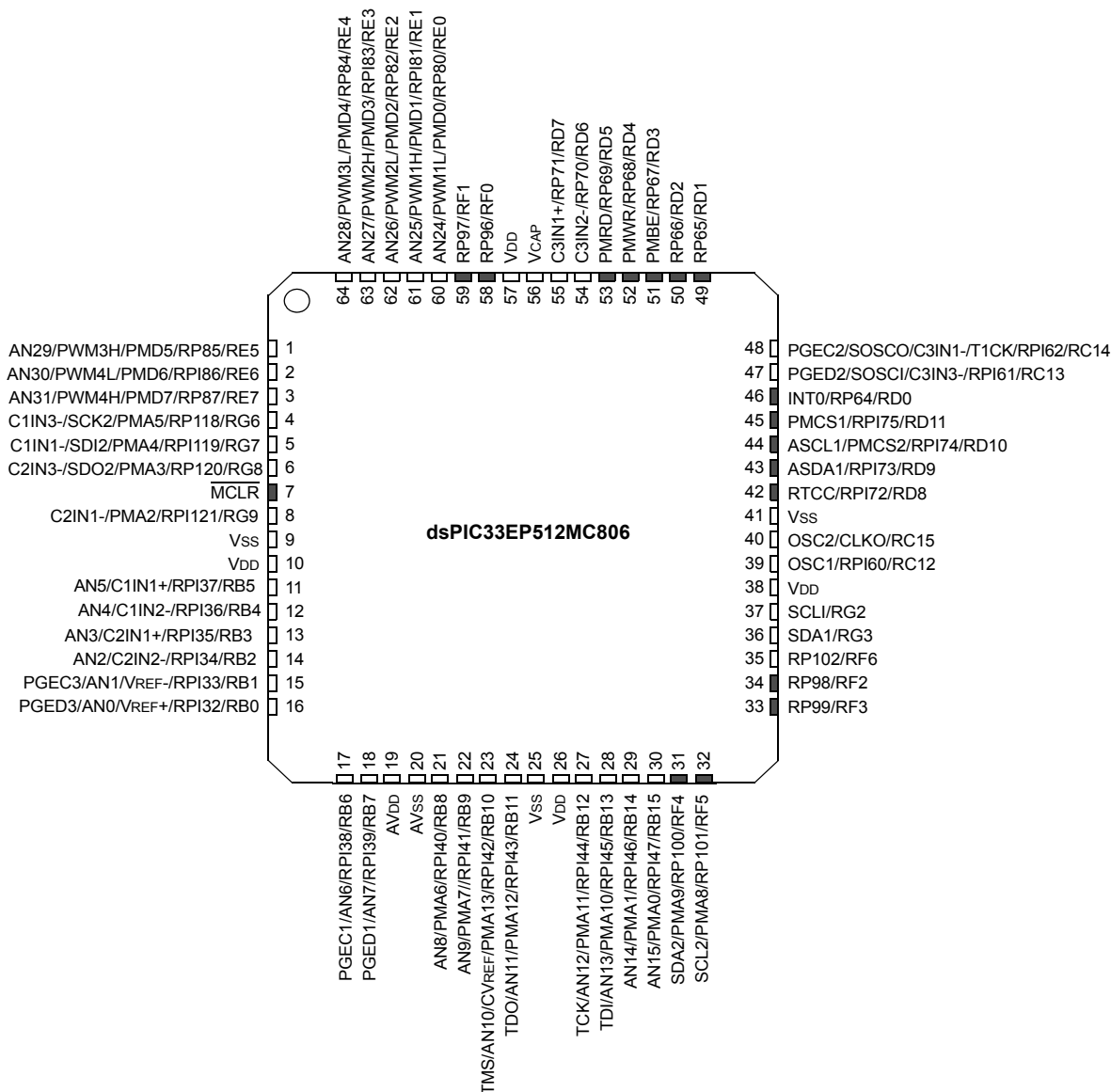
Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	122
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gu814t-i-pl

Pin Diagrams

64-Pin QFN

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select”** for available peripherals and for information on limitations.
- 2:** Every I/O port pin (RAX-RGX) can be used as change notification (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- 3:** The availability of I²C™ interfaces varies by device. Selection (SDAX/SCLx or ASDAX/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 “Special Features”** for more information.

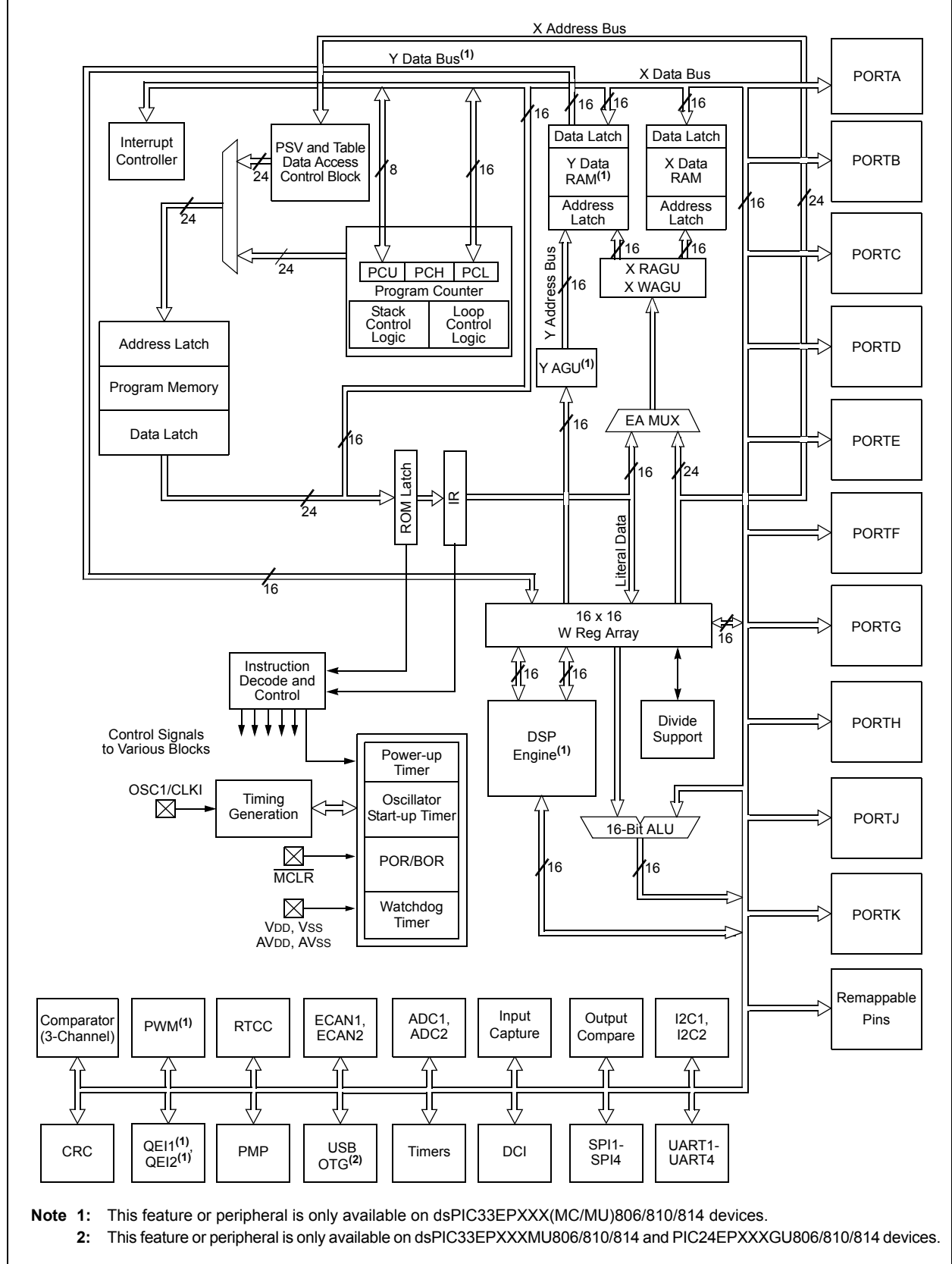


TABLE 4-28: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	CANCKS	REQOP<2:0>			OPMODE<2:0>			—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C1VEC	0404	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
C1FCTRL	0406	DMABS<2:0>			—	—	—	—	—	—	—	—	FSA<4:0>					0000
C1FIFO	0408	—	—	FBP<5:0>						—	—	FNRB<5:0>						0000
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT<7:0>								RERRCNT<7:0>								0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW<1:0>		BRP<5:0>						0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH<2:0>			SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>		F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>		0000
C1FMSKSEL2	041A	F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>		F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-29: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
—	0400-041E	See Table 4-28																—
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI<1:0>		TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI<1:0>		0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI<1:0>		TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI<1:0>		0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI<1:0>		TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI<1:0>		0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI<1:0>		TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI<1:0>		xxxx
C1RXD	0440	Received Data Word																xxxx
C1TXD	0442	Transmit Data Word																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-1: NVMCON: NON-VOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
—	—	—	—	NVMOP<3:0> ^(3,4)			
bit 7				bit 0			

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **WR:** Write Control bit⁽¹⁾
1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once operation is complete
0 = Program or erase operation is complete and inactive
- bit 14 **WREN:** Write Enable bit⁽¹⁾
1 = Enables Flash program/erase operations
0 = Inhibits Flash program/erase operations
- bit 13 **WRERR:** Write Sequence Error Flag bit⁽¹⁾
1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
0 = The program or erase operation completed normally
- bit 12 **NVMSIDL:** NVM Stop-in-Idle Control bit⁽²⁾
1 = Flash voltage regulator goes into Stand-by mode during Idle mode
0 = Flash voltage regulator is active during Idle mode
- bit 11-4 **Unimplemented:** Read as '0'
- bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits^(1,3,4)
1111 = Reserved
1110 = Reserved
1101 = Bulk erase primary program Flash memory
1100 = Reserved
1011 = Reserved
1010 = Bulk erase auxiliary program Flash memory
0011 = Memory page erase operation
0010 = Memory row program operation
0001 = Memory word program operation⁽⁵⁾
0000 = Program a single Configuration register byte

- Note 1:** These bits can only be reset on a POR.
- 2:** If this bit is set, upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.
- 3:** All other combinations of NVMOP<3:0> are unimplemented.
- 4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
- 5:** Two adjacent words are programmed during execution of this operation.

10.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

**REGISTER 11-15: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14
(dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEB1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEA1R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB1R<6:0>:** Assign B (QEB) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R<6:0>:** Assign A (QEA) to the Corresponding RPn/RPIn Pin bits
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

**REGISTER 11-17: RPINR16: PERIPHERAL PIN SELECT INPUT REGISTER 16
(dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEB2R<6:0> ⁽¹⁾						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEA2R<6:0> ⁽¹⁾						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB2R<6:0>:** Assign B (QE12) to the Corresponding RPn/RPIn Pin bits⁽¹⁾
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA2R<6:0>:** Assign A (QE12) to the Corresponding RPn/RPIn Pin bits⁽¹⁾
(see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

Note 1: These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

REGISTER 11-30: RPINR30: PERIPHERAL PIN SELECT INPUT REGISTER 30

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS3R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7

bit 6-0

Unimplemented: Read as '0'

SS3R<6:0>: Assign SPI3 Slave Select Input ($\overline{SS3}$) to the Corresponding RPN/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-38: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SYNCI2R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14-8 **DTCMP1R<6:0>:** Assign PWM Dead-Time Compensation Input 1 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'bit 6-0 **SYNCI2R<6:0>:** Assign PWM Synchronization Input 2 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXX(MC/MU)8XX DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. “High-Speed PWM”** (DS70645) of the “*dsPIC33E/PIC24E Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(MC/MU)806/810/814 devices support a dedicated Pulse-Width Modulation (PWM) module with up to 14 outputs.

The high-speed PWM module consists of the following major features:

- Two master time base modules with Special Event Triggers
- PWM module input clock prescaler
- Two synchronization inputs
- Two synchronization outputs
- Up to seven PWM generators
- Two PWM outputs per generator (PWMxH and PWMxL)
- Individual period, duty cycle and phase shift for each PWM output
- Period, duty cycle, phase shift and dead-time resolution of 8.32 ns
- Immediate update mode for PWM period, duty cycle and phase shift
- Independent Fault and current-limited inputs for each PWM
- Cycle-by-Cycle and Latched Fault modes
- PWM time-base capture upon current limit
- Seven Fault inputs and three comparator outputs available for Faults and current limits
- Programmable ADC trigger with interrupt for each PWM pair

- Complementary PWM outputs
- Push-Pull PWM outputs
- Redundant PWM outputs
- Edge-Aligned PWM mode
- Center-Aligned PWM mode
- Variable Phase PWM mode
- Multi-Phase PWM mode
- Fixed Off Time PWM mode
- Current-Limit PWM mode
- Current Reset PWM mode
- PWMxH and PWMxL output override control
- PWMxH and PWMxL output pin swapping
- Chopping mode (also known as Gated mode)
- Dead-time insertion
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB)
- 8 mA PWM pin output drive

Note: Duty cycle, dead time, phase shift and frequency resolution is 16.64 ns in Center-Aligned PWM mode.

The high-speed PWM module contains up to seven PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. Two master time base generators provide a synchronous signal as a common time base to synchronize the various PWM outputs. Each generator can operate independently or in synchronization with either of the two master time bases. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limited signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known “safe” state.

Each PWM can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWM module also generates two Special Event Triggers to the ADC module based on the two master time bases.

The high-speed PWM module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNC11 and SYNC12 pins are the input pins, which can synchronize the high-speed PWM module with an external signal. The SYNCO1 and SYNCO2 pins are output pins that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWM module and its interconnection with the CPU and other peripherals.

REGISTER 16-22: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER x

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15						bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH ⁽¹⁾	BCL ⁽¹⁾	BPHH	BPHL	BPLH	BPLL
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxH
- bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxH
- bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxL
- bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxL
- bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected Fault input
0 = Leading-Edge Blanking is not applied to selected Fault input
- bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input
- bit 9-6 **Unimplemented:** Read as '0'
- bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit⁽¹⁾
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when selected blanking signal is high
- bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit⁽¹⁾
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when selected blanking signal is low
- bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
0 = No blanking when PWMxH output is high
- bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
0 = No blanking when PWMxH output is low
- bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high
- bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

26.3 RTCC Registers

REGISTER 26-1: RCFGAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit⁽²⁾

1 = RTCC module is enabled

0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit

1 = RTCVAL register can be written to by the user application

0 = RTCVAL register is locked out from being written to by the user application

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit

1 = A rollover is about to occur in 32 clock edges (approximately 1 ms)

0 = A rollover will not occur

bit 11 **HALFSEC:** Half-Second Status bit⁽³⁾

1 = Second half period of a second

0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit

1 = RTCC output is enabled

0 = RTCC output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Pointer bits

Points to the corresponding RTCC Value register when reading the RTCVAL register; the RTCPTR<1:0> value decrements on every access of the RTCVAL register until it reaches '00'.

Note 1: The RCFGAL register is only affected by a POR.

2: A write to the RTCEN bit is only allowed when RTCWREN = 1.

3: This bit is read-only. It is cleared when the lower half of the MINSEC register is written.

NOTES:

FIGURE 32-25: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

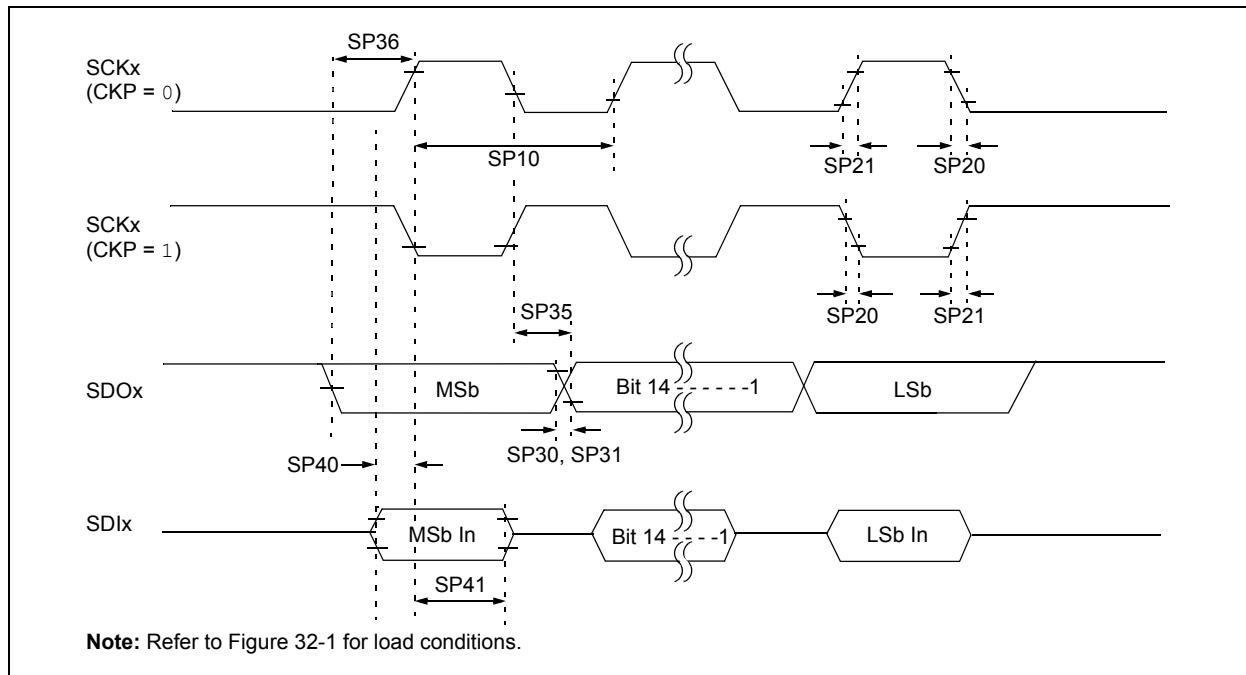


TABLE 32-43: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscP	Maximum SCKx Frequency	—	—	10	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

Note 2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

Note 3: The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPIx pins.

TABLE 32-47: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	TscP	Maximum SCKx Input Frequency	—	—	15	MHz	See Note 3
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx $\uparrow$ or SCKx $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx} \uparrow$ to SDOx Output, High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{SSx} \uparrow$ after SCKx Edge	1.5 TCY + 40	—	—	ns	See Note 4

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 32-58: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (see Note 4) (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	76	—	—	ns	
AD51	trc	ADC Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	12 TAD	—	—	
AD56	FCNV	Throughput Rate	—	—	1.1	Msps	Using sequential sampling
AD57	TSAMP	Sample Time	2 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger ⁽²⁾	2 TAD	—	3 TAD	—	Auto-Convert Trigger not selected
AD61	tpSS	Sample Start from Setting Sample (SAMP) bit ⁽²⁾	2 TAD	—	3 TAD	—	
AD62	tcSS	Conversion Completion to Sample Start (ASAM = 1) ⁽²⁾	—	0.5 TAD	—	—	
AD63	tdPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽²⁾	—	—	20	μs	See Note 3

Note 1: These parameters are characterized but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

3: The tDPU parameter is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.

4: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

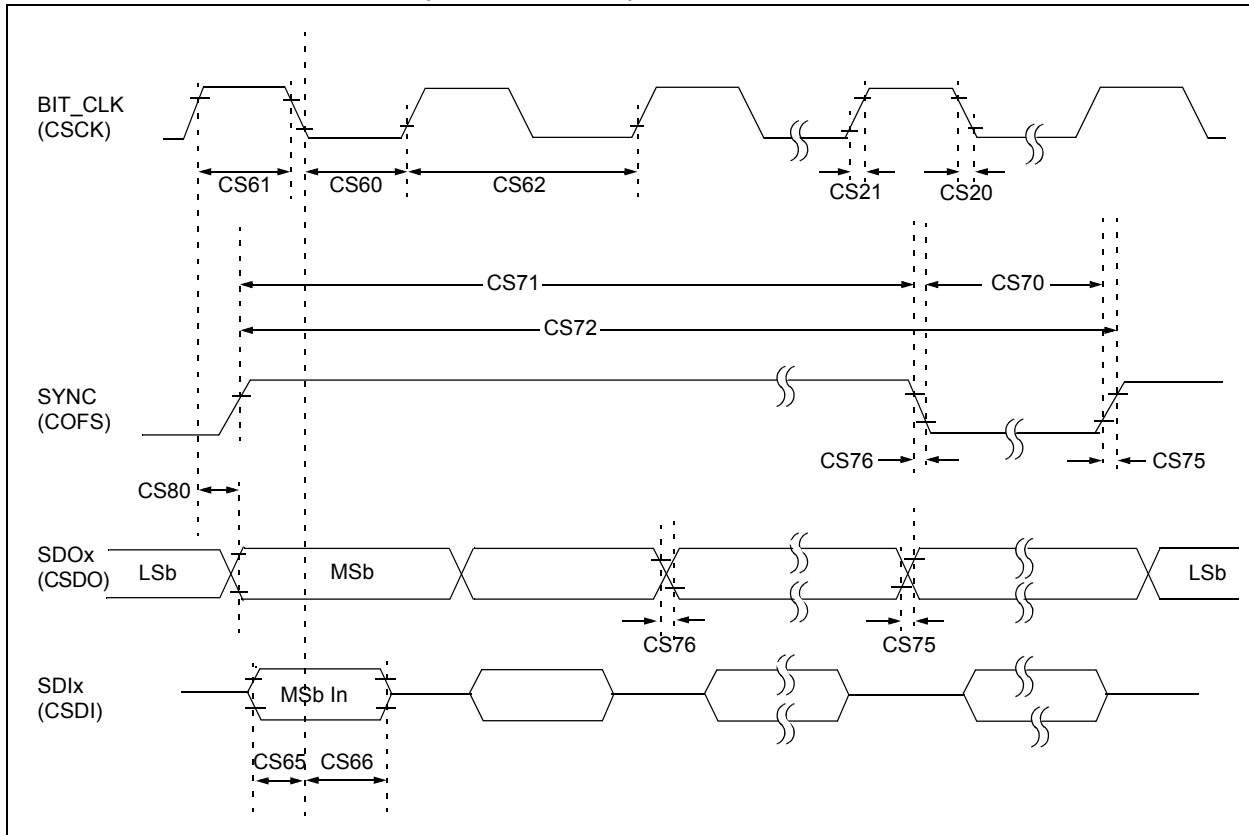
FIGURE 32-41: DCI MODULE (AC-LINK MODE) TIMING CHARACTERISTICS

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 21.0 “Enhanced CAN (ECAN™) Module”	Added the CANCKS bit to the ECAN Control Register 1 (CiCTRL1) (see Register 21-1).
Section 22.0 “USB On-The-Go (OTG) Module”	Removed the USB 3.3V Regulator logic from the USB Interface Diagram (see Figure 22-1).
Section 23.0 “10-bit/12-bit Analog-to-Digital Converter (ADC)”	Updated the ADC Conversion Clock Period Block Diagram (see Figure 23-2).
Section 29.0 “Special Features”	Updated the last paragraph of Section 29.1 “Configuration Bits” Added a note box after the last paragraph of Section 29.3 “BOR: Brown-out Reset (BOR)”. Added the RTSP Effect column to the Configuration Bits Description (see Table 29-2).
Section 30.0 “Instruction Set Summary”	Updated all Status Flags Affected to None for the MOV instruction and added Note 2 (see Table 30-2).
Section 32.0 “Electrical Characteristics”	Updated the Absolute Maximum Ratings (see page 457). Added Note 1 to the Operating MIPS vs. Voltage (see Table 32-1). Added parameter DI31 (ICNPD) to the I/O Pin Input Specifications (see Table 32-9). Updated the Minimum value for parameter DO26 in the I/O Pin Output Specifications (see Table 32-10). Updated the Minimum value for parameter D132b and the Minimum and Maximum values for parameters D136a, D136b, D137a, D137b, D138a, and D138b in the Program Memory specification (see Table 32-12). Updated the Minimum, Typical, and Maximum values for parameter OS10 (Oscillator Crystal Frequency: SOSC) in the External Clock Timing Requirements (see Table 32-16). Added Note 2 to the PLL Clock Timing Specifications (see Table 32-17). Updated all Timer1 External Clock Timing Requirements (see Table 32-23). Replaced Table 32-34 with Timer2, Timer4, Timer6, Timer8 External Clock Timing Requirements and Timer3, Timer5, Timer7, Timer9 External Clock Timing Requirements (see Table 32-24 and Table 32-25, respectively). Updated the Maximum value for parameter OC15 and the Minimum value for parameter OC20 in the OC/PWM Mode Timing Requirements (see Table 32-29). Updated the Operating Temperature in the ECAN Module I/O Timing Requirements and USB OTG Timing Requirements (see Table 32-51 and Table 32-53, respectively). Updated all SPI specifications (see Figure 32-15 through Figure 32-30 and Table 32-33 through Table 32-48). Removed Note 4 from the DCI Module Timing Requirements (see Table 32-59). Updated the Standard Operating Conditions voltage for the Comparator Specifications (see Table 32-61 through Table 32-64).

Revision F (February 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

Throughout the document, references to the package formerly known as XBGA where changed to TFBGA.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see **Section 18.1 “SPI Helpful Tips”** and **Section 18.2 “SPI Resources”**. The major changes are referenced by their respective section in Table A-4.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
“16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, USB and Advanced Analog”	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an “at-a-glance” format. The following devices were added to the Controller Families table (see Table 1 and the “Pin Diagrams” section): • dsPIC33EP512MC806 • dsPIC33EP512GP806 • PIC24EP512GP806
Section 2.0 “Guidelines for Getting Started with 16-Bit Digital Signal Controllers and Microcontrollers”	Added Section 2.9 “Application Examples”
Section 3.0 “CPU”	Updated the Status Register information in the Programmer’s Model (see Figure 3-2).
Section 4.0 “Memory Organization”	Added Interrupt Controller Register Maps (see Table 4-6 and Table 4-7). Added Peripheral Pin Select Output Register Map (see Table 4-39). Added PMD Register Maps (see Table 4-50 and Table 4-51). Added PORTF Register Map (see Table 4-64). Added PORTG Register Map (see Table 4-67). Updated the second note in Section 4.7 “Bit-Reversed Addressing (dsPIC33EPXXXMU806/810/814 Devices Only)”.
Section 11.0 “I/O Ports”	Added RPOR10: Peripheral Pin Select Output Register 10 (see Register 11-54).
Section 14.0 “Input Capture”	Updated the Input Capture Module Block Diagram (see Figure 14-1).
Section 15.0 “Output Compare”	Updated the Output Compare Module Block Diagram (see Figure 15-1).
Section 25.0 “Comparator Module”	Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-4).
Section 29.0 “Special Features”	Added Note 3 to the Configuration Bits Description (see Table 29-2).
Section 32.0 “Electrical Characteristics”	Updated the I/O pin Absolute Maximum Ratings. Updated Note 1 in the DC Characteristics: Operating Current (see Table 32-5). Updated Note 1 in the DC Characteristics: Idle Current (see Table 32-6). Updated Note 1 in the DC Characteristics: Power-down Current (see Table 32-7). Updated Note 1 in the DC Characteristics: Doze Current (see Table 32-8). Removed parameters DO16 and DO26, added parameter DO26a, updated parameters DO10 and DO20, and added Note 1 in the DC Characteristics: I/O Pin Output Specifications (see Table 32-10).

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