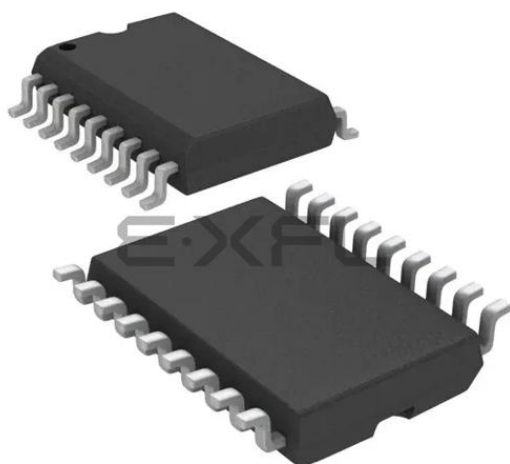




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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj12gp201-i-so

PIC24HJ12GP201/202

High-Performance, 16-bit Microcontrollers

Operating Range:

- Up to 40 MIPS operation (@ 3.0-3.6V):
 - Industrial temperature range (-40°C to +85°C)
 - Extended temperature range (-40°C to +125°C)

High-Performance CPU:

- Modified Harvard architecture
- C compiler optimized instruction set
- 16-bit-wide data path
- 24-bit-wide instructions
- Linear program memory addressing up to 4M instruction words
- Linear data memory addressing up to 64 Kbytes
- 71 base instructions, mostly one word/one cycle
- Sixteen 16-bit general purpose registers
- Flexible and powerful addressing modes
- Software stack
- 16 x 16 multiply operations
- 32/16 and 16/16 divide operations
- Up to ± 16 -bit shifts for up to 40-bit data

Interrupt Controller:

- 5-cycle latency
- Up to 21 available interrupt sources
- Up to three external interrupts
- Seven programmable priority levels
- Four processor exceptions

On-Chip Flash and SRAM:

- Flash program memory (12 Kbytes)
- Data SRAM (1024 bytes)
- Boot and General Security for Program Flash

Digital I/O:

- Peripheral Pin Select Functionality
- Up to 21 programmable digital I/O pins
- Wake-up/Interrupt-on-Change for up to 21 pins
- Output pins can drive from 3.0V to 3.6V
- Up to 5V output with open drain configurations on 5V tolerant pins
- 4 mA sink on all I/O pins

System Management:

- Flexible clock options:
 - External, crystal, resonator, internal RC
 - Fully integrated Phase-Locked Loop (PLL)
 - Extremely low-jitter PLL
- Power-up Timer
- Oscillator Start-up Timer/Stabilizer
- Watchdog Timer with its own RC oscillator
- Fail-Safe Clock Monitor (FSCM)
- Reset by multiple sources

Power Management:

- On-chip 2.5V voltage regulator
- Switch between clock sources in real time
- Idle, Sleep, and Doze modes with fast wake-up

Timers/Capture/Compare:

- Timer/Counters, up to three 16-bit timers:
 - Can pair up to make one 32-bit timer
 - One timer runs as Real-Time Clock with external 32.768 kHz oscillator
 - Programmable prescaler
- Input Capture (up to four channels):
 - Capture on up, down, or both edges
 - 16-bit capture input functions
 - 4-deep FIFO on each capture
- Output Compare (up to two channels):
 - Single or Dual 16-bit Compare mode
 - 16-bit Glitchless PWM Mode

TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	Reserved
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC1
22	14	0x000030	0x000130	Reserved
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	Reserved
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	Reserved
33	25	0x000046	0x000146	Reserved
34	26	0x000048	0x000148	Reserved
35	27	0x00004A	0x00014A	Reserved
36	28	0x00004C	0x00014C	Reserved
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	Reserved
39	31	0x000052	0x000152	Reserved
40	32	0x000054	0x000154	Reserved
41	33	0x000056	0x000156	Reserved
42	34	0x000058	0x000158	Reserved
43	35	0x00005A	0x00015A	Reserved
44	36	0x00005C	0x00015C	Reserved
45	37	0x00005E	0x00015E	Reserved
46	38	0x000060	0x000160	Reserved
47	39	0x000062	0x000162	Reserved
48	40	0x000064	0x000164	Reserved
49	41	0x000066	0x000166	Reserved
50	42	0x000068	0x000168	Reserved
51	43	0x00006A	0x00016A	Reserved
52	44	0x00006C	0x00016C	Reserved
53	45	0x00006E	0x00016E	Reserved

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **ALTIVT:** Enable Alternate Interrupt Vector Table bit
 1 = Use alternate vector table
 0 = Use standard (default) vector table
- bit 14 **DISI:** DISI Instruction Status bit
 1 = DISI instruction is active
 0 = DISI instruction is not active
- bit 13-3 **Unimplemented:** Read as '0'
- bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
 1 = Interrupt on negative edge
 0 = Interrupt on positive edge
- bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
 1 = Interrupt on negative edge
 0 = Interrupt on positive edge
- bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
 1 = Interrupt on negative edge
 0 = Interrupt on positive edge

REGISTER 7-10: IEC4: INTERRUPT ENABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	U1EIE	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **U1EIE:** UART1 Error Interrupt Enable bit

1 = Interrupt request enabled

0 = Interrupt request not enabled

bit 0 **Unimplemented:** Read as '0'

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REGISTER 8-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

000000000 = 2

000000001 = 3

000000010 = 4

•

•

•

000110000 = 50 (default)

•

•

•

111111111 = 513

Note 1: This register is reset only on a Power-on Reset (POR).

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REGISTER 10-9: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	SS1R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5

Unimplemented: Read as '0'

bit 4-0

SS1R<4:0>: Assign SPI1 Slave Select Input (SS1IN) to the Corresponding RPn pin bits

11111 = Input tied to Vss

01111 = Input tied to RP15

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0



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13.1 Input Capture Registers

REGISTER 13-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
 1 = Input capture module will halt in CPU Idle mode
 0 = Input capture module will continue to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture Timer Select bits
 1 = TMR2 contents are captured on capture event
 0 = TMR3 contents are captured on capture event

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
 11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
 1 = Input capture overflow occurred
 0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status bit (read-only)
 1 = Input capture buffer is not empty, at least one more capture value can be read
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
 111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode
 (Rising edge detect only, all other control bits are not applicable.)
 110 = Unused (module disabled)
 101 = Capture mode, every 16th rising edge
 100 = Capture mode, every 4th rising edge
 011 = Capture mode, every rising edge
 010 = Capture mode, every falling edge
 001 = Capture mode, every edge (rising and falling)
 (ICI<1:0> bits do not control interrupt generation for this mode.)
 000 = Input capture module turned off

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REGISTER 15-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
SPIEN	—	SPISIDL	—	—	—	—	—
bit 15						bit 8	

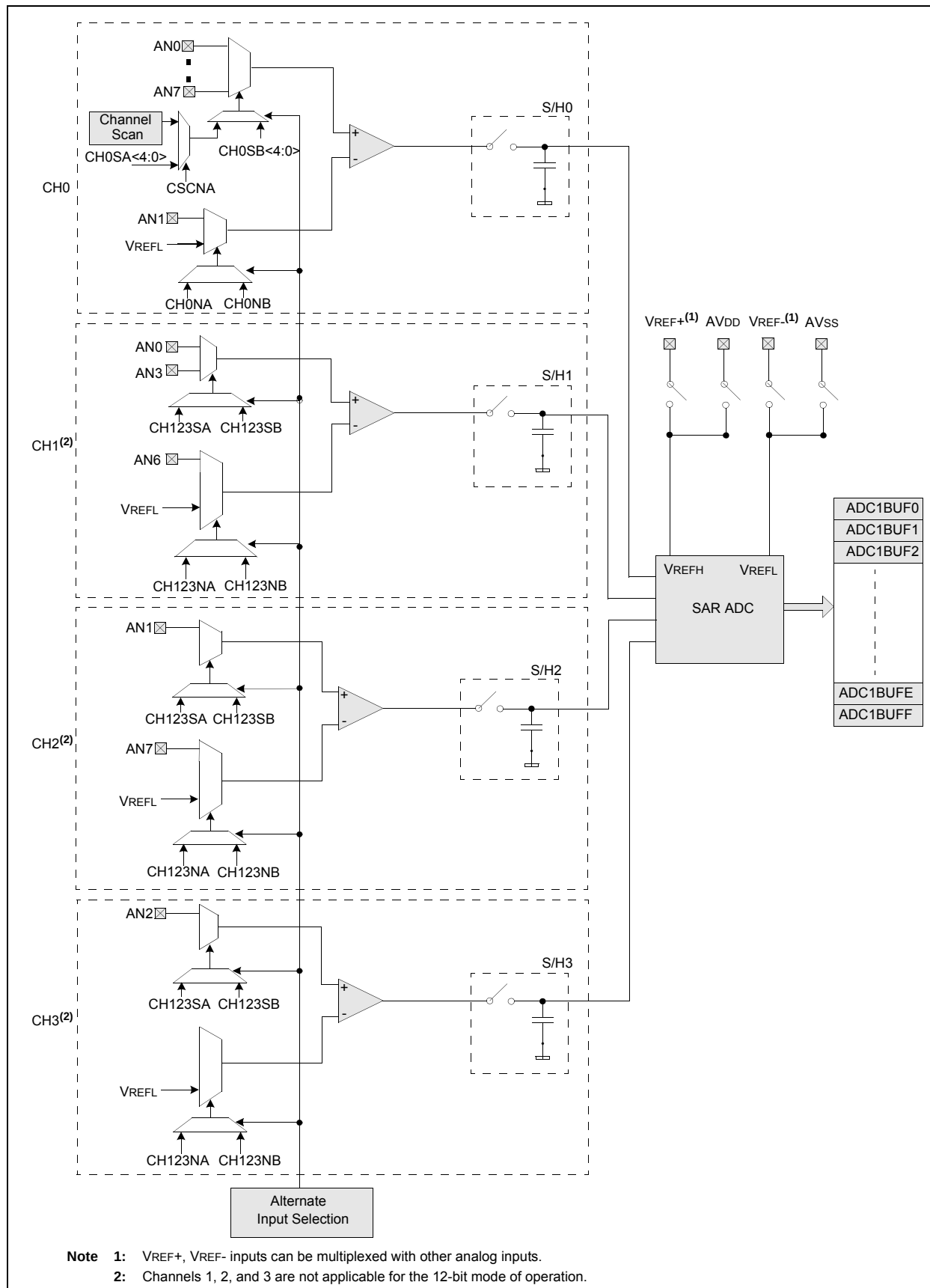
U-0	R/C-0	U-0	U-0	U-0	U-0	R-0	R-0
—	SPIROV	—	—	—	—	SPITBF	SPIRBF
bit 7						bit 0	

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **SPIEN:** SPIx Enable bit
1 = Enables module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPISIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred.
- bit 5-2 **Unimplemented:** Read as '0'
- bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty
Automatically set in hardware when CPU writes SPIxBUF location, loading SPIxTXB
Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR
- bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive complete, SPIxRXB is full
0 = Receive is not complete, SPIxRXB is empty
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB
Automatically cleared in hardware when core reads SPIxBUF location, reading SPIxRXB

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FIGURE 18-1: ADC BLOCK DIAGRAM FOR PIC24HJ12GP201 DEVICES



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REGISTER 18-4: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER (CONTINUED)

bit 8	CH123SB: Channel 1, 2, 3 Positive Input Select for Sample B bit PIC24HJ12GP201 devices only: <u>If AD12B = 1:</u> 1 = Reserved 0 = Reserved <u>If AD12B = 0:</u> 1 = CH1 positive input is AN3, CH2 and CH3 positive inputs are not connected 0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2 PIC24HJ12GP202 devices only: <u>If AD12B = 1:</u> 1 = Reserved 0 = Reserved <u>If AD12B = 0:</u> 1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5 0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2
bit 7-3	Unimplemented: Read as '0'
bit 2-1	CH123NA<1:0>: Channel 1, 2, 3 Negative Input Select for Sample A bits PIC24HJ12GP201 devices only: <u>If AD12B = 1:</u> 11 = Reserved 10 = Reserved 01 = Reserved 00 = Reserved <u>If AD12B = 0:</u> 11 = Reserved 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is not connected 01 = CH1, CH2, CH3 negative input is VREF- 00 = CH1, CH2, CH3 negative input is VREF- PIC24HJ12GP202 devices only: <u>If AD12B = 1:</u> 11 = Reserved 10 = Reserved 01 = Reserved 00 = Reserved <u>If AD12B = 0:</u> 11 = CH1 negative input is AN9, CH2 and CH3 negative inputs are not connected 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8 01 = CH1, CH2, CH3 negative input is VREF- 00 = CH1, CH2, CH3 negative input is VREF-

TABLE 19-2: PIC24HJ12GP201/202 CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	RTSP Effect	Description
FWDTEN	FWDT	Immediate	Watchdog Timer Enable bit 1 = Watchdog Timer always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	FWDT	Immediate	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
WDTPRE	FWDT	Immediate	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	FWDT	Immediate	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 . . . 0001 = 1:2 0000 = 1:1
ALT2C	FPOR	Immediate	Alternate I ² C™ pins 1 = I ² C mapped to SDA1/SCL1 pins 0 = I ² C mapped to ASDA1/ASCL1 pins
FPWRT<2:0>	FPOR	Immediate	Power-on Reset Timer Value Select bits 111 = PWRT = 128 ms 110 = PWRT = 64 ms 101 = PWRT = 32 ms 100 = PWRT = 16 ms 011 = PWRT = 8 ms 010 = PWRT = 4 ms 001 = PWRT = 2 ms 000 = PWRT = Disabled
JTAGEN	FICD	Immediate	JTAG Enable bit 1 = JTAG enabled 0 = JTAG disabled
ICS<1:0>	FICD	Immediate	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use

TABLE 20-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
66	TBLRDL	TBLRDL <i>Ws, Wd</i>	Read Prog<15:0> to Wd	1	2	None
67	TBLWTH	TBLWTH <i>Ws, Wd</i>	Write Ws<7:0> to Prog<23:16>	1	2	None
68	TBLWTL	TBLWTL <i>Ws, Wd</i>	Write Ws to Prog<15:0>	1	2	None
69	ULNK	ULNK	Unlink Frame Pointer	1	1	None
70	XOR	XOR <i>f</i>	$f = f .XOR. WREG$	1	1	N,Z
		XOR <i>f, WREG</i>	$WREG = f .XOR. WREG$	1	1	N,Z
		XOR <i>#lit10, Wn</i>	$Wd = lit10 .XOR. Wd$	1	1	N,Z
		XOR <i>Wb, Ws, Wd</i>	$Wd = Wb .XOR. Ws$	1	1	N,Z
		XOR <i>Wb, #lit5, Wd</i>	$Wd = Wb .XOR. lit5$	1	1	N,Z
71	ZE	ZE <i>Ws, Wnd</i>	Wnd = Zero-extend Ws	1	1	C,Z,N

FIGURE 22-2: EXTERNAL CLOCK TIMING

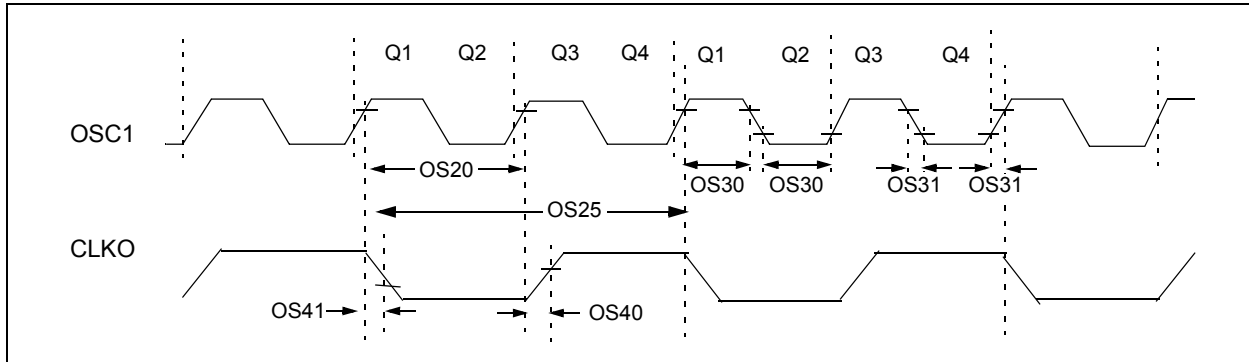


TABLE 22-16: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	40	MHz	EC
		Oscillator Crystal Frequency	3.5 10 —	— — —	10 40 33	MHz MHz kHz	XT HS SOSC
OS20	Tosc	Tosc = 1/Fosc ⁽⁴⁾	12.5	—	DC	ns	—
OS25	Tcy	Instruction Cycle Time ^(2,4)	25	—	DC	ns	—
OS30	TosL, TosH	External Clock in (OSC1) ⁽⁵⁾ High or Low Time	0.375 x Tsc	—	0.625 x Tsc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) ⁽⁵⁾ Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,5)	—	5.2	—	ns	—
OS41	TckF	CLKO Fall Time ^(3,5)	—	5.2	—	ns	—
OS42	GM	External Oscillator Transconductance ⁽⁶⁾	14	16	18	mA/V	VDD = 3.3V TA = +25°C

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

- 2:** Instruction cycle period (Tcy) equals two times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits can result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.
- 3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4:** These parameters are characterized by similarity, but are tested in manufacturing at FIN = 40 MHz only.
- 5:** These parameters are characterized by similarity, but are not tested in manufacturing.
- 6:** Data for this parameter is preliminary. This parameter is characterized, but is not tested in manufacturing.

FIGURE 22-8: OC/PWM MODULE TIMING CHARACTERISTICS

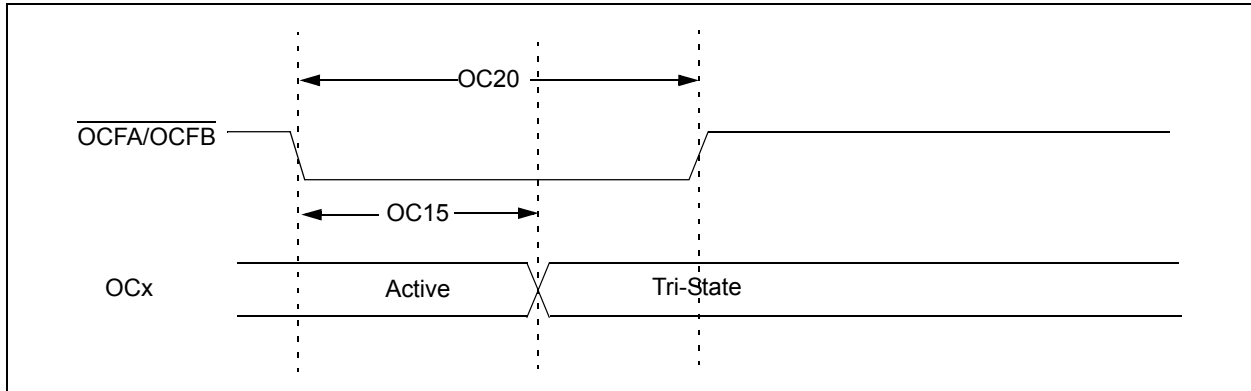


TABLE 22-27: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	$T_{CY} + 20$	ns	—
OC20	TFLT	Fault Input Pulse Width	$T_{CY} + 20$	—	—	ns	—

Note 1: These parameters are characterized by similarity, but are not tested in manufacturing.

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FIGURE 22-11: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = X, SMP = 1) TIMING CHARACTERISTICS

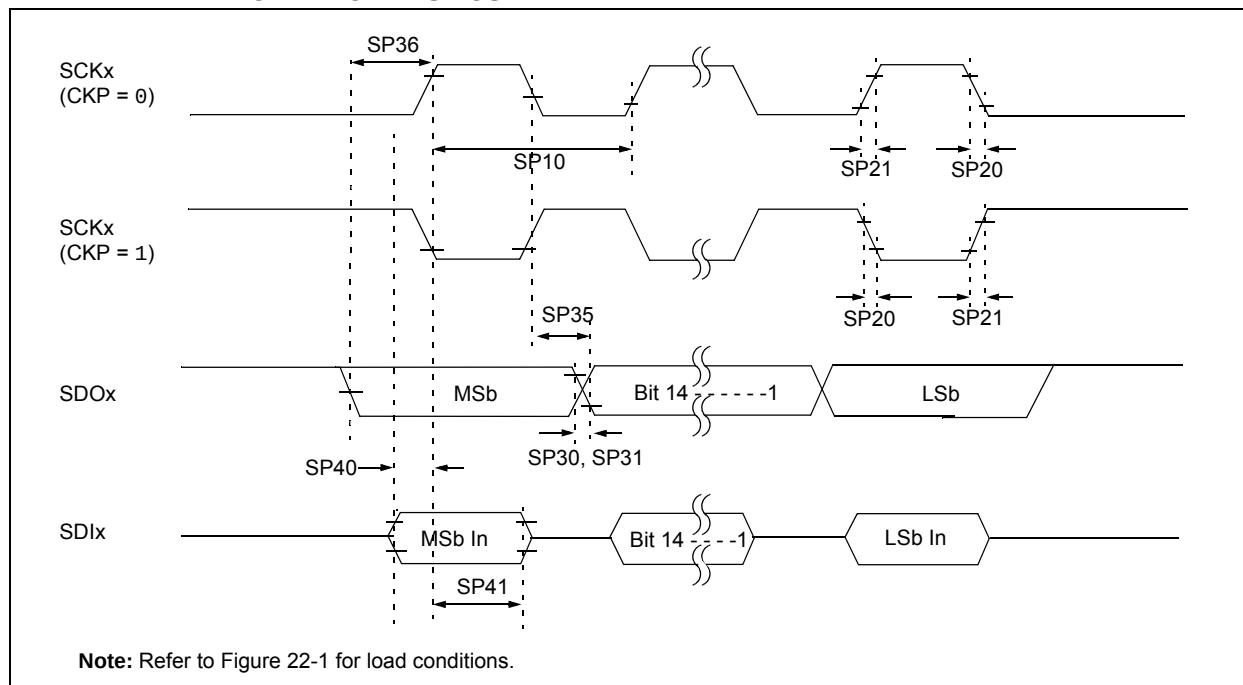


TABLE 22-30: SPIx MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = X, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	—	9	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	—
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	—

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

APPENDIX A: REVISION HISTORY

Revision A (February 2007)

This is the initial released version of this document.

Revision B (May 2007)

This revision includes the following corrections and updates:

- Minor typographical and formatting corrections throughout the data sheet text.
- New content:
 - Addition of bullet item (16-word conversion result buffer) (see **Section 17.1 “Key Features”**)
- Figure update:
 - Oscillator System Diagram (see Figure 7-1)
 - WDT Block Diagram (see Figure 18-2)
- Equation update:
 - Serial Clock Rate (see Equation 15-1)
- Register updates:
 - Clock Divisor Register (see Register 7-2)
 - PLL Feedback Divisor Register (see Register 7-3)
 - Peripheral Pin Select Input Registers (see Register 9-1 through Register 9-9)
 - ADC1 Input Channel 1, 2, 3 Select Register (see Register 17-4)
 - ADC1 Input Channel 0 Select Register (see Register 17-5)
- Table updates:
 - CNEN2 (see Table 3-2 and Table 3-3)
 - Reset Flag Bit Operation (see Table 5-1)
 - Configuration Bit Values for Clock Operation (see Table 7-1)
- Operation value update:
 - IOLOCK set/clear operation (see **Section 9.4.3.1 “Control Register Lock”**)
- The following tables in **Section 21.0 “Electrical Characteristics”** have been updated with preliminary values:
 - Updated Max MIPS for -40°C to +125°C Temp Range (see Table 21-1)
 - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-5)
 - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-6)
 - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-7)
 - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-8)
 - Updated parameter DI51, added parameter DI51a (see Table 21-9)
 - Added Note 1 (see Table 21-11)
 - Updated parameter OS30 (see Table 21-16)
 - Updated parameter OS52 (see Table 21-17)
 - Updated parameter F20, added Note 2 (see Table 21-18)
 - Updated parameter TA15 (see Table 21-22)
 - Updated parameter TB15 (see Table 21-23)
 - Updated parameter TC15 (see Table 21-24)
 - Updated parameters AD05, AD06, AD07, AD08, AD10, and AD11; added parameters AD05a and AD06a; added Note 2; modified ADC Accuracy headings to include measurement information (see Table 21-34)
 - Separated the ADC Module Specification table in to three tables (see Table 21-34, Table 21-35, and Table 21-36)
 - Updated parameter AD50 (see Table 21-37)
 - Updated parameters AD50 and AD57 (see Table 21-38)

TABLE 23-1: MAJOR SECTION UPDATES

Section Name	Update Description
Section 14.0 “Serial Peripheral Interface (SPI)”	Removed the following sections, which are now available in the related section of the “PIC24H Family Reference Manual”: • 14.1 “Interrupts” • 14.2 “Receive Operations” • 14.3 “Transmit Operations” • 14.4 “SPI Setup” (retained Figure 14-1: SPI Module Block Diagram)
Section 15.0 “Inter-Integrated Circuit™ (I²C)”	Removed the following sections, which are now available in the related section of the “PIC24H Family Reference Manual”: • 15.3 “I²C Interrupts” • 15.4 “Baud Rate Generator” (retained Figure 15-1: I²C Block Diagram) • 15.5 “I²C Module Addresses • 15.6 “Slave Address Masking” • 15.7 “IPMI Support” • 15.8 “General Call Address Support” • 15.9 “Automatic Clock Stretch” • 15.10 “Software Controlled Clock Stretching (STREN = 1)” • 15.11 “Slope Control” • 15.12 “Clock Arbitration” • 15.13 “Multi-Master Communication, Bus Collision, and Bus Arbitration • 15.14 “Peripheral Pin Select Limitations
Section 16.0 “Universal Asynchronous Receiver Transmitter (UART)”	Removed the following sections, which are now available in the related section of the “PIC24H Family Reference Manual”: • 16.1 “UART Baud Rate Generator” • 16.2 “Transmitting in 8-bit Data Mode • 16.3 “Transmitting in 9-bit Data Mode • 16.4 “Break and Sync Transmit Sequence” • 16.5 “Receiving in 8-bit or 9-bit Data Mode” • 16.6 “Flow Control Using $\overline{UxCTS}$ and $\overline{UxRTS}$ Pins” • 16.7 “Infrared Support” Removed IrDA references and Note 1, and updated the bit and bit value descriptions for UTXINV ($UxSTA<14>$) in the UARTx Status and Control Register (see Register 16-2).

TABLE 23-3: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 22.0 “Electrical Characteristics”	Updated the following Absolute Maximum Ratings: • Storage temperature • Voltage on any pin that is not 5V tolerant with respect to V_{SS} • Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} ≥ 3.0V • Voltage on any 5V tolerant pin with respect to V_{SS} when V_{DD} < 3.0V • Added Note 4 Revised parameters DI18, DI19, DI50, and DI51, added parameters DI21, DI25, DI26, DI27, DI28, DI29, DI60a, DI60b, and DI60c, and added Notes 5, 6, 7, 8, and 9 to the I/O Pin Input Specifications (see Table 22-9). Removed Note 2 from the AC Characteristics: Internal RC Accuracy (see Table 22-18). Updated the maximum value for parameter OC15 and the minimum value for parameter OC20 in the Simple OC/PWM Mode Timing Requirements (see Table 22-27). Updated <i>all</i> SPI specifications (see Table 22-28 through Table 22-35 and Figure 22-9 through Figure 22-16). Updated the minimum values for parameters AD05 and AD07, and the maximum value for parameter AD06 in the ADC Module Specifications (see Table 22-38). Added Note 4 regarding injection currents to the ADC Module Specifications (12-bit mode) (see Table 22-39). Added Note 4 regarding injection currents to the ADC Module Specifications (10-bit mode) (see Table 22-40).

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