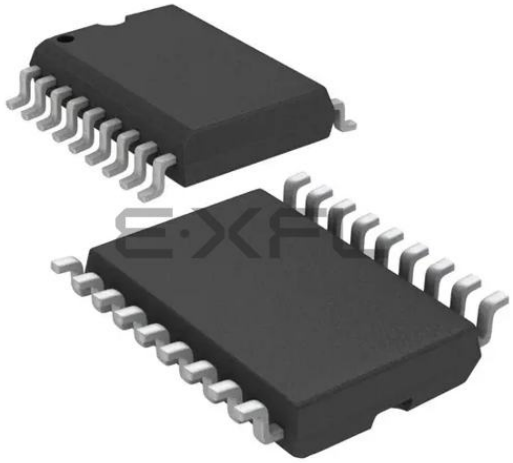

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj12gp201t-i-so

1.0 DEVICE OVERVIEW

Note 1:	This data sheet summarizes the features of the PIC24HJ12GP201/202 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
2:	Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 Memory Organization in this data sheet for device-specific register and bit information.

This document contains device specific information for the PIC24HJ12GP201/202 devices. PIC24H devices contain extensive functionality with a high-performance, 16-bit microcontroller (MCU) architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules in the PIC24HJ12GP201/202 family of devices. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

8.2 Clock Switching Operation

Applications are free to switch among any of the four clock sources (Primary, LP, FRC and LPRC) under software control at any time. To limit the possible side effects of this flexibility, PIC24HJ12GP201/202 devices have a safeguard lock built into the switch process.

Note:	Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch among the different primary submodes without reprogramming the device.

8.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in the Configuration register must be programmed to `0`. (Refer to Section 19.1 Configuration Bits for further details.) If the FCKSM1 Configuration bit is unprogrammed (`1`), the clock switching function and Fail-Safe Clock Monitor function are disabled. This is the default setting.

The NOSC control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC bits (OSCCON<14:12>) reflect the clock source selected by the FNOSC Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled. It is held at `0` at all times.

8.2.2 OSCILLATOR SWITCHING SEQUENCE

Performing a clock switch requires this basic sequence:

1. If desired, read the COSC bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSC control bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

When the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSC status bits with the new value of the NOSC control bits. If they are the same, the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and the CF (OSCCON<3>) status bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware waits until the Oscillator Start-up Timer (OST) expires. If the new source is using the PLL, the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC bit values are transferred to the COSC status bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM are enabled) or LP (if LPOSCEN remains set).

Note 1:	The processor continues to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
2:	Direct clock switches between any primary oscillator mode with PLL and FRC-PLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
3:	Refer to 7. Oscillator (DS70186) in the *"dsPIC33F/PIC24H Family Reference Manual"* for details.

8.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by programming. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the Watchdog Timer.

In the event of an oscillator failure, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. Then the application program can either attempt to restart the oscillator or execute a controlled shutdown. The trap can be treated as a warm Reset by simply loading the Reset address into the oscillator fail trap vector.

If the PLL multiplier is used to scale the system clock, the internal FRC is also multiplied by the same factor on clock failure. Essentially, the device switches to FRC with PLL on a clock failure.

NOTES:

REGISTER 10-9: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			SS1R<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 15-5 Unimplemented: Read as 0

bit 4-0 SS1R<4:0>: Assign SPI1 Slave Select Input (SS1IN) to the Corresponding RPn pin bits

11111 = Input tied to Vss
01111 = Input tied to RP15

00001 = Input tied to RP1
00000 = Input tied to RP0

16.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note 1:	This data sheet summarizes the features of the PIC24HJ12GP201/202 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 19. Inter-Integrated Circuit (I^2C) (DS70195) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).
2:	Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 Memory Organization in this data sheet for device-specific register and bit information.

The Inter-Integrated Circuit (I^2C) module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

The SCLx pin is clock
The SDAx pin is data

The I^2C module offers the following key features:

- I^2C interface supporting both Master and Slave modes of operation
- I^2C Slave mode supports 7-bit and 10-bit addresses
- I^2C Master mode supports 7-bit and 10-bit addresses
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation, detects bus collision and arbitrates accordingly

16.1 Operating Modes

The hardware fully implements all the master and slave functions of the I^2C Standard and Fast mode specifications, as well as 7-bit and 10-bit addressing.

The I^2C module can operate either as a slave or a master on an I^2C bus.

The following types of I^2C operation are supported:

- I^2C slave operation with 7-bit address
- I^2C slave operation with 10-bit address
- I^2C master operation with 7-bit or 10-bit address

For details about the communication sequence in each of these modes, refer to the Microchip web site (www.microchip.com) for the latest *"dsPIC33F/PIC24H Family Reference Manual"* sections.

16.2 I^2C Registers

I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CSTAT are read/write.

I2CxRSR is the shift register used for shifting data

I2CxRCV is the receive buffer and the register to which data bytes are written, or from which data bytes are read

I2CxTRN is the transmit register to which bytes are written during a transmit operation

I2CxADD register holds the slave address

ADD10 status bit indicates 10-bit Address mode

I2CxBRG acts as the Baud Rate Generator (BRG) reload value

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV, and an interrupt pulse is generated.

REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 S: Start bit

1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 R_W: Read/Write Information bit (when operating as I^2C slave)

1 = Read indicates data transfer is output from slave
0 = Write indicates data transfer is input to slave
Hardware set or clear after reception of I^2C device address byte.

bit 1 RBF: Receive Buffer Full Status bit

1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 TBF: Transmit Buffer Full Status bit

1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

NOTES:

18.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1:	This data sheet summarizes the features of the PIC24HJ12GP201/202 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 16 . Analog-to-Digital Converter (ADC) with DMA (DS70183) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).
2:	Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 Memory Organization in this data sheet for device-specific register and bit information.

The PIC24HJ12GP201/202 devices have up to 10 ADC module input channels.

The AD12B bit (AD1CON1<10>), allows each of the ADC modules to be configured as either a 10-bit, 4-sample-and-hold ADC (default configuration) or a 12-bit, 1-sample-and-hold ADC.

Note:	The ADC module must be disabled before the AD12B bit can be modified.

18.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- Up to 10 analog input pins
- External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan mode
- Selectable conversion trigger source
- Selectable Buffer Fill modes
- Operation during CPU Sleep and Idle modes
- 16-word conversion result buffer

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one sample-and-hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported

Depending on the particular device pinout, the ADC can have up to 10 analog input pins, designated AN0 through AN9. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs can be shared with other analog input pins.

The actual number of analog input pins and external voltage reference input configuration will depend on the specific device. Refer to the device data sheet for further details.

Block diagrams of the ADC module are shown in Figure 18-1 and Figure 18-2.

18.2 ADC Initialization

To configure the ADC module:

1. Select port pins as analog inputs (AD1PCFGH<15:0> or AD1PCFGL<15:0>).
2. Select voltage reference source to match expected range on analog inputs (AD1CON2<15:13>).
3. Select the analog conversion clock to match desired data rate with processor clock (AD1CON3<7:0>).
4. Determine how many sample-and-hold channels will be used (AD1CON2<9:8> and AD1PCFGH<15:0> or AD1PCFGL<15:0>).
5. Select the appropriate sample/conversion sequence (AD1CON1<7:5> and AD1CON3<12:8>).
6. Select the way conversion results are presented in the buffer (AD1CON1<9:8>).
   a) Turn on the ADC module (AD1CON1<15>).
7. Configure ADC interrupt (if required):
   a) Clear the AD1IF bit.
   b) Select ADC interrupt priority.

TABLE 22-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C TA +85°C for Industrial -40°C TA +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ (1)	Max	Units	Conditions
	IIL	Input Leakage Current (2,3)					
DI50		I/O Pins 5V Tolerant(4)			–2	µA	VSS VPIN VDD, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant(4)			–1	µA	VSS VPIN VDD, Pin at high-impedance, -40°C TA +85°C
DI51a		I/O Pins Not 5V Tolerant(4)			–2	µA	Shared with external reference pins, -40°C TA +85°C
DI51b		I/O Pins Not 5V Tolerant(4)			–3.5	µA	VSS VPIN VDD, Pin at high-impedance, -40°C TA +125°C
DI51c		I/O Pins Not 5V Tolerant(4)			–8	µA	Analog pins shared with external reference pins, -40°C TA +125°C
DI55		$\overline{\text{MCLR}}$			–2	µA	VSS VPIN VDD
DI56		OSC1			–2	µA	VSS VPIN VDD, XT and HS modes

Note 1: Data in Typ column is at 3.3V, 25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See Pin Diagrams for a list of 5V tolerant pins.

5: VIL source < (VSS 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any positive input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical absolute instantaneous sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

10: These parameters are characterized, but not tested.

TABLE 22-9: DC CHARACTERISTICS: I/O PI N INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C TA +85°C for Industrial -40°C TA +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ (1)	Max	Units	Conditions
DI60a	IICL	Input Low Injection Current	0		-5 (5,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, and SOSCO
DI60b	IICH	Input High Injection Current	0		+5 (6,7,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO, and digital 5V-tolerant designated pins
DI60c	IICT	Total Input Injection Current (sum of all I/O and control pins)	-20(9)		+20 (9)	mA	Absolute instantaneous sum of all – input injection currents from all I/O pins (| IICL + | IICH |) IICT

Note 1: Data in Typ column is at 3.3V, 25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See Pin Diagrams for a list of 5V tolerant pins.

5: VIL source < (VSS 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

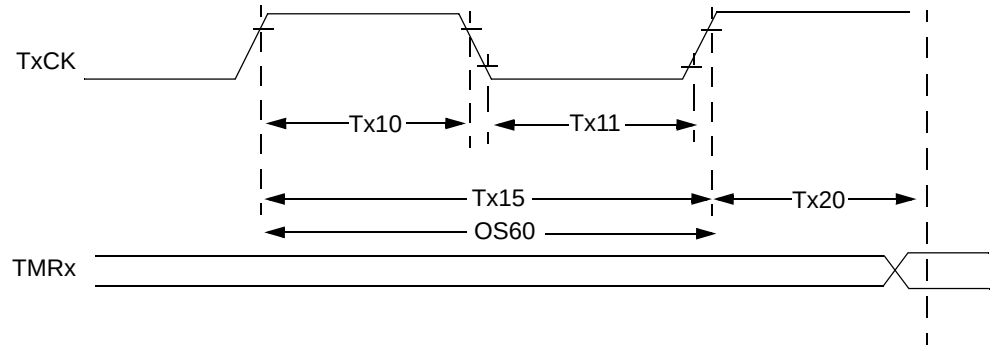
7: Digital 5V tolerant pins cannot tolerate any positive input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical absolute instantaneous sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

10: These parameters are characterized, but not tested.

FIGURE 22-5: TIMER1, 2, 3 AND 4 EXTERNAL CLOCK TIMING CHARACTERISTICS



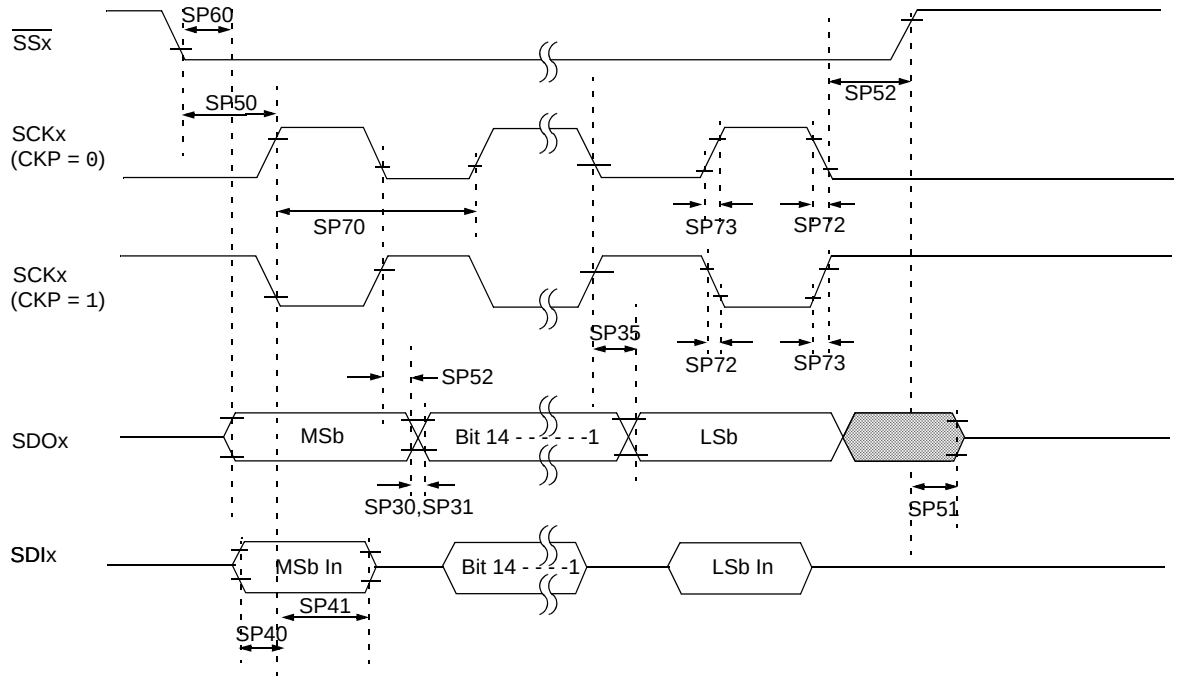
Note: Refer to Figure 22-1 for load conditions.

TABLE 22-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS (1)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C TA +85°C for Industrial -40°C TA +125°C for Extended				
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
TA10	TTXH	TxCK High Time	Synchronous, no prescaler	TCY + 20			ns	Must also meet parameter TA15. N = prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(TCY + 20)/N			ns	
			Asynchronous	20			ns	
TA11	TTXL	TxCK Low Time	Synchronous, no prescaler	(TCY + 20)			ns	Must also meet parameter TA15. N = prescale value (1, 8, 64, 256)
			Synchronous, with prescaler	(TCY + 20)/N			ns	
			Asynchronous	20			ns	
TA15	TTXP	TxCK Input Period	Synchronous, no prescaler	2 TCY + 40			ns	
			Synchronous, with prescaler	Greater of: 40 ns or (2 TCY + 40)/ N				N = prescale value (1, 8, 64, 256)
			Asynchronous	40			ns	
OS60	Ft1	SOSCI/T1CK Oscillator Input frequency Range (oscillator enabled by setting bit TCS (T1CON<1>))		DC		50	kHz	
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40		1.75 TCY + 40		

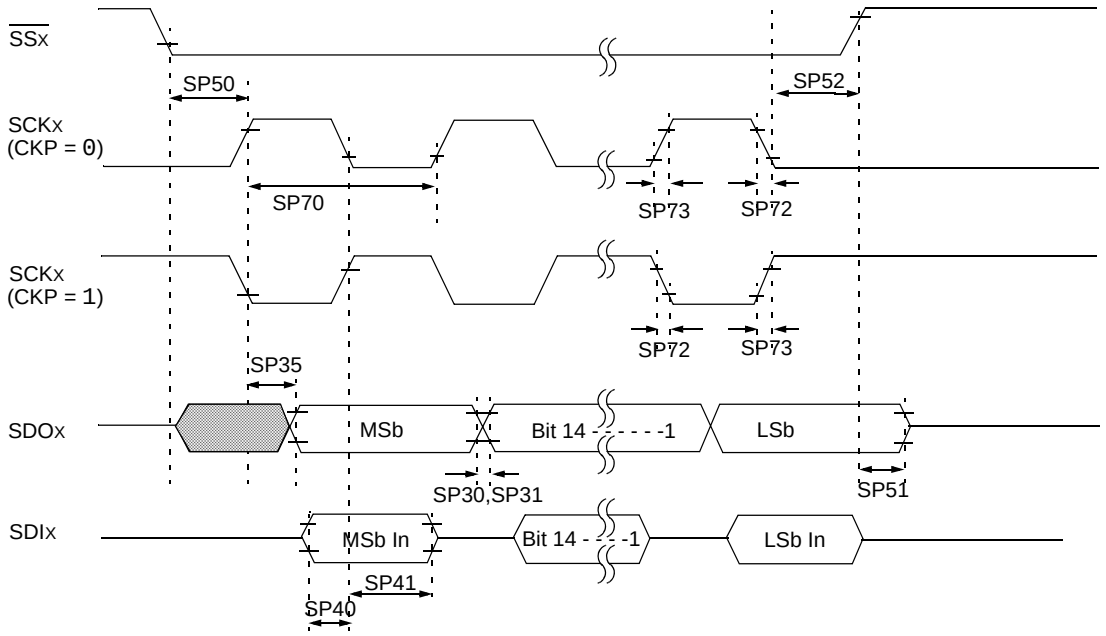
Note 1: Timer1 is a Type A.

FIGURE 22-14: SPIx SLAVE MODE (FULL-DUPLEX, CKE = **1**, CKP = **1**, SMP = **0**) TIMING CHARACTERISTICS



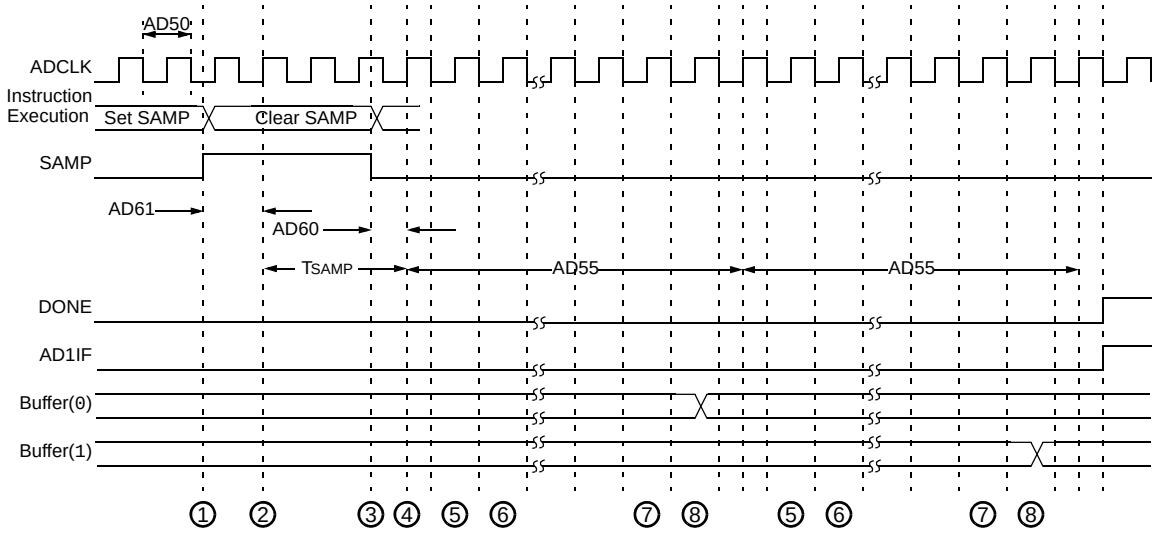
Note: Refer to Figure 22-1 for load conditions.

FIGURE 22-16: SPIx SLAVE MODE (FULL-DUPLEX, CKE = **0**, CKP = **0**, SMP = **0**) TIMING CHARACTERISTICS



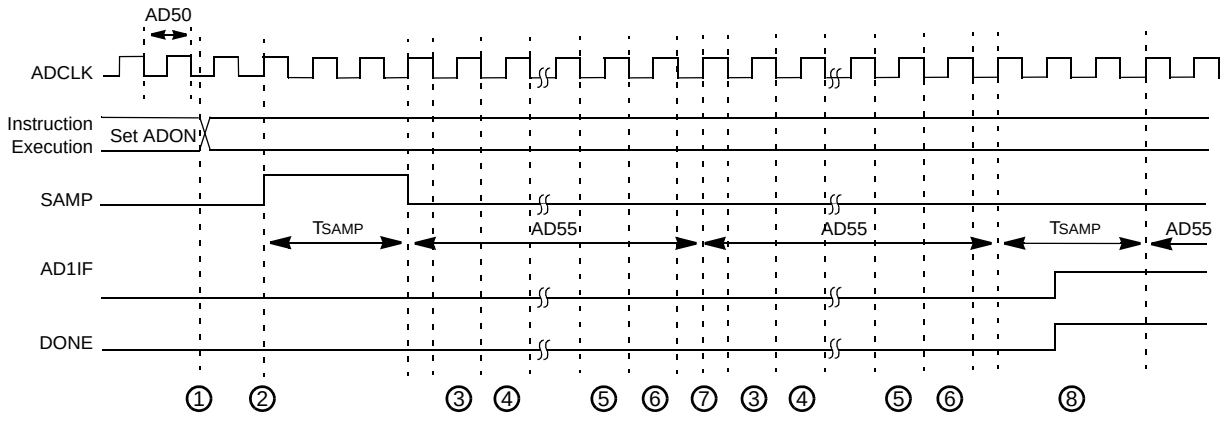
Note: Refer to Figure 22-1 for load conditions.

FIGURE 22-22: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = **01**, SIMSAM = **0**, ASAM = **0**, SSRC<2:0> = **000**)



1. Software sets AD1CON. SAMP to start sampling.
2. Sampling starts after discharge period. T SAMP is described in Section 16. Analog-to-Digital Converter (ADC) (DS70183) in the *"dsPIC33F/PIC24H Family Reference Manual"*.
3. Software clears AD1CON. SAMP to start conversion.
4. Sampling ends, conversion sequence starts.
5. Convert bit 9.
6. Convert bit 8.
7. Convert bit 0.
8. One T AD for end of conversion.

FIGURE 22-23: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = **01**, SIMSAM = **0**, ASAM = **1**, SSRC<2:0> = **111**, SAMC<4:0> = **00001**)



1. Software sets ADxCON. ADON to start AD operation.
2. Sampling starts after discharge period. T SAMP is described in Section 16. Analog-to-Digital Converter (ADC) (DS70183) in the *"dsPIC33F/PIC24H Family Reference Manual"*. Refer to the Microchip web site for the latest family reference manual sections.
3. Convert bit 9.
4. Convert bit 8.
5. Convert bit 0.
6. One T AD for end of conversion.
7. Begin conversion of next channel.
8. Sample for time specified by SAMC<4:0>.

NOTES:

Revision C (May 2008)

This revision includes minor typographical and formatting changes throughout the data sheet text.

The major changes are referenced by their respective section in the following table.

TABLE 23-1: MAJOR SECTION UPDATES

Section Name	Update Description
High-Performance, 16-Bit Digital Signal Controllers	Added SSOP to list of available 28-pin packages (see Packaging: and Table 1). Added External Interrupts column to Remappable Peripherals in the Controller Families table and Note 2 (see Table 1). Added Note 1 to all pin diagrams, which references RPn pin usage by remappable peripherals (see Pin Diagrams).
Section 1.0 Device Overview	Changed Capture Input pin names from IC0-IC1 to IC1-IC2 and updated description for AVDD (see Table 1-1).
Section 3.0 Memory Organization	Updated Reset values for the following SFRs: IPC0, IPC2-IPC7, IPC16, and INTTREG (see Table 3-4). The following changes were made to the ADC1 Register Maps: Updated the bit range for AD1CON3 from ADCS<5:0> to ADCS<7:0>) (see Table 3-14 and Table 3-15). Added Bit 6 (PCFG7) and Bit 7 (PCFG6) names to AD1PCFGL (Table 3-14). Added Bit 6 (CSS7) and Bit 7 (CSS6) names to AD1CSSL (see Table 3-14). Changed Bit 5 and Bit 4 in AD1CSSL to unimplemented (see Table 3-14). Updated the Reset value for CLKDIV in the System Control Register Map (see Table 3-19).
Section 4.0 Flash Program Memory	Updated Section 4.3 Programming Operations with programming time formula.
Section 5.0 Resets	Entire section was replaced to maintain consistency with other PIC24H data sheets.
Section 7.0 Oscillator Configuration	Removed the first sentence of the third clock source item (External Clock) in Section 7.1.1.2 Primary Updated the default bit values for DOZE and FRCDIV in the Clock Divisor Register (see Register 7-2). Added the center frequency in the OSCTUN register for the FRC Tuning bits (TUN<5:0>) value 011111 and updated the center frequency for bits value 011110 (see Register 7-4)
Section 8.0 Power-Saving Features	Added the following two registers: PMD1: Peripheral Module Disable Control Register 1 PMD2: Peripheral Module Disable Control Register 2
Section 9.0 I/O Ports	Added paragraph and Table 9-1 to Section 9.1.1 Open-Drain Configuration , which provides details on I/O pins and their functionality. Removed the following sections, which are now available in the related section of the *"PIC24H Family Reference Manual"*: 9.4.2 Available Peripherals 9.4.3.3 Mapping 9.4.5 Considerations for Peripheral Pin Selection
Section 13.0 Output Compare	Replaced sections 13.1, 13.2, and 13.3 and related figures and tables with entirely new content.

TABLE 23-1: MAJOR SECTION UPDATES

Section Name	Update Description
Section 22.0 Packaging Information	Added 28-lead SSOP package marking information.
Product Identification System	Added Plastic Shrink Small Outline (SSOP) package information.