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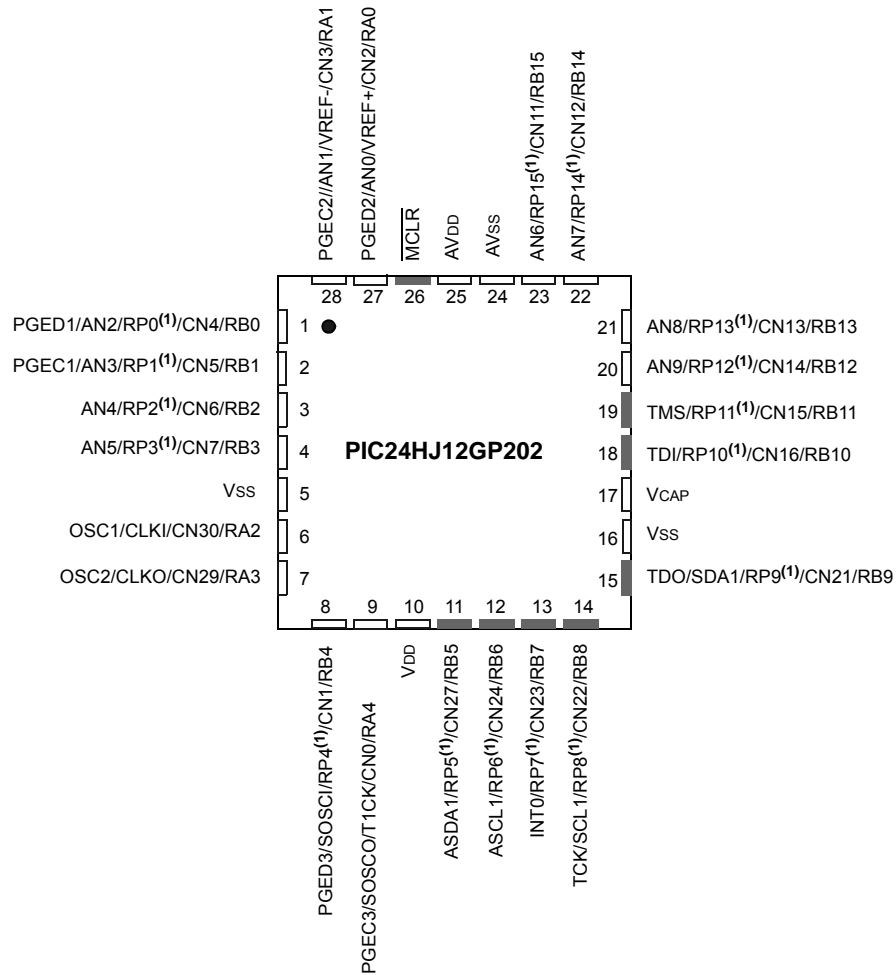
Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPS
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj12gp202-i-ss

Pin Diagrams (Continued)

28-Pin QFN⁽²⁾

■ = Pins are up to 5V tolerant



Note 1: The RPN pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.

2: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the PIC24HJ12GP201/202 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “*dsPIC33F/PIC24H Family Reference Manual*”, which is available from the Microchip website (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the PIC24HJ12GP201/202 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins (even if ADC module is not used) (see **Section 2.2 “Decoupling Capacitors”**)
- VCAP (see **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”**)
- MCLR pin (see **Section 2.4 “Master Clear (MCLR) Pin”**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 “ICSP Pins”**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 “External Oscillator Pins”**)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD, and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 μF (100 nF), 10-20V. This capacitor should be a low-ESR and have a resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the microcontroller. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the microcontroller pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

TABLE 4-16: PORTA REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	02C2	—	—	—	—	—	—	—	—	—	—	—	RA4	RA3	RA2	RA1	RA0	xxxx
LATA	02C4	—	—	—	—	—	—	—	—	—	—	—	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
ODCA	02C6	—	—	—	—	—	—	—	—	—	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: PORTB REGISTER MAP FOR PIC24HJ12GP202

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02CA	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CC	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	02CE	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: PORTB REGISTER MAP FOR PIC24HJ12GP201

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	—	—	—	—	TRISB9	TRISB8	TRISB7	—	—	TRISB4	—	—	TRISB1	TRISB0	C393
PORTB	02CA	RB15	RB14	—	—	—	—	RB9	RB8	RB7	—	—	RB4	—	—	RB1	RB0	xxxx
LATB	02CC	LATB15	LATB14	—	—	—	—	LATB9	LATB8	LATB7	—	—	LATB4	—	—	LATB1	LATB0	xxxx
ODCB	02CE	ODCB15	ODCB14	—	—	—	—	ODCB9	ODCB8	ODCB7	—	—	ODCB4	—	—	ODCB1	ODCB0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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9.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions
- The WDT is automatically cleared
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 9.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the `PWRSVAV` instruction, or the first instruction in the ISR.

9.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSVAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

9.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this may not be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (`CLKDIV<11>`). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (`CLKDIV<14:12>`). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (`CLKDIV<15>`). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the UART module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the UART module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

9.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific PIC24H variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

TABLE 10-2: OUTPUT SELECTION FOR REMAPPABLE PIN (RPn)

Function	RPnR<4:0>	Output Name
NULL	00000	RPn tied to default port pin
U1TX	00011	RPn tied to UART1 Transmit
U1RTS	00100	RPn tied to UART1 Ready To Send
SDO1	00111	RPn tied to SPI1 Data Output
SCK1OUT	01000	RPn tied to SPI1 Clock Output
SS1OUT	01001	RPn tied to SPI1 Slave Select Output
OC1	10010	RPn tied to Output Compare 1
OC2	10011	RPn tied to Output Compare 2

10.4.3 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24H devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit pin select lock

10.4.3.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 0x46 to OSCCON<7:0>.
2. Write 0x57 to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

Note: MPLAB® C30 provides built-in C language functions for unlocking the OSCCON register:

```
__builtin_write_OSCCONL(value)
__builtin_write_OSCCONH(value)
```

See MPLAB IDE Help for more information.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the peripheral pin selects to be configured with a single unlock sequence followed by an update to all control registers, then locked with a second lock sequence.

10.4.3.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset will be triggered.

10.4.3.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows user applications unlimited access (with the proper use of the unlock sequence) to the peripheral pin select registers.

10.5 Peripheral Pin Select Registers

The PIC24HJ12GP201/202 devices implement 17 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (9)
- Output Remappable Peripheral Registers (8)

Note: Input and Output Register values can only be changed if OSCCON<IOLOCK> = 0. See **Section 10.4.3.1 “Control Register Lock”** for a specific command sequence.

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REGISTER 10-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T3CKR<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T2CKR<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **T3CKR<4:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn pin bits

11111 = Input tied to Vss

01111 = Input tied to RP15

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **T2CKR<4:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits

11111 = Input tied to Vss

01111 = Input tied to RP15

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

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REGISTER 10-5: RPINR10: PERIPHERAL PIN SELECT INPUT REGISTERS 10

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	IC8R<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	IC7R<4:0>				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13

Unimplemented: Read as '0'

bit 12-8

IC8R<4:0>: Assign Input Capture 8 (IC8) to the corresponding pin RPn pin bits

11111 = Input tied to Vss

01111 = Input tied to RP15

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

bit 7-5

Unimplemented: Read as '0'

bit 4-0

IC7R<4:0>: Assign Input Capture 7 (IC7) to the corresponding pin RPn pin bits

11111 = Input tied to Vss

01111 = Input tied to RP15

•

•

•

00001 = Input tied to RP1

00000 = Input tied to RP0

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NOTES:

REGISTER 17-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 4	URXINV: Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH: High Baud Rate Enable bit 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	STSEL: Stop Bit Selection bit 1 = Two Stop bits 0 = One Stop bit

- Note 1:** Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).

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TABLE 19-2: PIC24HJ12GP201/202 CONFIGURATION BITS DESCRIPTION

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection 1 = Boot segment may be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size x11 = No Boot program Flash segment Boot space is 256 Instruction Words (except interrupt vectors) 110 = Standard security; boot program Flash segment ends at 0x0003FE 010 = High security; boot program Flash segment ends at 0x0003FE Boot space is 768 Instruction Words (except interrupt vectors) 101 = Standard security; boot program Flash segment, ends at 0x0007FE 001 = High security; boot program Flash segment ends at 0x0007FE Boot space is 1792 Instruction Words (except interrupt vectors) 100 = Standard security; boot program Flash segment ends at 0x000FFE 000 = High security; boot program Flash segment ends at 0x000FFE
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bit 11 = User program memory is not code-protected 10 = Standard security 0x = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	Two-speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) oscillator with postscaler 110 = Internal Fast RC (FRC) oscillator with divide-by-16 101 = LPRC oscillator 100 = Secondary (LP) oscillator 011 = Primary (XT, HS, EC) oscillator with PLL 010 = Primary (XT, HS, EC) oscillator 001 = Internal Fast RC (FRC) oscillator with PLL 000 = FRC oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, fail-safe clock monitor is disabled 01 = Clock switching is enabled, fail-safe clock monitor is disabled 00 = Clock switching is enabled, fail-safe clock monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCI0FNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is clock output 0 = OSC2 is general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary oscillator disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode

TABLE 20-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD f	$f = f + WREG$	1	1	C,DC,N,OV,Z
		ADD f, WREG	$WREG = f + WREG$	1	1	C,DC,N,OV,Z
		ADD #lit10, Wn	$Wd = lit10 + Wd$	1	1	C,DC,N,OV,Z
		ADD Wb, Ws, Wd	$Wd = Wb + Ws$	1	1	C,DC,N,OV,Z
		ADD Wb, #lit5, Wd	$Wd = Wb + lit5$	1	1	C,DC,N,OV,Z
2	ADDC	ADDC f	$f = f + WREG + (C)$	1	1	C,DC,N,OV,Z
		ADDC f, WREG	$WREG = f + WREG + (C)$	1	1	C,DC,N,OV,Z
		ADDC #lit10, Wn	$Wd = lit10 + Wd + (C)$	1	1	C,DC,N,OV,Z
		ADDC Wb, Ws, Wd	$Wd = Wb + Ws + (C)$	1	1	C,DC,N,OV,Z
		ADDC Wb, #lit5, Wd	$Wd = Wb + lit5 + (C)$	1	1	C,DC,N,OV,Z
3	AND	AND f	$f = f .AND. WREG$	1	1	N,Z
		AND f, WREG	$WREG = f .AND. WREG$	1	1	N,Z
		AND #lit10, Wn	$Wd = lit10 .AND. Wd$	1	1	N,Z
		AND Wb, Ws, Wd	$Wd = Wb .AND. Ws$	1	1	N,Z
		AND Wb, #lit5, Wd	$Wd = Wb .AND. lit5$	1	1	N,Z
4	ASR	ASR f	$f = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR f, WREG	$WREG = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR Ws, Wd	$Wd = \text{Arithmetic Right Shift } Ws$	1	1	C,N,OV,Z
		ASR Wb, Wns, Wnd	$Wnd = \text{Arithmetic Right Shift } Wb \text{ by } Wns$	1	1	N,Z
		ASR Wb, #lit5, Wnd	$Wnd = \text{Arithmetic Right Shift } Wb \text{ by } lit5$	1	1	N,Z
5	BCLR	BCLR f, #bit4	Bit Clear f	1	1	None
		BCLR Ws, #bit4	Bit Clear Ws	1	1	None
6	BRA	BRA C, Expr	Branch if Carry	1	1 (2)	None
		BRA GE, Expr	Branch if greater than or equal	1	1 (2)	None
		BRA GEU, Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA GT, Expr	Branch if greater than	1	1 (2)	None
		BRA GTU, Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA LE, Expr	Branch if less than or equal	1	1 (2)	None
		BRA LEU, Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA LT, Expr	Branch if less than	1	1 (2)	None
		BRA LTU, Expr	Branch if unsigned less than	1	1 (2)	None
		BRA N, Expr	Branch if Negative	1	1 (2)	None
		BRA NC, Expr	Branch if Not Carry	1	1 (2)	None
		BRA NN, Expr	Branch if Not Negative	1	1 (2)	None
		BRA NZ, Expr	Branch if Not Zero	1	1 (2)	None
		BRA Expr	Branch Unconditionally	1	2	None
		BRA Z, Expr	Branch if Zero	1	1 (2)	None
BRA Wn	Computed Branch	1	2	None		
7	BSET	BSET f, #bit4	Bit Set f	1	1	None
		BSET Ws, #bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C Ws, Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z Ws, Wb	Write Z bit to Ws<Wb>	1	1	None
9	BTG	BTG f, #bit4	Bit Toggle f	1	1	None
		BTG Ws, #bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC f, #bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC Ws, #bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS f, #bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS Ws, #bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None

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TABLE 22-17: PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8	MHz	ECPLL, HSPPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency	100	—	200	MHz	—
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	mS	—
OS53	DCLK	CLKO Stability (Jitter) ⁽²⁾	-3	0.5	3	%	Measured over 100 ms period

- Note 1:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$\text{Peripheral Clock Jitter} = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{\text{Peripheral Bit Rate Clock}}\right)}}$$

For example: Fosc = 32 MHz, DCLK = 3%, SPI bit rate clock, (i.e., SCK) is 2 MHz.

$$\text{SPI SCK Jitter} = \left[\frac{DCLK}{\sqrt{\left(\frac{32 \text{ MHz}}{2 \text{ MHz}}\right)}} \right] = \left[\frac{3\%}{\sqrt{16}} \right] = \left[\frac{3\%}{4} \right] = 0.75\%$$

TABLE 22-18: AC CHARACTERISTICS: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
Internal FRC Accuracy @ 7.3728 MHz⁽¹⁾							
F20a	FRC	-2	—	+2	%	-40°C ≤TA ≤+85°C	VDD = 3.0-3.6V
F20b	FRC	-5	—	+5	%	-40°C ≤TA ≤+125°C	VDD = 3.0-3.6V

- Note 1:** Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.

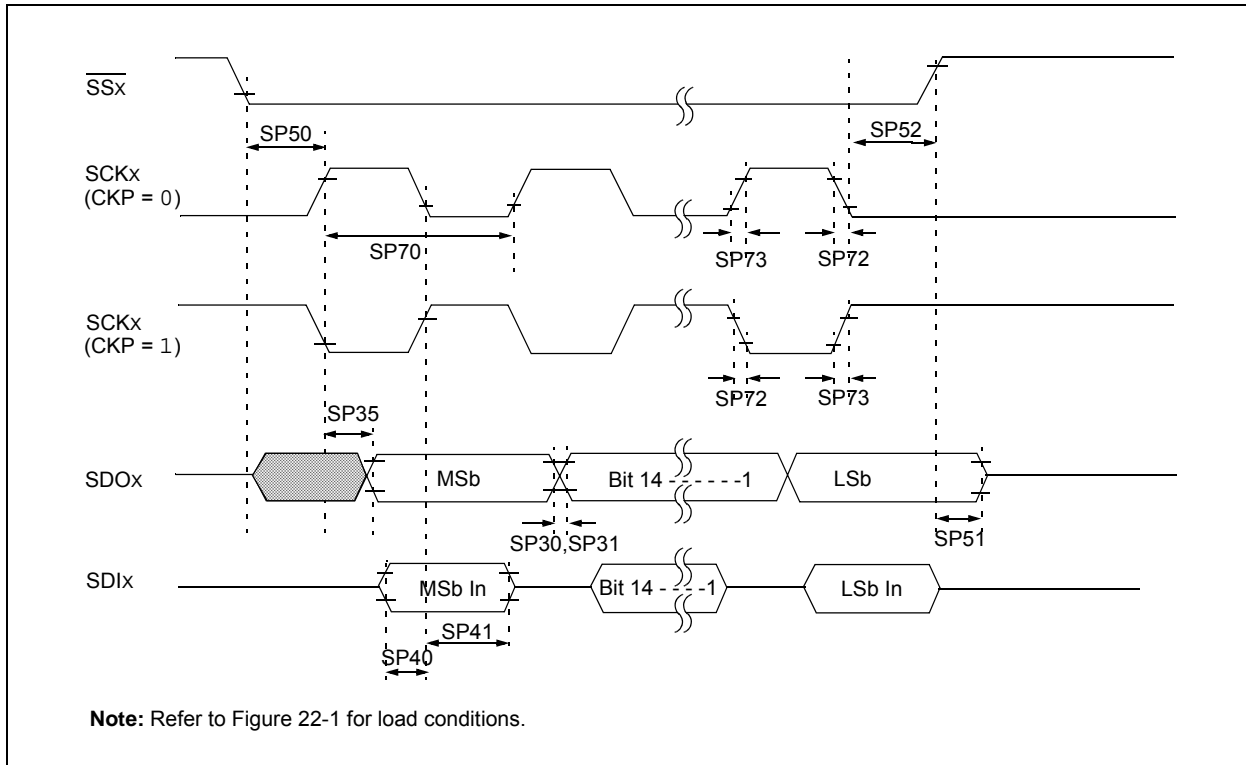
TABLE 22-19: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
LPRC @ 32.768 kHz^(1,2)							
F21a	LPRC	-20	±6	+20	%	-40°C ≤TA ≤+85°C	VDD = 3.0-3.6V
F21b	LPRC	-70	—	+70	%	-40°C ≤TA ≤+125°C	VDD = 3.0-3.6V

- Note 1:** Change of LPRC frequency as VDD changes.
- 2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 19.4 “Watchdog Timer (WDT)”** for more information.

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FIGURE 22-15: SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



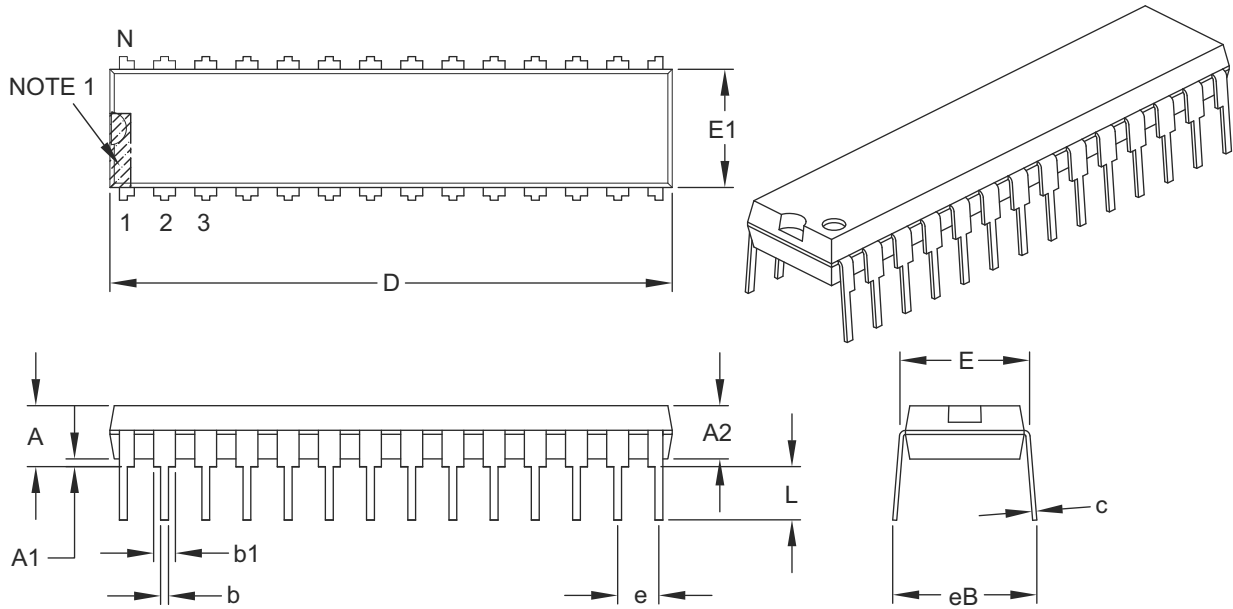
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NOTES:

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28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

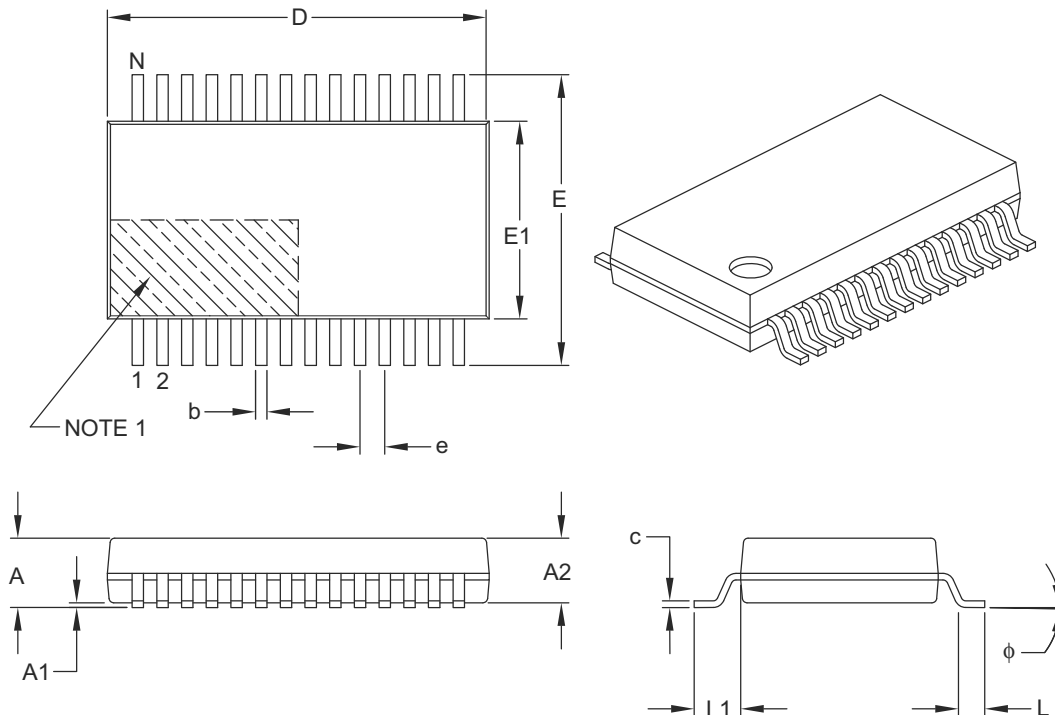
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

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28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

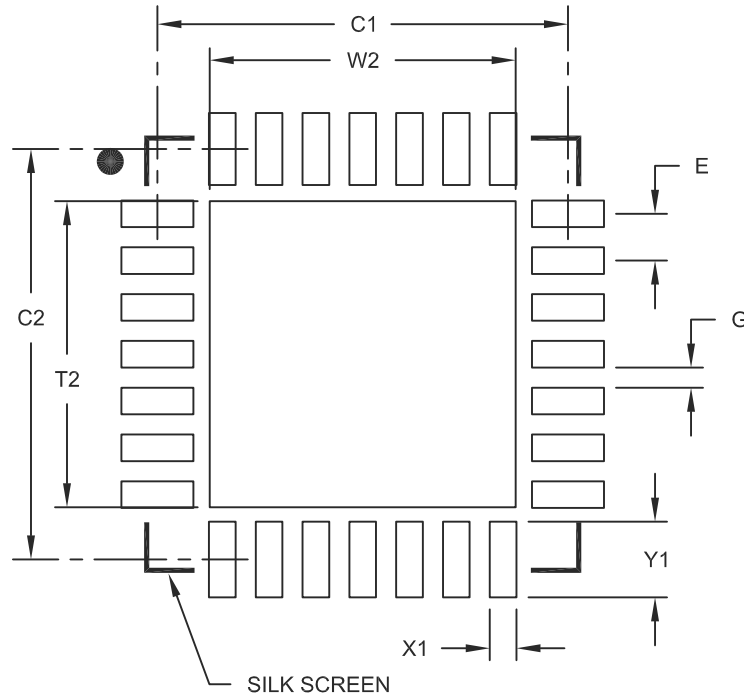
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

PIC24HJ12GP201/202

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

PIC24HJ12GP201/202

Revision E (July 2011)

This revision includes formatting changes and minor typographical throughout the data sheet text.

Global changes include:

- Removed Preliminary marking from the footer
- Updated all family reference manual information in the note boxes located at the beginning of most chapters
- Changed all instances of VCAP/VDDCORE to VCAP

All other major changes are referenced by their respective section in the following table.

TABLE 23-3: MAJOR SECTION UPDATES

Section Name	Update Description
Section 2.0 “Guidelines for Getting Started with 16-bit Microcontrollers”	Changed the title of section 2.3 to Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)” . Updated the second paragraph in Section 2.9 “Unused I/Os” .
Section 4.0 “Memory Organization”	Revised the data memory implementation value in the third paragraph of Section 4.2 “Data Address Space” . Updated the All Resets values for TMR1, TMR2, and TMR3 in the Timer Register Map (see Table 4-5).
Section 8.0 “Oscillator Configuration”	Added Note 3 to the Oscillator Control Register (see Register 8-1). Added Note 2 to the Clock Divisor Register (see Register 8-2). Added Note 1 to the PLL Feedback Divisor Register (see Register 8-3). Added Note 2 to the FRC Oscillator Tuning Register (see Register 8-4).
Section 10.0 “I/O Ports”	Revised the second paragraph in Section 10.1.1 “Open-Drain Configuration” .
Section 14.0 “Output Compare”	Updated the Output Compare Module Block Diagram (see Figure 14-1).
Section 17.0 “Universal Asynchronous Receiver Transmitter (UART)”	Revised the UART module Baud Rate features, replacing both items with “Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS”.
Section 19.0 “Special Features”	Revised all paragraphs in Section 19.1 “Configuration Bits” . Updated the Device Configuration Register Map (see Table 19-1). Added the RTSP Effect column in the Configuration Bits Description (see Table 19-2).

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