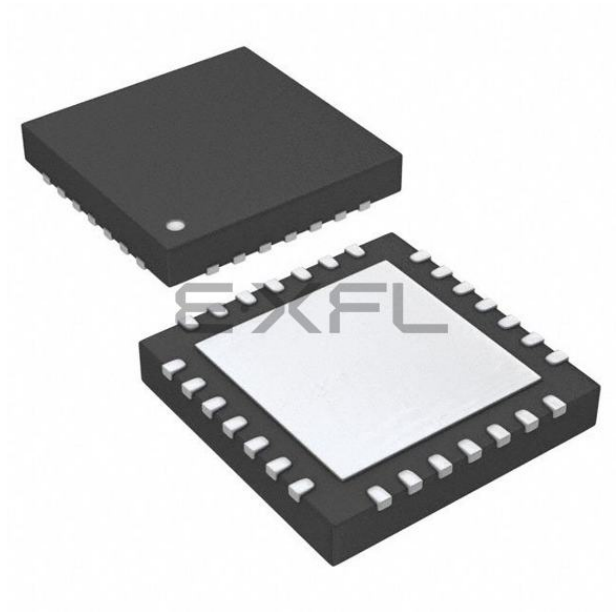
# Microchip Technology - PIC24HJ12GP202T-I/ML Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 40 MIPs |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 12KB (4K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 10x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24hj12gp202t-i-ml |

## PIC24HJ12GP201/202 Product Families

The device names, pin counts, memory sizes and peripheral availability of each family are listed below, followed by their pinout diagrams.

**TABLE 1: PIC24HJ12GP201/202 CONTROLLER FAMILIES**

| Device | Pins | Program Flash Memory (Kbyte) | RAM (Kbyte) | Remappable Peripherals | | | | | | | 10-Bit/12-Bit ADC | $I^2C$™ | I/O Pins (Max) | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Remappable Pins | 16-bit Timer | Input Capture | Output Compare Std. PWM | UART | External Interrupts(2) | SPI | | | | |
| PIC24HJ12GP201 | 18 | 12 | 1 | 8 | 3(1) | 4 | 2 | 1 | 3 | 1 | 1 ADC, 6 ch | 1 | 13 | PDIP SOIC |
| PIC24HJ12GP202 | 28 | 12 | 1 | 16 | 3(1) | 4 | 2 | 1 | 3 | 1 | 1 ADC, 10 ch | 1 | 21 | SPDIP SOIC SSOP QFN |

**Note 1:** Only two out of three timers are remappable.

**2:** Only two out of three interrupts are remappable.

### 4.2.5 SOFTWARE STACK

In addition to its use as a working register, the W15 register in the PIC24HJ12GP201/202 devices is also used as a software Stack Pointer. The Stack Pointer always points to the first available free word and grows from lower to higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 4-4. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

| **Note:** | A PC push during exception processing concatenates the SRL register to the MSB of the PC prior to the push. |
|---|---|

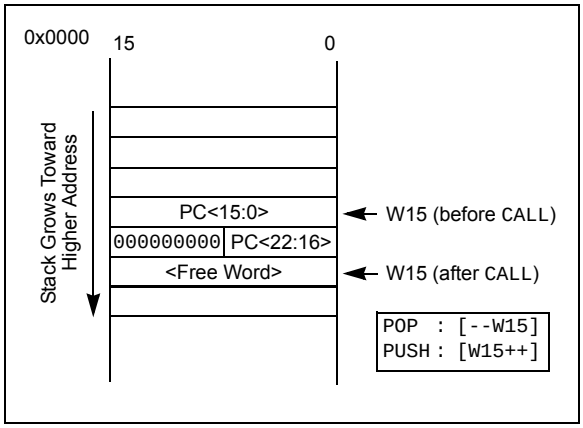
The Stack Pointer Limit register (SPLIM) associated with the Stack Pointer sets an upper address boundary for the stack. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word-aligned.

When an EA is generated using W15 as a source or destination pointer, the resulting address is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal and a push operation is performed, a stack error trap will not occur. However, the stack error trap will occur on a subsequent push operation. For example, to cause a stack error trap when the stack grows beyond address 0x0C00 in RAM, initialize the SPLIM with the value 0x0BFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800. This prevents the stack from interfering with the SFR space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

**FIGURE 4-4: CALL STACK FRAME**




### 4.2.6 DATA RAM PROTECTION FEATURE

The PIC24H product family supports Data RAM protection features that enable segments of RAM to be protected when used in conjunction with Boot and Secure Code Segment Security. BSRAM (Secure RAM segment for BS) is accessible only from the Boot Segment Flash code, when it is enabled. SSRAM (Secure RAM segment for RAM) is accessible only from the Secure Segment Flash code, when it is enabled. See Table 4-1 for an overview of the BSRAM and SSRAM SFRs.

## 4.3 Instruction Addressing Modes

The addressing modes shown in Table 4-22 form the basis of the addressing modes that are optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those provided by other instruction types.

### 4.3.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

### 4.3.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

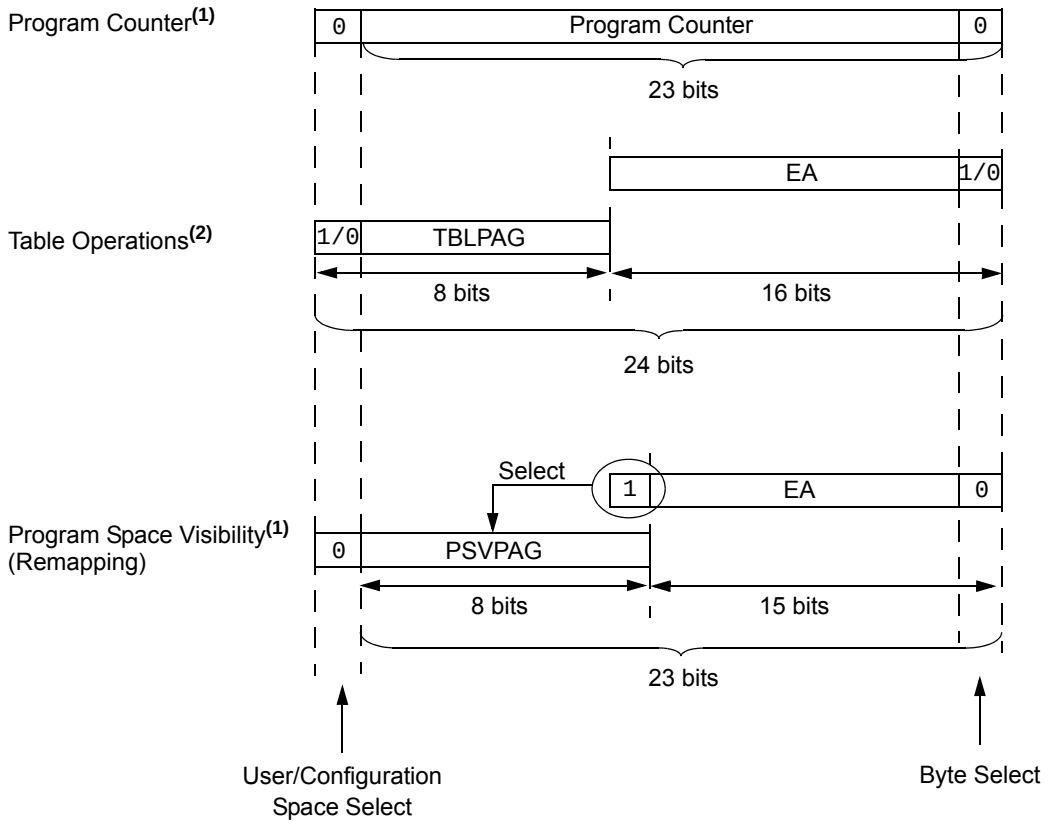
Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be register direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

| **Note:** | Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes. |
|---|---|

**FIGURE 4-5: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**




**Note 1:** The LSb of program space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.

**2:** Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)**

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | — | — | — | — | CM | VREGS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN(2) | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A configuration mismatch Reset has occurred
0 = A configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

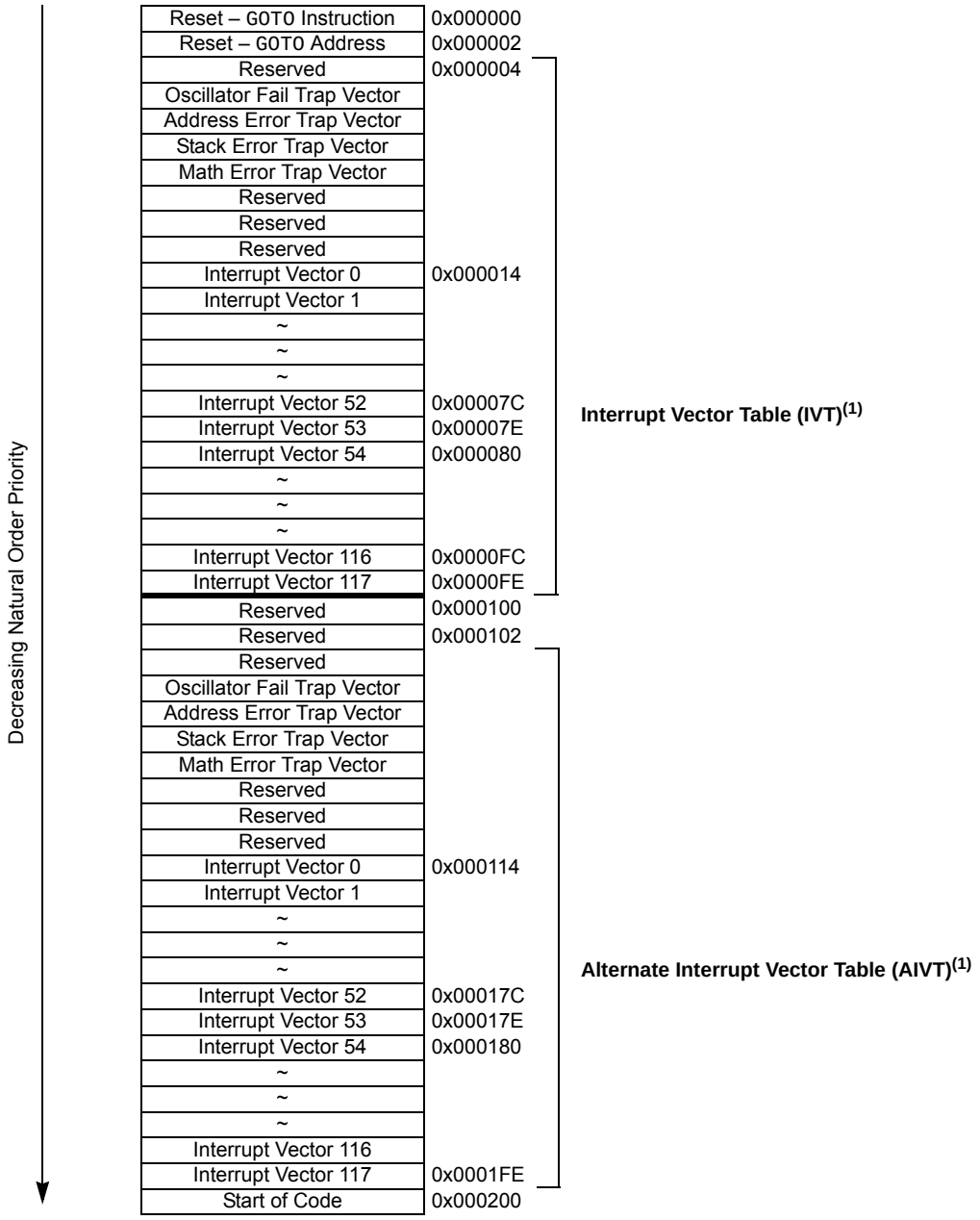
bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**FIGURE 7-1: PIC24HJ12GP201/202 INTERRUPT VECTOR TABLE**




**Note 1:** See Table 7-1 for the list of implemented interrupt vectors.

**REGISTER 7-16: IPC5: INTERRUPT PRIORITY CONTROL REGISTER 5**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC8IP<2:0> | | | — | IC7IP<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | INT1IP<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **IC8IP<2:0>:** Input Capture Channel 8 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

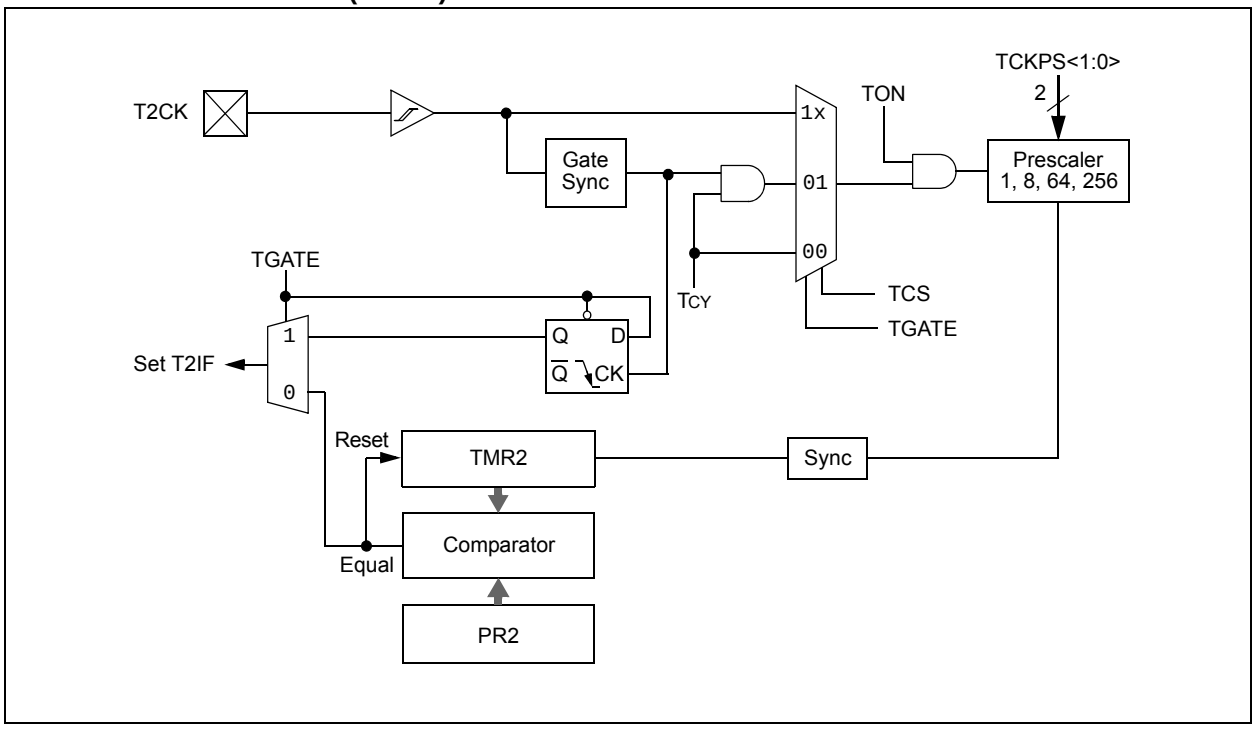
bit 10-8 **IC7IP<2:0>:** Input Capture Channel 7 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **INT1IP<2:0>:** External Interrupt 1 Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

**NOTES:**

**FIGURE 12-2: TIMER2 (16-BIT) BLOCK DIAGRAM**



**REGISTER 15-2: SPIxCON1: SPIx CONTROL REGISTER 1**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSEN(2) | CKP | MSTEN | SPRE<2:0>(3) | | | PPRE<1:0>(3) | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx pin bit (SPI Master modes only)
1 = Internal SPI clock is disabled, pin functions as I/O
0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Serial output data changes on transition from active clock state to Idle clock state (see bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (see bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin used for Slave mode
0 = $\overline{SSx}$ pin not used by module. Pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

**Note 1:** The CKE bit is not used in the Framed SPI modes. Program this bit to '0' for the Framed SPI modes (FRMEN = 1).

**2:** This bit must be cleared when FRMEN = 1.

**3:** Do not set both Primary and Secondary prescalers to a value of 1:1.

## 16.0 INTER-INTEGRATED CIRCUIT™ ($I^2C$™)

**Note 1:** This data sheet summarizes the features of the PIC24HJ12GP201/202 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Section 19. Inter-Integrated Circuit™ ($I^2C$™)"** (DS70195) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Inter-Integrated Circuit™ ($I^2C$™) module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard, with a 16-bit interface.

The $I^2C$ module has a 2-pin interface:

- The SCLx pin is clock
- The SDAx pin is data

The $I^2C$ module offers the following key features:

- $I^2C$ interface supporting both Master and Slave modes of operation
- $I^2C$ Slave mode supports 7-bit and 10-bit addresses
- $I^2C$ Master mode supports 7-bit and 10-bit addresses
- $I^2C$ port allows bidirectional transfers between master and slaves
- Serial clock synchronization for $I^2C$ port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- $I^2C$ supports multi-master operation, detects bus collision and arbitrates accordingly

### 16.1 Operating Modes

The hardware fully implements all the master and slave functions of the $I^2C$ Standard and Fast mode specifications, as well as 7-bit and 10-bit addressing.

The $I^2C$ module can operate either as a slave or a master on an $I^2C$ bus.

The following types of $I^2C$ operation are supported:

- $I^2C$ slave operation with 7-bit address
- $I^2C$ slave operation with 10-bit address
- $I^2C$ master operation with 7-bit or 10-bit address

For details about the communication sequence in each of these modes, refer to the Microchip web site (www.microchip.com) for the latest *"dsPIC33F/PIC24H Family Reference Manual"* sections.

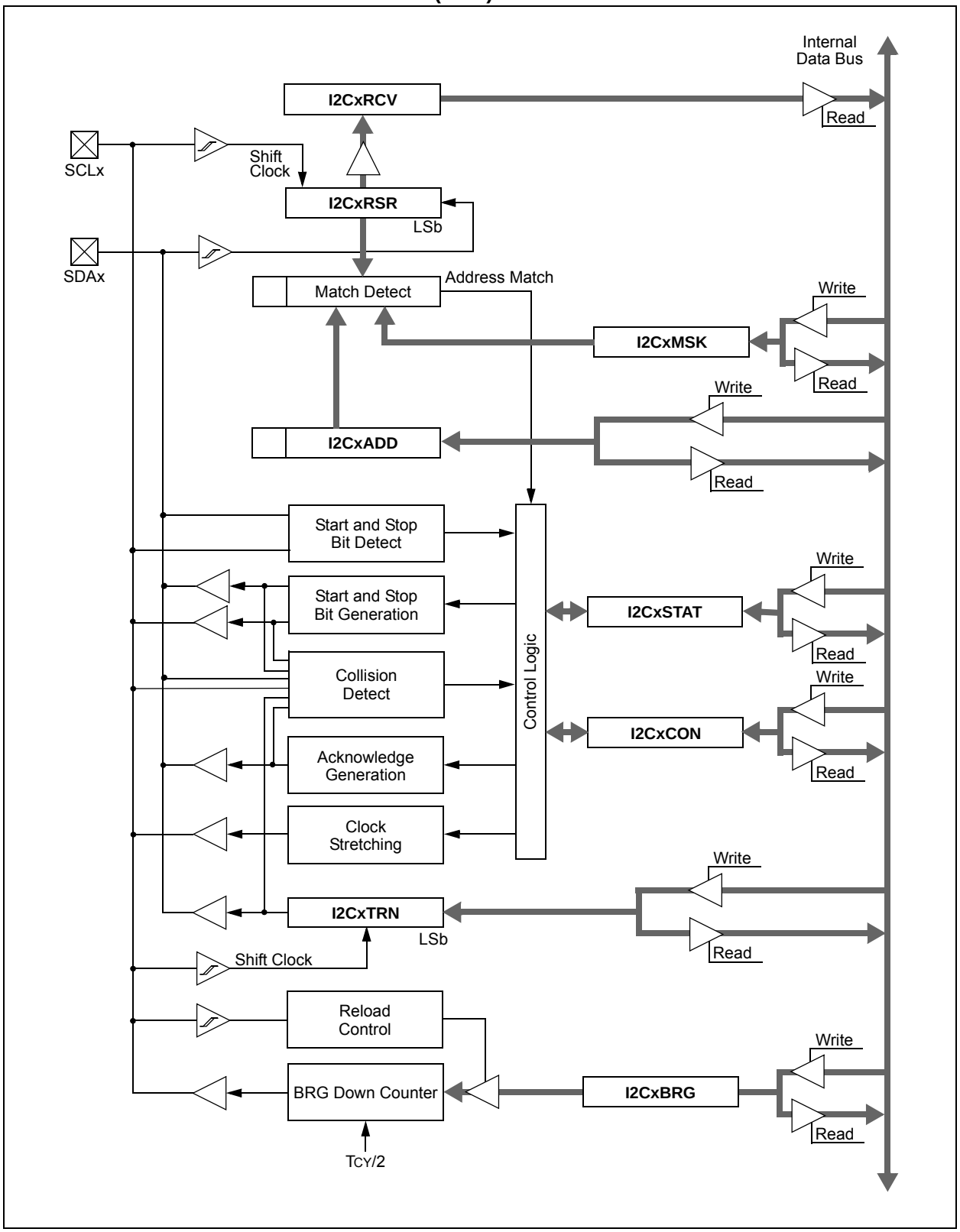
### 16.2 $I^2C$ Registers

I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CSTAT are read/write.

- I2CxRSR is the shift register used for shifting data
- I2CxRCV is the receive buffer and the register to which data bytes are written, or from which data bytes are read
- I2CxTRN is the transmit register to which bytes are written during a transmit operation
- I2CxADD register holds the slave address
- ADD10 status bit indicates 10-bit Address mode
- I2CxBRG acts as the Baud Rate Generator (BRG) reload value

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV, and an interrupt pulse is generated.

**FIGURE 16-1: I²C™ BLOCK DIAGRAM (x = 1)**



**REGISTER 17-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 4 **URXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

**Note 1:** Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

**REGISTER 17-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode enabled. If 9-bit mode is not selected, this does not take effect.
0 = Address Detect mode disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (read-only/clear-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed. Clearing a previously set OERR bit (1 →0 transition) will reset the receiver buffer and the UxRSR to the empty state.

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

**Note 1:** Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F/PIC24H Family Reference Manual"* for information on enabling the UART module for transmit operation.

**TABLE 19-2: PIC24HJ12GP201/202 CONFIGURATION BITS DESCRIPTION**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| BWRP | FBS | Immediate | Boot Segment Program Flash Write Protection<br>1 = Boot segment may be written<br>0 = Boot segment is write-protected |
| BSS<2:0> | FBS | Immediate | Boot Segment Program Flash Code Protection Size<br>X11 = No Boot program Flash segment<br><br>Boot space is 256 Instruction Words (except interrupt vectors)<br>110 = Standard security; boot program Flash segment ends at 0x0003FE<br>010 = High security; boot program Flash segment ends at 0x0003FE<br><br>Boot space is 768 Instruction Words (except interrupt vectors)<br>101 = Standard security; boot program Flash segment, ends at 0x0007FE<br>001 = High security; boot program Flash segment ends at 0x0007FE<br><br>Boot space is 1792 Instruction Words (except interrupt vectors)<br>100 = Standard security; boot program Flash segment ends at 0x000FFE<br>000 = High security; boot program Flash segment ends at 0x000FFE |
| GSS<1:0> | FGS | Immediate | General Segment Code-Protect bit<br>11 = User program memory is not code-protected<br>10 = Standard security<br>0x = High security |
| GWRP | FGS | Immediate | General Segment Write-Protect bit<br>1 = User program memory is not write-protected<br>0 = User program memory is write-protected |
| IESO | FOSCSEL | Immediate | Two-speed Oscillator Start-up Enable bit<br>1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready<br>0 = Start-up device with user-selected oscillator source |
| FNOSC<2:0> | FOSCSEL | If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate | Initial Oscillator Source Selection bits<br>111 = Internal Fast RC (FRC) oscillator with postscaler<br>110 = Internal Fast RC (FRC) oscillator with divide-by-16<br>101 = LPRC oscillator<br>100 = Secondary (LP) oscillator<br>011 = Primary (XT, HS, EC) oscillator with PLL<br>010 = Primary (XT, HS, EC) oscillator<br>001 = Internal Fast RC (FRC) oscillator with PLL<br>000 = FRC oscillator |
| FCKSM<1:0> | FOSC | Immediate | Clock Switching Mode bits<br>1x = Clock switching is disabled, fail-safe clock monitor is disabled<br>01 = Clock switching is enabled, fail-safe clock monitor is disabled<br>00 = Clock switching is enabled, fail-safe clock monitor is enabled |
| IOL1WAY | FOSC | Immediate | Peripheral Pin Select Configuration<br>1 = Allow only one reconfiguration<br>0 = Allow multiple reconfigurations |
| OSCIOFNC | FOSC | Immediate | OSC2 Pin Function bit (except in XT and HS modes)<br>1 = OSC2 is clock output<br>0 = OSC2 is general purpose digital I/O pin |
| POSCMD<1:0> | FOSC | Immediate | Primary Oscillator Mode Select bits<br>11 = Primary oscillator disabled<br>10 = HS Crystal Oscillator mode<br>01 = XT Crystal Oscillator mode<br>00 = EC (External Clock) mode |

**TABLE 20-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|
| 47 | RCALL | RCALL Expr | Relative Call | 1 | 2 | None |
| | | RCALL Wn | Computed Call | 1 | 2 | None |
| 48 | REPEAT | REPEAT #lit14 | Repeat Next Instruction lit14 + 1 times | 1 | 1 | None |
| | | REPEAT Wn | Repeat Next Instruction (Wn) + 1 times | 1 | 1 | None |
| 49 | RESET | RESET | Software device Reset | 1 | 1 | None |
| 50 | RETFIE | RETFIE | Return from interrupt | 1 | 3 (2) | None |
| 51 | RETLW | RETLW #lit10,Wn | Return with literal in Wn | 1 | 3 (2) | None |
| 52 | RETURN | RETURN | Return from Subroutine | 1 | 3 (2) | None |
| 53 | RLC | RLC f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 54 | RLNC | RLNC f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 55 | RRC | RRC f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |
| 56 | RRNC | RRNC f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 57 | SE | SE Ws,Wnd | Wnd = sign-extended Ws | 1 | 1 | C,N,Z |
| 58 | SETM | SETM f | f = 0xFFFF | 1 | 1 | None |
| | | SETM WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM Ws | Ws = 0xFFFF | 1 | 1 | None |
| 59 | SL | SL f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL f,WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL Ws,Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL Wb,Wns,Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL Wb,#lit5,Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 60 | SUB | SUB f | f = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB f,WREG | WREG = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB #lit10,Wn | Wn = Wn – lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB Wb,Ws,Wd | Wd = Wb – Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB Wb,#lit5,Wd | Wd = Wb – lit5 | 1 | 1 | C,DC,N,OV,Z |
| 61 | SUBB | SUBB f | f = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB f,WREG | WREG = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB #lit10,Wn | Wn = Wn – lit10 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB Wb,Ws,Wd | Wd = Wb – Ws – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB Wb,#lit5,Wd | Wd = Wb – lit5 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 62 | SUBR | SUBR f | f = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR f,WREG | WREG = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR Wb,Ws,Wd | Wd = Ws – Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR Wb,#lit5,Wd | Wd = lit5 – Wb | 1 | 1 | C,DC,N,OV,Z |
| 63 | SUBBR | SUBBR f | f = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR f,WREG | WREG = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR Wb,Ws,Wd | Wd = Ws – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR Wb,#lit5,Wd | Wd = lit5 – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 64 | SWAP | SWAP.b Wn | Wn = nibble swap Wn | 1 | 1 | None |
| | | SWAP Wn | Wn = byte swap Wn | 1 | 1 | None |
| 65 | TBLRDH | TBLRDH Ws,Wd | Read Prog<23:16> to Wd<7:0> | 1 | 2 | None |

**TABLE 22-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(5,8) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, and SOSCO |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(6,7,8) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, SOSCI, SOSCO, and digital 5V-tolerant designated pins |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(9) | — | +20(9) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins<br>( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** See **"Pin Diagrams"** for a list of 5V tolerant pins.

**5:** VIL source < (VSS – 0.3). Characterized but not tested.

**6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

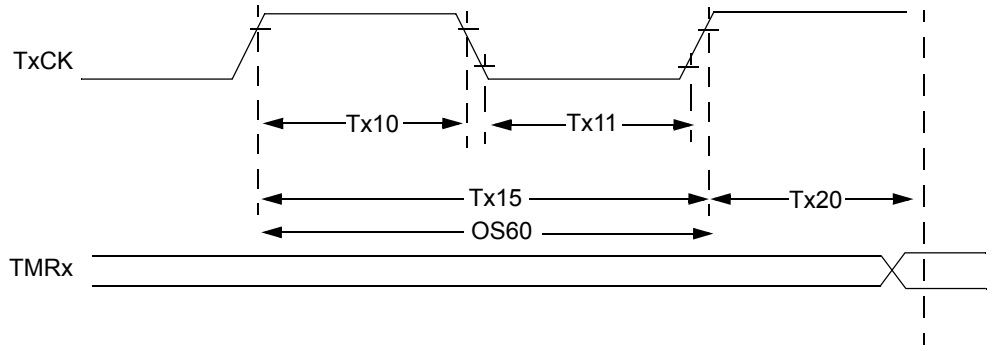
**7:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

**8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**10:** These parameters are characterized, but not tested.

**FIGURE 22-5: TIMER1, 2, 3 AND 4 EXTERNAL CLOCK TIMING CHARACTERISTICS**



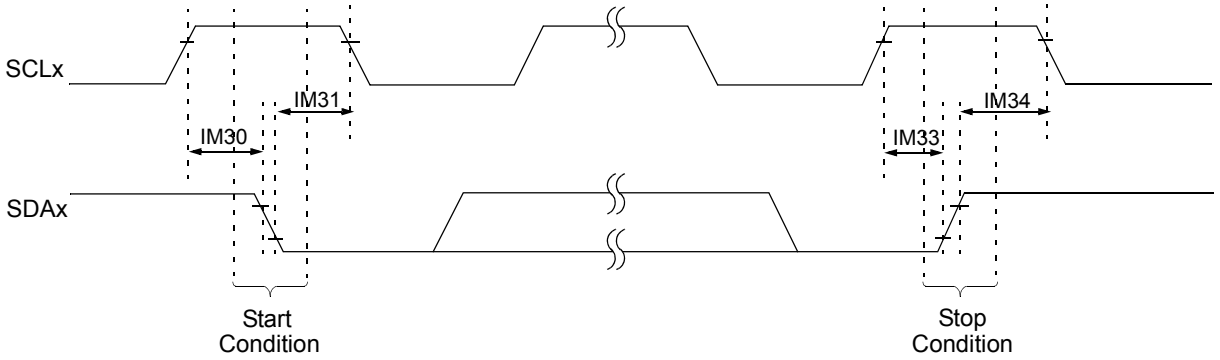

**Note:** Refer to Figure 22-1 for load conditions.

**TABLE 22-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous, no prescaler | TCY + 20 | — | — | ns | Must also meet parameter TA15. N = prescale value (1, 8, 64, 256) |
| | | | Synchronous, with prescaler | (TCY + 20)/N | — | — | ns | |
| | | | Asynchronous | 20 | — | — | ns | |
| TA11 | TTXL | TxCK Low Time | Synchronous, no prescaler | (TCY + 20) | — | — | ns | Must also meet parameter TA15. N = prescale value (1, 8, 64, 256) |
| | | | Synchronous, with prescaler | (TCY + 20)/N | — | — | ns | |
| | | | Asynchronous | 20 | — | — | ns | |
| TA15 | TTXP | TxCK Input Period | Synchronous, no prescaler | 2 TCY + 40 | — | — | ns | — |
| | | | Synchronous, with prescaler | Greater of: 40 ns or (2 TCY + 40)/ N | — | — | — | N = prescale value (1, 8, 64, 256) |
| | | | Asynchronous | 40 | — | — | ns | — |
| OS60 | Ft1 | SOSCI/T1CK Oscillator Input frequency Range (oscillator enabled by setting bit TCS (T1CON<1>)) | | DC | — | 50 | kHz | — |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | | 1.75 TCY + 40 | — | — |

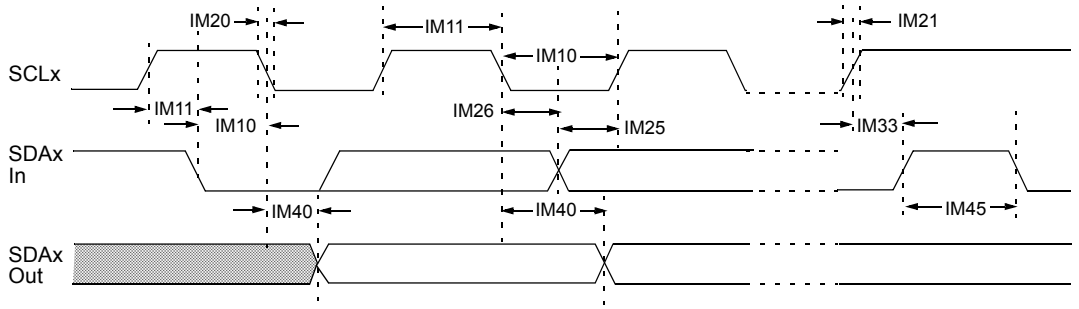
**Note 1:** Timer1 is a Type A.

**FIGURE 22-17: I²Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 22-1 for load conditions.

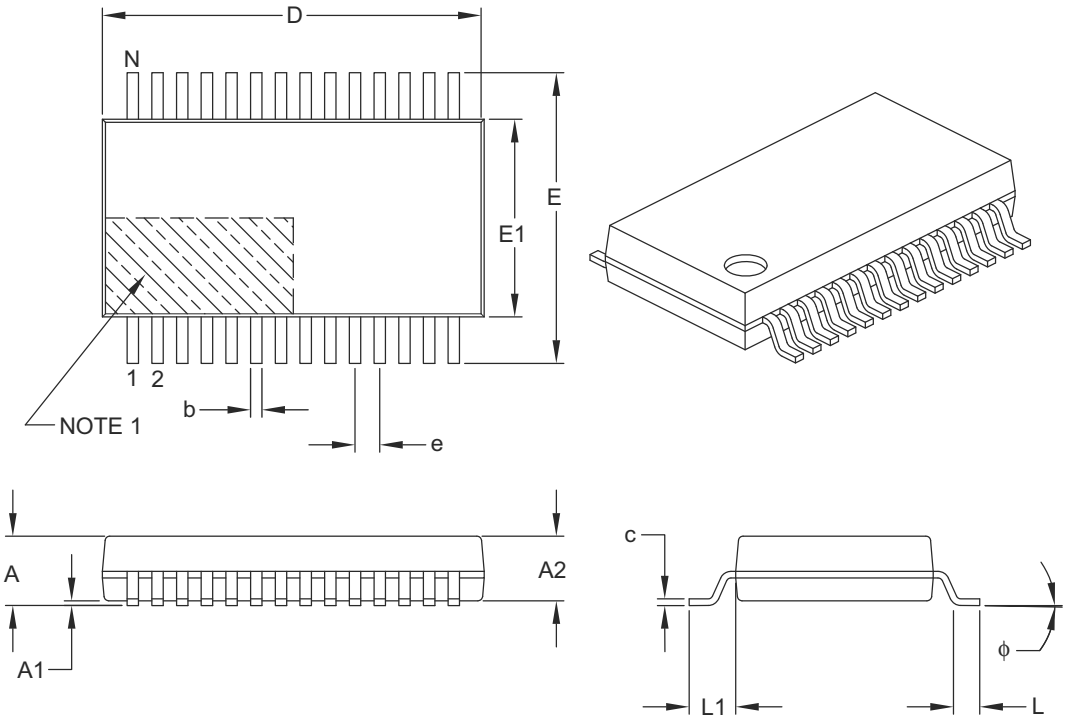
**FIGURE 22-18: I²Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 22-1 for load conditions.

## 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

## APPENDIX A: REVISION HISTORY

**Revision A (February 2007)**

This is the initial released version of this document.

**Revision B (May 2007)**

This revision includes the following corrections and updates:

- Minor typographical and formatting corrections throughout the data sheet text.
- New content:
  - Addition of bullet item (16-word conversion result buffer) (see **Section 17.1 “Key Features”**)
- Figure update:
  - Oscillator System Diagram (see Figure 7-1)
  - WDT Block Diagram (see Figure 18-2)
- Equation update:
  - Serial Clock Rate (see Equation 15-1)
- Register updates:
  - Clock Divisor Register (see Register 7-2)
  - PLL Feedback Divisor Register (see Register 7-3)
  - Peripheral Pin Select Input Registers (see Register 9-1 through Register 9-9)
  - ADC1 Input Channel 1, 2, 3 Select Register (see Register 17-4)
  - ADC1 Input Channel 0 Select Register (see Register 17-5)
- Table updates:
  - CNEN2 (see Table 3-2 and Table 3-3)
  - Reset Flag Bit Operation (see Table 5-1)
  - Configuration Bit Values for Clock Operation (see Table 7-1)
- Operation value update:
  - IOLOCK set/clear operation (see **Section 9.4.3.1 “Control Register Lock”**)
- The following tables in **Section 21.0 “Electrical Characteristics”** have been updated with preliminary values:
  - Updated Max MIPS for -40°C to +125°C Temp Range (see Table 21-1)
  - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-5)
  - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-6)
  - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-7)
  - Added new parameters for +40°C and updated Typical and Max values for most parameters (see Table 21-8)
  - Updated parameter DI51, added parameter DI51a (see Table 21-9)
  - Added Note 1 (see Table 21-11)
  - Updated parameter OS30 (see Table 21-16)
  - Updated parameter OS52 (see Table 21-17)
  - Updated parameter F20, added Note 2 (see Table 21-18)
  - Updated parameter TA15 (see Table 21-22)
  - Updated parameter TB15 (see Table 21-23)
  - Updated parameter TC15 (see Table 21-24)
  - Updated parameters AD05, AD06, AD07, AD08, AD10, and AD11; added parameters AD05a and AD06a; added Note 2; modified ADC Accuracy headings to include measurement information (see Table 21-34)
  - Separated the ADC Module Specification table in to three tables (see Table 21-34, Table 21-35, and Table 21-36)
  - Updated parameter AD50 (see Table 21-37)
  - Updated parameters AD50 and AD57 (see Table 21-38)