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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj12gp202t-i-so

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 CPU

- Note 1: This data sheet summarizes the features of the PIC24HJ12GP201/202 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Section 2. CPU" (DS70204) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip website (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The PIC24HJ12GP201/202 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and addressing modes. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M by 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction and the table instructions. Overhead-free, single-cycle program loop constructs are supported using the REPEAT instruction, which is interruptible at any point.

The PIC24HJ12GP201/202 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The PIC24HJ12GP201/202 instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, PIC24HJ12GP201/202 devices are capable of executing a data (or program data) memory read, a working register (data) read, a data memory write, and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model for the PIC24HJ12GP201/202 is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be linearly addressed as 32K words or 64 Kbytes using an Address Generation Unit (AGU). The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

3.2 Special MCU Features

The PIC24HJ12GP201/202 features a 17-bit by 17-bit, single-cycle multiplier. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication makes mixed-sign multiplication possible.

The PIC24HJ12GP201/202 supports 16/16 and 32/16 integer divide operations. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A multi-bit data shifter is used to perform up to a 16-bit, left or right shift in a single cycle.

3.4 Arithmetic Logic Unit (ALU)

The PIC24HJ12GP201/202 ALU is 16 bits wide and is capable of addition, subtraction, bit shifts, and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV), and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The PIC24HJ12GP201/202 CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.4.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several multiplication modes:

- 1. 16-bit x 16-bit signed
- 2. 16-bit x 16-bit unsigned
- 3. 16-bit signed x 5-bit (literal) unsigned
- 4. 16-bit unsigned x 16-bit unsigned
- 5. 16-bit unsigned x 5-bit (literal) unsigned
- 6. 16-bit unsigned x 16-bit signed
- 7. 8-bit unsigned x 8-bit unsigned

3.4.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 1. 32-bit signed/16-bit signed divide
- 2. 32-bit unsigned/16-bit unsigned divide
- 3. 16-bit signed/16-bit signed divide
- 4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. Sixteen-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.4.3 MULTI-BIT DATA SHIFTER

The multi-bit data shifter is capable of performing up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either a working register or a memory location.

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

6.4 External Reset (EXTR)

The external Reset is generated by driving the MCLR pin low. The MCLR pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse width will generate a Reset. Refer to **Section 22.0** "**Electrical Characteristics**" for minimum pulse width specifications. The External Reset (MCLR) Pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the MCLR Reset.

6.4.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate Reset signals to Reset multiple devices in the system. This external Reset signal can be directly connected to the MCLR pin to Reset the device when the rest of system is Reset.

6.4.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to Reset the device, the external Reset pin (MCLR) should be tied directly or resistively to VDD. In this case, the MCLR pin will not be used to generate a Reset. The external Reset pin (MCLR) does not have an internal pull-up and must not be left unconnected.

6.5 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert SYSRST, placing the device in a special Reset state. This Reset state will not reinitialize the clock. The clock source in effect prior to the RESET instruction will remain. SYSRST is released at the next instruction cycle, and the Reset vector fetch will commence.

The Software Reset (Instruction) Flag (SWR) bit in the Reset Control (RCON<6>) register is set to indicate the software Reset.

6.6 Watchdog Time-out Reset (WDTO)

Whenever a Watchdog Time-out occurs, the device will asynchronously assert SYSRST. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out Flag (WDTO) bit in the Reset Control (RCON<4>) register is set to indicate the Watchdog Reset. Refer to **Section 19.4 "Watchdog Timer (WDT)**" for more information on Watchdog Reset.

6.7 Trap Conflict Reset

If a lower-priority hard trap occurs while a higher-priority trap is being processed, a hard trap conflict Reset occurs. The hard traps include exceptions of priority level 13 through level 15, inclusive. The address error (level 13) and oscillator error (level 14) traps fall into this category.

The Trap Reset Flag (TRAPR) bit in the Reset Control (RCON<15>) register is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 "Interrupt Controller"** for more information on trap conflict Resets.

6.8 Configuration Mismatch Reset

To maintain the integrity of the peripheral pin select control registers, they are constantly monitored with shadow registers in hardware. If an unexpected change in any of the registers occur (such as cell disturbances caused by ESD or other external events), a configuration mismatch Reset occurs.

The Configuration Mismatch Flag (CM) bit in the Reset Control (RCON<9>) register is set to indicate the configuration mismatch Reset. Refer to **Section 10.0 "I/O Ports"** for more information on the configuration mismatch Reset.

Note:	The configuration mismatch feature and
	associated Reset flag is not available on
	all devices.

6.9 Illegal Condition Device Reset

An illegal condition device Reset occurs due to the following sources:

- Illegal Opcode Reset
- Uninitialized W Register Reset
- · Security Reset

The Illegal Opcode or Uninitialized W Access Reset Flag (IOPUWR) bit in the Reset Control (RCON<14>) register is set to indicate the illegal condition device Reset.

6.9.1 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that is fetched from program memory.

The illegal opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the illegal opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	Reserved
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – ADC1
22	14	0x000030	0x000130	Reserved
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	Reserved
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	Reserved
33	25	0x000046	0x000146	Reserved
34	26	0x000048	0x000148	Reserved
35	27	0x00004A	0x00014A	Reserved
36	28	0x00004C	0x00014C	Reserved
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	Reserved
39	31	0x000052	0x000152	Reserved
40	32	0x000054	0x000154	Reserved
41	33	0x000056	0x000156	Reserved
42	34	0x000058	0x000158	Reserved
43	35	0x00005A	0x00015A	Reserved
44	36	0x00005C	0x00015C	Reserved
45	37	0x00005E	0x00015E	Reserved
40	38	0x000060	UXUUU160	Reserved
47	39	0x000062	0x000162	Reserved
48	40	0x000064	0x000164	Reserved
49	41		0x000166	Reserved
50	42		0x000168	Reserved
51	43	0x00006A	0x00016A	Reserved
52	44	0x00006C	0x00016C	Reserved
53	45	0X00006E	UXUUU16E	Reserved

TABLE 7-1: INTERRUPT VECTORS

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INTOIF
DIL 7							DILU
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13	AD1IF: ADC1	Conversion C	omplete Inter	rupt Flag Statu	s bit		
	1 = Interrupt r	equest has oc	curred				
bit 12	U1TXIF: UAR	RT1 Transmitte	r Interrupt Flag	n Status bit			
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	equest has no	t occurred				
bit 11	U1RXIF: UAF	RT1 Receiver li	nterrupt Flag S	Status bit			
	1 = Interrupt r	equest has oc equest has no	curred t occurred				
bit 10	SPI1IF: SPI1	Event Interrup	t Flag Status k	oit			
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	request has no	t occurred				
bit 9	SPI1EIF: SPI	1 Fault Interru	ot Flag Status	bit			
	1 = Interrupt r 0 = Interrupt r	equest has oc equest has no	curred t occurred				
bit 8	T3IF: Timer3	Interrupt Flag	Status bit				
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	request has no	t occurred				
bit 7	T2IF: Timer2	Interrupt Flag	Status bit				
	1 = Interrupt r 0 = Interrupt r	equest has oc equest has no	currea t occurred				
bit 6	OC2IF: Outpu	ut Compare Ch	annel 2 Interr	upt Flag Status	s bit		
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	request has no	t occurred				
bit 5	IC2IF: Input C	Capture Chann	el 2 Interrupt I	-lag Status bit			
	1 = Interrupt r 0 = Interrupt r	equest nas oc equest has no	currea t occurred				
bit 4	Unimplemen	ted: Read as '	0'				
bit 3	T1IF: Timer1	Interrupt Flag	Status bit				
	1 = Interrupt r	equest has oc	curred				
	0 = Interrupt r	request has no	t occurred		1.11		
dit 2	OC1IF: Outpu	ut Compare Ch	annel 1 Interr	upt Flag Status	s dit		
	0 = Interrupt r	request has no	t occurred				
	-	-					

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
	—	INT2IF	—	—	—	—	—	
bit 15							bit 8	
R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	
IC8IF	IC7IF	—	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	
bit 7							bit 0	
Legend:								
R = Readable	hit	W = Writable	hit	U = Unimpler	mented hit read	1 as '0'		
-n = Value at F	POR	'1' = Bit is set	bit	'0' = Bit is cle	ared	x = Bit is unkr	nown	
				0 21110 010				
bit 15-14	Unimplemer	ted: Read as '	0'					
bit 13	INT2IF: Exter	rnal Interrupt 2	Flag Status b	it				
	1 = Interrupt	request has occ	curred					
h# 40.0	0 = Interrupt	request has not						
DIT 12-8	Unimplemen	nted: Read as 1						
DIT 7		capture Channe		Flag Status bit				
	1 = Interrupt 0 = Interrupt	request has oct	toccurred					
bit 6	IC7IF: Input (Capture Channe	el 7 Interrupt	Flag Status bit				
	1 = Interrupt	request has occ	curred					
	0 = Interrupt	request has not	t occurred					
bit 5	Unimplemen	nted: Read as ')' Flas Otatus h	:1				
DIT 4	1 = Interrupt	rnal Interrupt 1	Flag Status D	It				
	1 = Interrupt 0 = Interrupt	request has oct	toccurred					
bit 3	CNIF: Input (Change Notifica	tion Interrupt	Flag Status bit				
	1 = Interrupt	request has occ	curred					
	0 = Interrupt	request has not	toccurred					
bit 2	Unimplemer	ted: Read as '	D'	.				
bit 1	MI2C1IF: I2C	C1 Master Even	ts Interrupt FI	ag Status bit				
	\perp = Interrupt 0 = Interrupt	request has occ request has not	currea t occurred					
bit 0	SI2C1IF: I2C	1 Slave Events	Interrupt Flag	a Status bit				
	1 = Interrupt	request has occ	curred	,				
	0 = Interrupt request has not occurred							

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

REGISTER 7-18: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	—	_	_	_	_	_	—	
bit 15							bit 8	
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	
		U1EIP<2:0>		—	_	—	—	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-7	Unimplemen	ted: Read as '	0'					
bit 6-4	U1EIP<2:0>:	UART1 Error I	nterrupt Priori	ty bits				
	111 = Interrup	ot is priority 7 (highest priorit	y interrupt)				
	•							
	•							
	•							
	001 = Interrup	ot is priority 1						
	000 = Interrur	at source is dis	ahled					
			abica					

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

- bit 3
 CF: Clock Fail Detect bit (read/clear by application)

 1 = FSCM has detected clock failure

 0 = FSCM has not detected clock failure

 bit 2
 Unimplemented: Read as '0'

 bit 4
 LDOSCEN: Secondary (LD) Opcillator Enable bit
- bit 1 LPOSCEN: Secondary (LP) Oscillator Enable bit
 - 1 = Enable secondary oscillator
 - 0 = Disable secondary oscillator
- bit 0 OSWEN: Oscillator Switch Enable bit
 - 1 = Request oscillator switch to selection specified by NOSC<2:0> bits
 - 0 = Oscillator switch is complete
- **Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70186) in the *"dsPIC33F/PIC24H Family Reference Manual"* (available from the Microchip web site) for details.
 - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
 - **3:** This register is reset only on a Power-on Reset (POR).

9.0 POWER-SAVING FEATURES

- Note 1: This data sheet summarizes the features of the PIC24HJ12GP201/202 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Section 9. Watchdog Timer and Power-Saving Modes" (DS70196) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip website (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The PIC24HJ12GP201/202 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. PIC24HJ12GP201/202 devices can manage power consumption in four different ways:

- Clock frequency
- Instruction-based Sleep and Idle modes
- Software-controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

9.1 Clock Frequency and Clock Switching

PIC24HJ12GP201/202 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0** "**Oscillator Configuration**".

9.2 Instruction-Based Power-Saving Modes

PIC24HJ12GP201/202 devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The Assembler syntax of the PWRSAV instruction is shown in Example 9-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake-up.

9.2.1 SLEEP MODE

The following events occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled
- The LPRC clock continues to run if the WDT is enabled
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode
- Some device features or peripherals may continue to operate. This includes items such as the input change notification on the I/O ports, or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled

The device will wake-up from Sleep mode on any of the these events:

- · Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV #SLEEP_MODE ; Put the device into Sleep mode PWRSAV #IDLE_MODE ; Put the device into Idle mode

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
					U1CTSR<4:0	>	
bit 15							bit 8
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—			U1RXR<4:0	>	
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-13	Unimplemen	ted: Read as	'0'				
bit 12-8	U1CTSR<4:0	>: Assign UAF	RT1 Clear to S	end (U1CTS) t	o the correspo	nding RPn pin b	oits
	11111 = I npu	t tied to Vss					
	01111 = Inpu	t tied to RP15					
	•						
	•						
	00001 - Inn u	t tied to PP1					
	00000 = Inpu	t tied to RP0					
bit 7-5	Unimplemen	ted: Read as	ʻ0'				
bit 4-0	U1RXR<4:0>	: Assign UAR	T1 Receive (U	1RX) to the cor	responding RI	Pn pin bits	
	11111 = Inpu	t tied to Vss	, ,			·	
	01111 = Inpu	t tied to RP15					
	•						
	•						
	•						
	00001 = Inpu	t tied to RP1					
	00000 = Inpu	t tied to RP0					

REGISTER 10-7: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	_	—	_	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	<u> </u>	<u> </u>	—	<u> </u>		FRMDLY	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown	
bit 15	FRMEN: Fran	ned SPIx Supp	ort bit				
	1 = Framed S 0 = Framed S	Plx support en	abled (SSx pi sabled	n used as fram	ne sync pulse in	put/output)	
bit 14	SPIFSD: Fran	me Sync Pulse	Direction Cor	ntrol bit			
	1 = Frame sy	nc pulse input ((slave)				
	0 = Frame sy	nc pulse output	t (master)				
bit 13	FRMPOL: Fra	ame Sync Puls	e Polarity bit				
	1 = Frame sy	nc pulse is acti	ve-high				
h# 40.0	0 = Frame sy	nc pulse is acti	ve-low				
DIL 12-2	Unimplement	ted: Read as					
bit 1	FRMDLY: Fra	me Sync Pulse	Edge Select	bit			
	1 = Frame syl	nc pulse coinci	des with first l dos first bit old	oit clock			
hit 0		ted. This hit m	uet not be cot	to (1) by the u	eer application		
	ommplemen		usi noi de sel		sei application.		

REGISTER 15-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ⁽¹⁾		USIDL	IREN ⁽²⁾	RTSMD	_	UEN	<1:0>
bit 15		•					bit 8
R/W-0 HC	R/W-0	R/W-0 HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL
bit 7							bit 0
r							
Legend:		HC = Hardwa	re cleared				
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	UARTEN: UA 1 = UARTx is 0 = UARTx is minimal	RTx Enable bit enabled; all U disabled; all L	(1) ARTx pins ar JARTx pins ar	e controlled by e controlled by	r UARTx as defi / port latches; U	ned by UEN<1: IARTx power co	0> onsumption
bit 14	Unimplemen	ted: Read as '	כ'				
bit 13	USIDL: Stop i	n Idle Mode bi	t				
	1 = Discontin 0 = Continue	ue module ope module operat	eration when o tion in Idle mo	levice enters lo de	dle mode		
bit 12	IREN: IrDA [®] I	Encoder and D	ecoder Enabl	e bit ⁽²⁾			
	$1 = IrDA^{\mathbb{R}} energy = 0$ $0 = IrDA^{\mathbb{R}} energy = 0$	coder and deco coder and deco	oder enabled oder disabled				
bit 11	RTSMD: Mod	e Selection for	UxRTS Pin b	it			
	$1 = \frac{UxRTS}{UxRTS} p$ 0 = UxRTS p	in in Simplex m in in Flow Conf	node trol mode				
bit 10	Unimplemen	ted: Read as '	כי				
bit 9-8	UEN<1:0>: U	ARTx Enable b	oits				
	11 = UxTX, UxRX and BCLK pins are enabled and used; UxCTS pin controlled by port latches 10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin controlled by port latches 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/BCLK pins controlled by port latches						
bit 7	WAKE: Wake	-up on Start bit	Detect Durin	g Sleep Mode	Enable bit		
	1 = UARTx w in hardwa 0 = No wake-	vill continue to s are on following -up enabled	sample the Ux rising edge	RX pin; interrı،	upt generated o	n falling edge; t	bit cleared
bit 6	LPBACK: UA	RTx Loopback	Mode Select	bit			
	1 = Enable L	oopback mode					
	0 = Loopback	k mode is disab	oled				
bit 5	ABAUD: Auto	-Baud Enable	bit				
	1 = Enable ba before otl	aud rate measu her data; cleare	urement on th ed in hardwar	e next charact e upon comple	er – requires re etion	ception of a Sy	nc field (0x55)
	0 = Baud rate	e measurement	t disabled or o	completed			
Note 1: Re	efer to Section 1 formation on ena	7. "UART" (DS bling the UART	S70188) in the I module for r	e <i>"dsPIC33F/P</i> eceive or trans	PIC24H Family F smit operation.	Reference Manı	ual" for

REGISTER 17-1: UXMODE: UARTX MODE REGISTER

2: This feature is only available for the 16x BRG mode (BRGH = 0).





19.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC24HJ12GP201/202 devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.

PIC24HJ12GP201/202 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- · JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™]) programming capability
- In-Circuit emulation

19.1 Configuration Bits

PIC24HJ12GP201/202 devices provide nonvolatile memory implementation for device configuration bits. Refer to **Section 25.** "**Device Configuration**" (DS70194) of the "*dsPIC33F/PIC24H Family Reference Manual*", for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 0xF80000.

The Device Configuration register map is shown in Table 19-1.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 19-2.

Note that address 0xF80000 is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using table reads and table writes.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF80000	FBS	—	—	_	—		BSS<2:0>		BWRP
0xF80002	Reserved	_	—	_	—	—	_		_
0xF80004	FGS	_	—	_	—	—	GSS<1	:0>	GWRP
0xF80006	FOSCSEL	IESO	—			-	FNC)SC<2:0>	•
0xF80008	FOSC	FCKSM	<1:0>	IOL1WAY	—	—	OSCIOFNC	POSCM	1D<1:0>
0xF8000A	FWDT	FWDTEN	WINDIS	_	WDTPRE	WDTPOST		<3:0>	
0xF8000C	FPOR	F	Reserved(1)	ALTI2C	—	FPWRT<2:0>		•
0xF8000E	FICD	Reserv	ed ⁽²⁾	JTAGEN	—	—	—	ICS<	:1:0>
0xF80010	FUID0				User Unit ID	Byte 0			
0xF80012	FUID1		User Unit ID Byte 1						
0xF80014	FUID2	User Unit ID Byte 2							
0xF80016	FUID3				User Unit ID	Byte 3			

TABLE 19-1: DEVICE CONFIGURATION REGISTER MAP⁽²⁾

Legend: — = unimplemented bit, read as '0'.

Note 1: Reserved bits read as '1' and must be programmed as '1'.

2: These bits are reserved for use by development tools and must be programmed as '1'.

PIC24HJ12GP201/202

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection 1 = Boot segment may be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size x11 = No Boot program Flash segment
			Boot space is 256 Instruction Words (except interrupt vectors) 110 = Standard security; boot program Flash segment ends at 0x0003FE 010 = High security; boot program Flash segment ends at 0x0003FE
			Boot space is 768 Instruction Words (except interrupt vectors) 101 = Standard security; boot program Flash segment, ends at 0x0007FE 001 = High security; boot program Flash segment ends at 0x0007FE
			Boot space is 1792 Instruction Words (except interrupt vectors) 100 = Standard security; boot program Flash segment ends at 0x000FFE 000 = High security; boot program Flash segment ends at 0x000FFE
GSS<1:0>	FGS	Immediate	General Segment Code-Protect bit 11 = User program memory is not code-protected 10 = Standard security 0x = High security
GWRP	FGS	Immediate	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	FOSCSEL	Immediate	 Two-speed Oscillator Start-up Enable bit 1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start-up device with user-selected oscillator source
FNOSC<2:0>	FOSCSEL	If clock switch is enabled, RTSP effect is on any device Reset; otherwise, Immediate	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) oscillator with postscaler 110 = Internal Fast RC (FRC) oscillator with divide-by-16 101 = LPRC oscillator 100 = Secondary (LP) oscillator 011 = Primary (XT, HS, EC) oscillator with PLL 010 = Primary (XT, HS, EC) oscillator 001 = Internal Fast RC (FRC) oscillator with PLL 000 = FRC oscillator
FCKSM<1:0>	FOSC	Immediate	Clock Switching Mode bits 1x = Clock switching is disabled, fail-safe clock monitor is disabled 01 = Clock switching is enabled, fail-safe clock monitor is disabled 00 = Clock switching is enabled, fail-safe clock monitor is enabled
IOL1WAY	FOSC	Immediate	Peripheral Pin Select Configuration 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	FOSC	Immediate	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is clock output 0 = OSC2 is general purpose digital I/O pin
POSCMD<1:0>	FOSC	Immediate	Primary Oscillator Mode Select bits 11 = Primary oscillator disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode

TABLE 19-2: PIC24HJ12GP201/202 CONFIGURATION BITS DESCRIPTION

DC CHA	DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature-40°C ≤TA ≤+85°C for Industrial-40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic ⁽³⁾	Min	Min Typ ⁽¹⁾ Max		Units	Conditions	
		Program Flash Memory						
D130	Eр	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C	
D131	Vpr	VDD for Read	VMIN	—	3.6	V	Vмın = Minimum operating voltage	
D132b	VPEW	VDD for Self-Timed Write	VMIN	_	3.6	V	Vмın = Minimum operating voltage	
D134	TRETD	Characteristic Retention	20	_	—	Year	Provided no other specifications are violated (-40°C to +125°C)	
D135	IDDP	Supply Current during Programming	—	10	—	mA		
D136a	Trw	Row Write Time	1.32	_	1.74	ms	Trw = 11064 FRC cycles, TA = +85°C, See Note 2	
D136b	Trw	Row Write Time	1.28	_	1.79	ms	Trw = 11064 FRC cycles, Ta = +125°C, See Note 2	
D137a	TPE	Page Erase Time	20.1	—	26.5	ms	TPE = 168517 FRC cycles, TA = +85°C, See Note 2	
D137b	TPE	Page Erase Time	19.5	_	27.3	ms	TPE = 168517 FRC cycles, TA = +125°C, See Note 2	
D138a	Tww	Word Write Cycle Time	42.3	_	55.9	μs	Tww = 355 FRC cycles, TA = +85°C, See Note 2	
D138b	Tww	Word Write Cycle Time	41.1	—	57.6	μs	Tww = 355 FRC cycles, TA = +125°C, See Note 2	

TABLE 22-12: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.37 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 22-18) and the value of the FRC Oscillator Tuning register (see Register 8-4). For complete details on calculating the Minimum and Maximum time see Section 5.3 "Programming Operations".

3: These parameters are ensured by design, but are not characterized or tested in manufacturing.

TABLE 22-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \leq TA \leq +85^{\circ}C$ for Industrial $-40^{\circ}C \leq TA \leq +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristics	Min	Тур	Max	Units	Comments
	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10	_	μF	Capacitor must be low series resistance (< 5 ohms)

Note 1: Typical VCAP pin voltage = 2.5V when VDD \geq VDDMIN.

FIGURE 22-12: SPIX MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 22-31:SPIX MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING
REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)				
			Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency		_	9	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCKx Output Fall Time	_	—	_	ns	See parameter DO32 and Note 4
SP21	TscR	SCKx Output Rise Time	_	—	_	ns	See parameter DO31 and Note 4
SP30	TdoF	SDOx Data Output Fall Time	_	_	_	ns	See parameter DO32 and Note 4
SP31	TdoR	SDOx Data Output Rise Time	-	—	_	ns	See parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	_
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—		ns	_
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_		ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30			ns	_

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

3: The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width	Х			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2051A

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch			1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

Section Name	Update Description
Section 22.0 "Electrical Characteristics"	 Updated the following Absolute Maximum Ratings: Storage temperature Voltage on any pin that is not 5V tolerant with respect to Vss Voltage on any 5V tolerant pin with respect to Vss when VDD ≥ 3.0V Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V Added Note 4
	Revised parameters DI18, DI19, DI50, and DI51, added parameters DI21, DI25, DI26, DI27, DI28, DI29, DI60a, DI60b, and DI60c, and added Notes 5, 6, 7, 8, and 9 to the I/O Pin Input Specifications (see Table 22-9).
	Removed Note 2 from the AC Characteristics: Internal RC Accuracy (see Table 22-18).
	Updated the maximum value for parameter OC15 and the minimum value for parameter OC20 in the Simple OC/PWM Mode Timing Requirements (see Table 22-27).
	Updated <i>all</i> SPI specifications (see Table 22-28 through Table 22-35 and Figure 22-9 through Figure 22-16).
	Updated the minimum values for parameters AD05 and AD07, and the maximum value for parameter AD06 in the ADC Module Specifications (see Table 22-38).
	Added Note 4 regarding injection currents to the ADC Module Specifications (12-bit mode) (see Table 22-39).
	Added Note 4 regarding injection currents to the ADC Module Specifications (10-bit mode) (see Table 22-40).

TABLE 23-3: MAJOR SECTION UPDATES (CONTINUED)