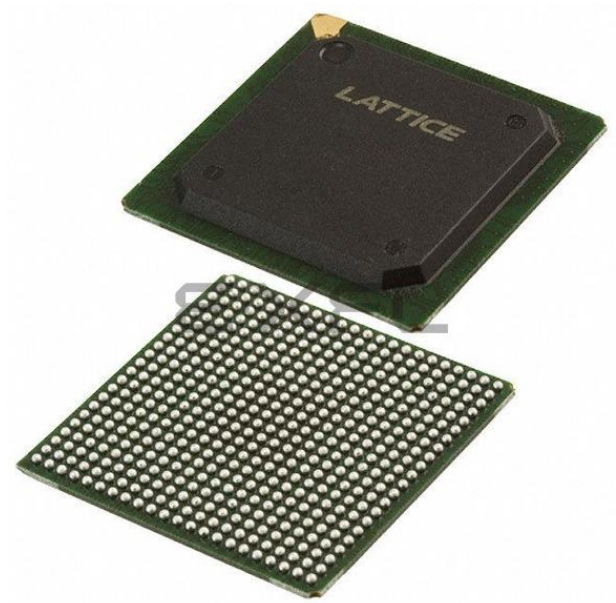
Lattice Semiconductor Corporation - LC51024MV-75F484C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	317
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024mv-75f484c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC51024MV	LC51024MV-52F484C	Active / Orderable	
	LC51024MV-52FN484C		
	LC51024MV-75F484C		
	LC51024MV-75FN484C		
	LC51024MV-75F484I		
	LC51024MV-75FN484I		
	LC51024MV-52F672C		
	LC51024MV-52FN672C		
	LC51024MV-75F672C		
	LC51024MV-75FN672C		
	LC51024MV-75F672I		
	LC51024MV-75FN672I		
LC51024MB	LC51024MB-52F484C	**Discontinued**	PCN#09-10
	LC51024MB-52FN484C		
	LC51024MB-75F484C		
	LC51024MB-75FN484C		
	LC51024MB-75F484I		
	LC51024MB-75FN484I		
	LC51024MB-52F672C		
	LC51024MB-52FN672C		
	LC51024MB-75F672C		
	LC51024MB-75FN672C		
	LC51024MB-75F672I		
	LC51024MB-75FN672I		
LC51024MC	LC51024MC-52F484C	**Discontinued**	PCN#09-10
	LC51024MC-52FN484C		
	LC51024MC-75F484C		
	LC51024MC-75FN484C		
	LC51024MC-75F484I		
	LC51024MC-75FN484I		
	LC51024MC-52F672C		
	LC51024MC-52FN672C		
	LC51024MC-75F672C		
	LC51024MC-75FN672C		
	LC51024MC-75F672I		
	LC51024MC-75FN672I		

ispXPLD™ 5000MX Family

3.3V, 2.5V and 1.8V In-System Programmable
eXpanded Programmable Logic Device XPLD™ Family

February 2010 **Data Sheet**

Features

- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
  - LVTTL
- **Expanded In-System Programmability (ispXP™)**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
  - Design security
- **High Speed Operation**
  - 4.0ns pin-to-pin delays, 300MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Typical static power: 20 to 50mA (1.8V), 30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - IEEE 1149.1 interface for boundary scan testing
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging
  - Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	3.7ns
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	250MHz
Functional Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Figure 3. MFB in SuperWIDE Logic Mode†

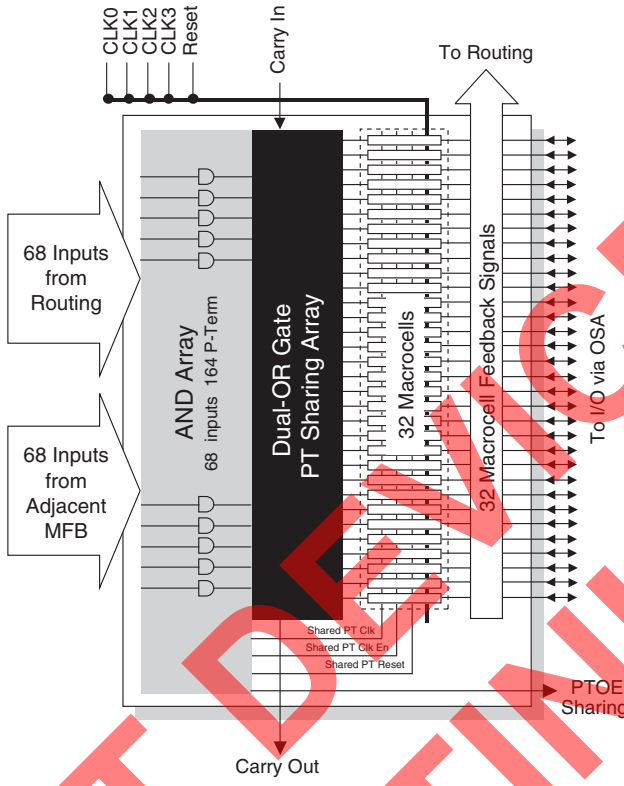


Figure 4. Macrocell Slice in Logic Mode AND-Array

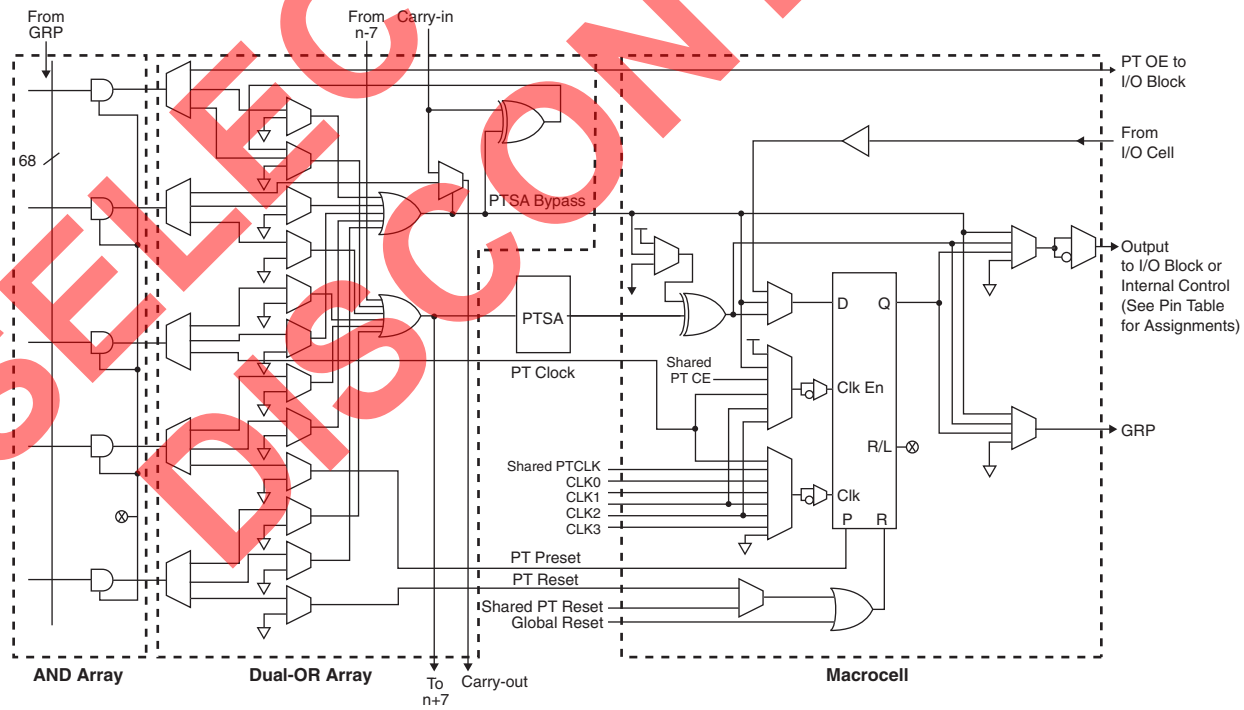


Figure 15. PLL Block Diagram

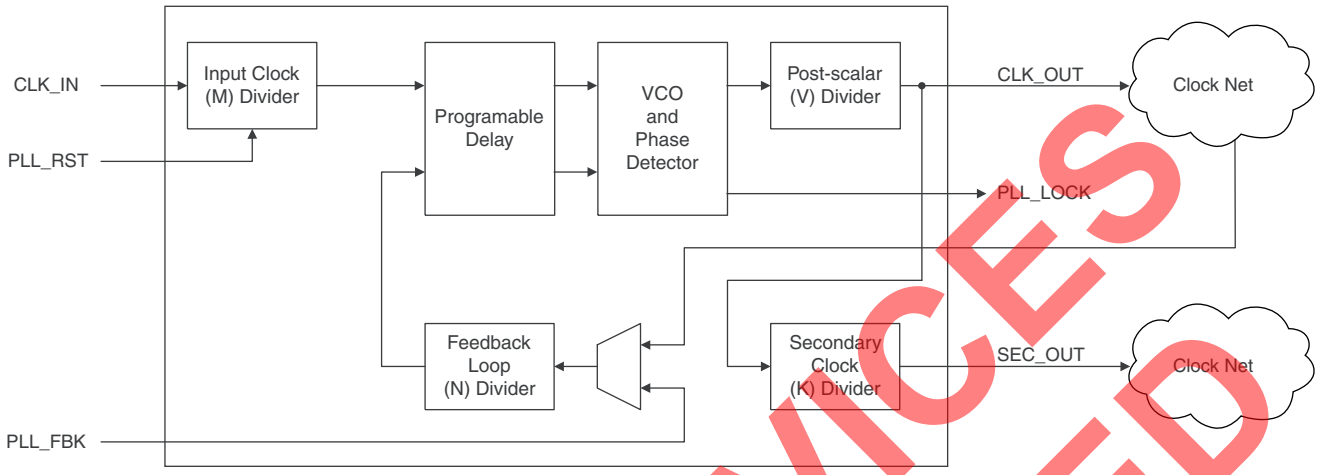
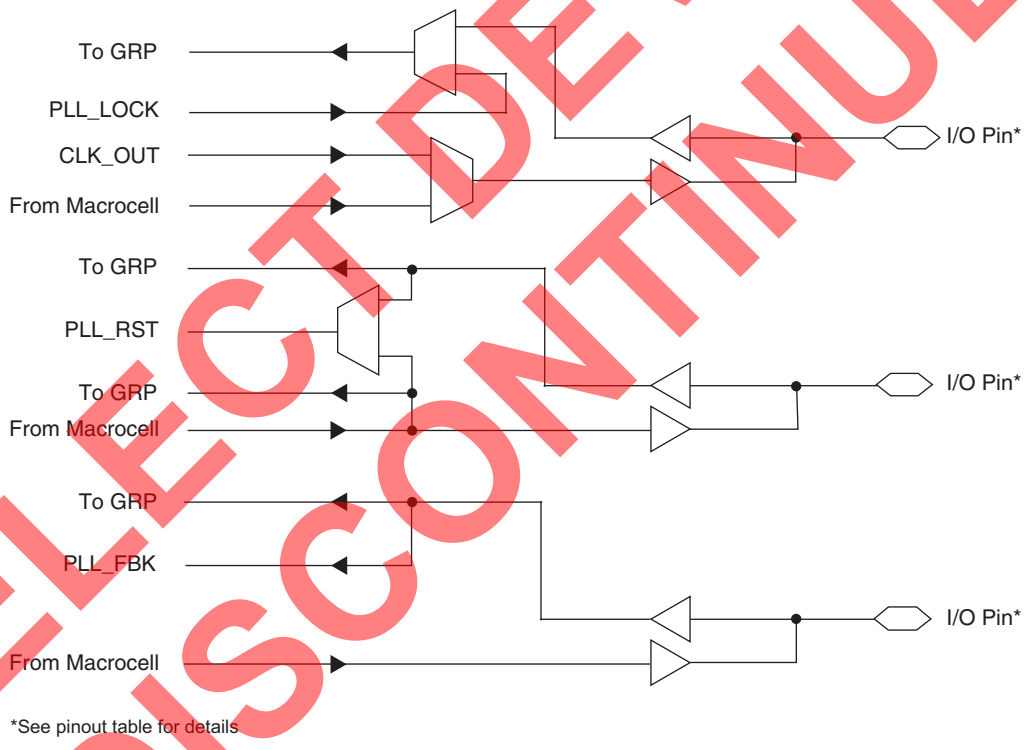


Figure 16. Connection of Optional PLL Inputs and Outputs



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

Output Sharing Array (OSA)

A number of I/O pads are available in each sysIO bank to route the selected number of macrocells from the MFB outputs directly to the I/O pads in logic mode. In the ispXPLD 5000MX, the large number of inputs and PTs to the MFB as well as the presence of the PTSA can cover most routing flexibility of signals to I/O cells. The Output Sharing Array gives additional routing capability and I/O access to an MFB when a wide output function takes up the whole MFB and cannot be easily divided across multiple MFBs. By using the OSA, the wide output function, such as 32-bit FIFO, can have all of its output signals from the one MFB routed to I/O cells. In a given I/O block, the wide output functions must share the I/O pads with other logic functions.

The OSA bypass option routes the MFB signal directly to the I/O cell, allowing a direct connection to the I/O cell. The logic functions use the option to provide faster speed to the outputs. The Logic Signal Connection tables list the OSA bypass as the primary macrocell and OSA options as alternate macrocells. Similarly, the Alternate Input listing in the table shows the alternate macrocell input connection for a given I/O pin. Figure 17 shows the alternate macrocell connections in an I/O cell.

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedback line to its associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The MFBs are grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PTOE signal is derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

sysIO Differential DC Electrical Characteristics

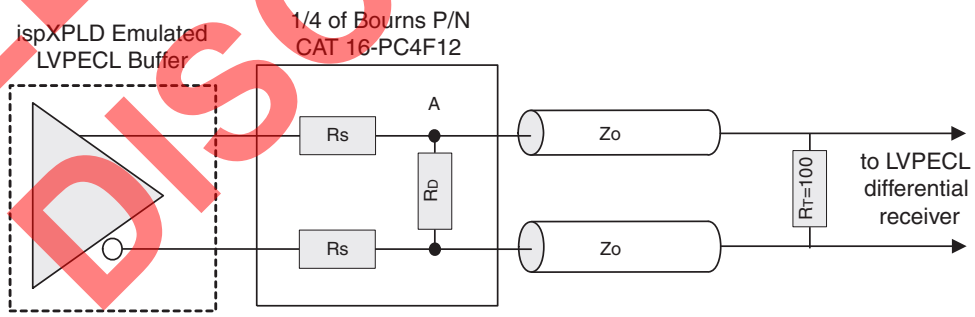
Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS					
V_{INP}	Input Voltage		0V	—	2.4V
V_{THD}	Differential Input Threshold	0.2 ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input Current	Power On	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50mV
V_{OS}	Output Voltage Offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125V	1.20V	1.375V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—	24mA

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input voltage	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 19). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V

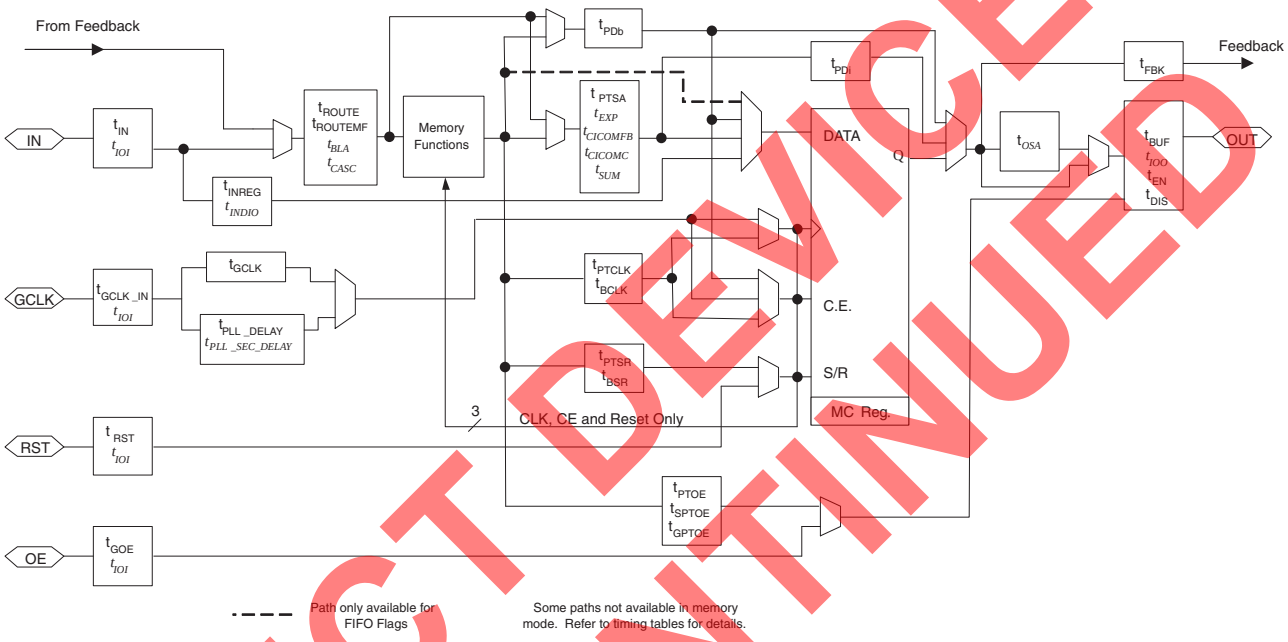
Figure 19. LVPECL Driver with Three Resistor Pack



Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



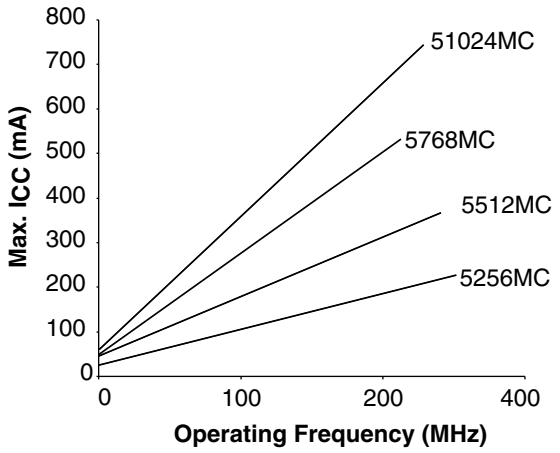
ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CAMWMSKS}$	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t_{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t_{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

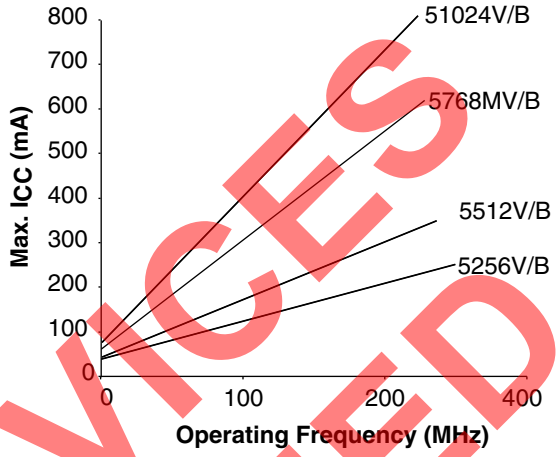
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	34N	E30	-	-	E31	H14
3	34P	E28	-	-	E29	G16
3	35N	E26	-	-	E27	G15
3	35P	E24/PLL_FBK1	-	-	E25	F15
3	36N	E22/PLL_RST1	E27	F27	E23	H12
3	36P	E21	E26	F26	-	G14
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	37N	E20	E25	F25	-	F16
-	-	VCCO3	-	-	-	VCCO3
3	37P	E18	E24	F24	E19	E16
-	-	GND	-	-	-	GND
3	38N	E16	E23	F23	E17	G13
3	38P	E14	E22	F22	E15	G12
3	39N	E12	E21	F21	E13	F14
3	39P	E10/CLK_OUT1	E20	F20	E11	E15
-	-	VCC	-	-	-	VCC
3	40N	E8	E19	F19	E9	D12
3	40P	E6	E18	F18	E7	B14
3	41N	E5	E17	F17	-	C13
3	41P	E4	E16	F16	-	A14
3	42N	E2	E31	F31	E3	A13
3	42P	E0	E30	F30	E1	B13
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
-	-	VCCO3	-	-	-	VCCO3
3	43N	F30	E15	F15	F31	B11
3	43P	F28	E14	F14	F29	C11
3	44N	F26	E13	F13	F27	B10
3	44P	F24	E12	F12	F25	A10
3	45N	F22	E11	F11	F23	C10
3	45P	F21	E10	F10	-	D10
3	46N	F20	E9	F9	-	C9
3	46P	F18	E8	F8	F19	E9
3	47N	F16/VREF3	E29	F29	F17	D9
3	47P	F14	E28	F28	F15	F9
3	48N	F12	E7	F7	F13	A9
3	48P	F10	E6	F6	F11	F8
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	49N	F8	E5	F5	F9	E8
-	-	VCCO3	-	-	-	VCCO3
3	49P	F6	E4	F4	F7	A8
3	50N	F5	E3	F3	-	B9
3	50P	F4	E2	F2	-	D8
-	-	VCC	-	-	-	VCC

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	51N	F2	E1	F1	F3	B8
3	51P	F0	E0	F0	F1	C8
0	52N	G30	G31	H31	G31	B7
0	52P	G28	G30	H30	G29	A7
-	-	GND	-	-	-	NC
0	53N	G26	G29	H29	G27	D7
0	53P	G24	G28	H28	G25	C7
0	54N	G22	G27	H27	G23	B6
-	-	VCCO0	-	-	-	VCCO0
0	54P	G21	G26	H26	-	E7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	55N	G20	G25	H25	-	E6
0	55P	G18	G24	H24	G19	A6
0	56N	G16/VREF0	G3	H3	G17	A5
0	56P	G14	G2	H2	G15	A4
0	57N	G12	G23	H23	G13	B5
0	57P	G10	G22	H22	G11	A3
0	58N	G8	G21	H21	G9	B4
0	58P	G6	G20	H20	G7	B3
0	59N	G5	G19	H19	-	C5
0	59P	G4	G18	H18	-	C6
0	60N	G2	G1	H1	G3	D5
0	60P	G0	G0	H0	G1	D6
-	-	VCCO0	-	-	-	VCCO0
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	61N	I14	I23	K23	I15	149	G13	D22
3	61P	I12	I22	K22	I13	150	G12	D21
3	62N	I10	I21	K21	I11	151	F14	J20
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	J19
3	63N	I6	K31	—	I7	—	F12	E20
—	—	V_{CC}	—	—	—	153	VCC	VCC
3	63P	I4	K30	L30	I5	—	F13	F20
3	64N	I2	K29	L28	I3	—	D16	H17
3	64P	I0	K28	L26	I1	—	D15	H18
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	65N	J30	K27	—	J31	—	—	J18
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	65P	J28	K26	—	J29	—	—	H19
3	66N	J26	K25	—	J27	—	—	G20
3	66P	J24	K24	—	J25	—	—	G19
3	67N	J22	K23	—	J23	—	—	C22
3	67P	J20	K22	—	J21	—	—	C21
3	68N	J18	K21	—	J19	—	—	D20
3	68P	J16	K20	—	J17	—	—	C19
3	69N	J14	K19	—	J15	—	C16	F19
3	69P	J12	K18	—	J13	—	B16	E19
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	70N	J10	K17	—	J11	—	C15	G18
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	70P	J8	K16	—	J9	—	B15	F18
3	71N	J6	K15	—	J7	—	E14	B20
3	71P	J4	K14	—	J5	—	D14	B19
3	72N	J2	K13	—	J3	—	E13	A20
3	72P	J0	K12	—	J1	—	A15	A19
3	73N	K30	I19	K19	K31	154	D12	D18
3	73P	K28	I18	K18	K29	155	B14	C18
3	74N	K26	I17	K17	K27	156	C13	G17
3	74P	K24	I16	K16	K25	157	A14	F16
3	75N	K22	I31	K31	K23	158	A13	E17
3	75P	K21	I30	K30	—	159	B13	D17
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	GND (Bank 3)
3	76N	K20	K11	L21	—	—	D11	B18
—	—	V_{CCO3}	—	—	—	161	V_{CCO3}	V_{CCO3}
3	76P	K18	K10	L20	K19	—	B12	A18
3	77N	K16	K9	L18	K17	—	C12	C17
3	77P	K14	K8	L16	K15	—	E11	B17
3	78N	K12	K7	L12	K13	—	—	C16
3	78P	K10	K6	L10	K11	—	—	B16

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10[1]	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	46N	G6	H19	-	G7	—	AB19
2	47P	G8	H20	-	G9	—	AA19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	47N	G10	H21	-	G11	—	U17
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	48P	G12	H22	-	G13	—	V18
2	48N	G14	H23	-	G15	—	AB21
2	49P	G16	H24	-	G17	—	U18
2	49N	G18	H25	-	G19	—	T17
2	50P	G20	H26	-	G21	R16	AB20
2	50N	G22	H27	-	G23	P16	AA20
2	51P	G24	H28	-	G25	N15	Y19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	51N	G26	H29	-	G27	N14	V19
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	52P	G28	F16	H16	G29	N16	T18
2	52N	G30	F17	H17	G31	M16	R17
2	53P	H0	F18	H18	H1	M14	U19
2	53N	H2	F19	H19	H3	M15	T19
2	54P	H4	H30	E24	H5	—	V20
-	-	VCC	-	-	-	VCC	VCC
2	54N	H6	H31	E26	H7	—	U20
2	55P	H8	F20	H20	H9	L13	W20
2	55N	H10	F21	H21	H11	L12	Y21
2	56P	H12	F22	H22	H13	L15	R18
2	56N	H14	F23	H23	H15	L16	R19
-	-	GND	-	-	-	GND	GND
2	57P	H16	F24	H24	H17	L14	W21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	57N	H18	F25	H25	H19	K15	Y22
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	58P	H20	F26	H26	H21	K14	R20
2	58N	H22	F27	H27	H23	K12	P20
2	59P	H24	F28	H28	H25	K13	T21
2	59N	H26	F29	H29	H27	J13	R21
2	60P	H28	F30	H30	H29	J14	U21
2	60N	H30	F31	H31	H31	J12	V21
-	-	TOE	-	-	-	J15	W22
-	-	RESET	-	-	-	J11	V22
-	-	GOE0	-	-	-	H11	T22
-	-	GOE1	-	-	-	H13	R22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	76P	L30/PLL_FBK1	L0	J0	L31	F15	E21
3	77N	M0/PLL_RST1	P27	N27	M1	H12	G22
3	77P	M2	P26	N26	M3	G14	F21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	78N	M4	P25	N25	M5	F16	H21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	78P	M6	P24	N24	-	E16	G21
-	-	GND	-	-	-	GND	GND
3	79N	M8	P23	N23	M9	G13	D22
3	79P	M10	P22	N22	M11	G12	D21
3	80N	M12	P21	N21	M13	F14	J20
3	80P	M14/CLK_OUT1	P20	N20	M15	E15	J19
3	81N	M16	N31	-	M17	F12	E20
-	-	VCC	-	-	-	VCC	VCC
3	81P	M18	N30	M30	M19	F13	F20
3	82N	M20	N29	M28	M21	D16	H17
3	82P	M22	N28	M26	M23	D15	H18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	83N	M24	N27	-	M25	—	J18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	83P	M26	N26	-	M27	—	H19
3	84N	M28	N25	-	M29	—	G20
3	84P	M30	N24	-	M31	—	G19
-	-	GND	-	-	-	GND	GND
3	85N	N0	N23	-	N1	—	C22
-	-	VCC	-	-	-	VCC	VCC
3	85P	N2	N22	-	N3	—	C21
3	86N	N4	N21	-	-	—	D20
3	86P	N6	N20	-	-	—	C19
3	87N	N8	N19	-	N9	C16	F19
3	87P	N10	N18	-	N11	B16	E19
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	88N	N12	N17	-	N13	C15	G18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	88P	N14	N16	-	N15	B15	F18
3	89N	N16	N15	-	N17	E14	B20
3	89P	N18	N14	-	N19	D14	B19
3	90N	N20	N13	-	N21	E13	A20
3	90P	N22	N12	-	N23	A15	A19
3	91N	N24	P19	N19	N25	D12	D18
3	91P	N26	P18	N18	N27	B14	C18
3	92N	N28	P17	N17	N29	C13	G17
3	92P	N30	P16	N16	N31	A14	F16

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5

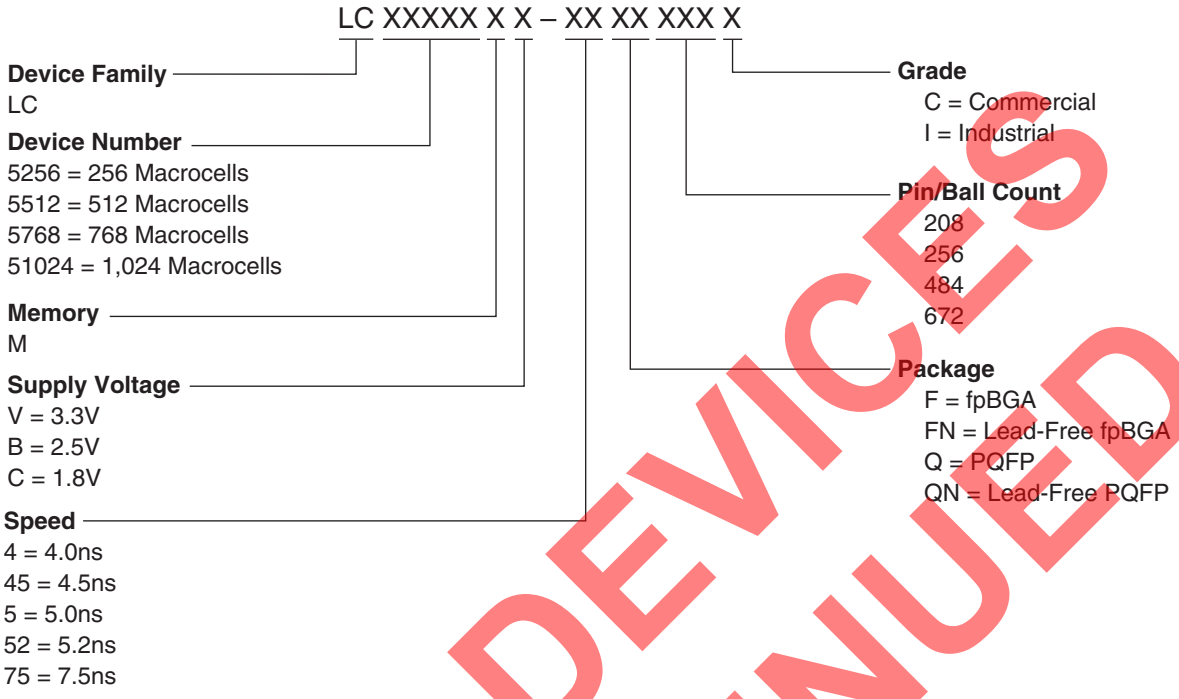
ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	63P	K8	L20	-	K9	AA19	AA18
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	63N	K10	L21	-	K11	U17	Y18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	64P	K12	L22	-	K13	V18	AD25
2	64N	K14	L23	-	K15	AB21	AD26
2	65P	K16	L24	-	K17	U18	AC23
2	65N	K18	L25	-	K19	T17	AC24
2	66P	K20	L26	-	K21	AB20	AC25
2	66N	K22	L27	-	K23	AA20	AC26
2	67P	K24	L28	-	K25	Y19	AB22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	67N	K26	L29	-	K27	V19	AB23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	68P	K28	J16	L16	K29	T18	AB24
2	68N	K30	J17	L17	K31	R17	AB25
2	69P	L0	J18	L18	L1	U19	AB26
2	69N	L2	J19	L19	L3	T19	AA26
2	70P	L4	L30	I24	L5	V20	AA22
-	-	VCC	-	-	-	VCC	VCC
2	70N	L6	L31	I26	L7	U20	Y21
2	71P	L8	J20	L20	L9	W20	AA23
2	71N	L10	J21	L21	L11	Y21	AA24
2	72P	L12	J22	L22	L13	R18	AA25
2	72N	L14	J23	L23	L15	R19	Y26
-	-	GND	-	-	-	GND	GND
2	73P	L16	J24	L24	L17	W21	Y22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	73N	L18	J25	L25	L19	Y22	Y23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	74P	L20	J26	L26	L21	R20	W20
2	74N	L22	J27	L27	L23	P20	V20
2	75P	L24	J28	L28	L25	T21	W21
2	75N	L26	J29	L29	L27	R21	V21
2	76P	L28	J30	L30	L29	U21	Y24
2	76N	L30	J31	L31	L31	V21	Y25
2	77P	N0	P0	N0	N1	—	W22
2	77N	N2	P1	N1	N3	—	W23
2	78P	N4	P2	N2	N5	—	W24
-	-	VCC	-	-	-	VCC	VCC
2	78N	N6	P3	N3	N7	—	W25
-	-	GND	-	-	-	GND	GND
2	79P	N8	P4	N4	N9	—	W26

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	142N	Y26	Y29	AA29	Y27	B11	A10
0	142P	Y24	Y28	AA28	Y25	A11	A9
0	143N	Y22	Y27	AA27	Y23	F11	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	Y20	Y26	AA26	Y21	F10	A7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	Y18	Y25	AA25	Y19	E10	A6
0	144P	Y16	Y24	AA24	Y17	C10	A5
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	A4
0	145P	Y12	Y2	AA2	Y13	B10	A3
0	146N	Y10	Y23	AA23	Y11	A10	B10
0	146P	Y8	Y22	AA22	Y9	A9	B9
0	147N	Y6	Y21	AA21	Y7	C9	B8
0	147P	Y4	Y20	AA20	Y5	D9	B7
0	148N	Y2	Y19	AA19	Y3	F9	B6
0	148P	Y0	Y18	AA18	Y1	E9	B5
0	149N	Z30	Y1	AA1	Z31	A8	B4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	149P	Z28	Y0	AA0	Z29	B8	B3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	150N	Z26	AA29	-	Z27	A7	C10
0	150P	Z24	AA28	-	Z25	B7	C9
0	151N	Z22	AA27	-	Z23	A5	C8
0	151P	Z20	AA26	-	Z21	B5	C7
0	152N	Z18	AA25	-	Z19	B6	C6
0	152P	Z16	AA24	-	Z17	C7	C5
0	153N	Z14	AA23	-	Z15	E8	C4
0	153P	Z12	AA22	-	Z13	E7	D5
0	154N	Z10	AA21	-	Z11	E6	D9
-	-	VCC	-	-	-	VCC	VCC
0	154P	Z8	AA20	-	Z9	D6	D8
-	-	GND	-	-	-	GND	GND
0	155N	Z6	AA19	-	Z7	D8	D7
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	155P	Z4	AA18	-	Z5	F8	D6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	156N	Z2	AA17	-	Z3	F7	F9
0	156P	Z0	AA16	-	Z1	D7	E9
0	157N	AA30	AA15	-	AA31	C6	F7
0	157P	AA28	AA14	-	AA29	C5	F8
0	158N	AA26	AA13	-	AA27	C4	G8
0	158P	AA24	AA12	-	AA25	D5	G9

Part Number Description



Ordering Information

Note: For voltage families offered in industrial temperature grades and for all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -45XXXXC is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only. In addition, the fastest commercial speed grade (-5) for the LC5768MB/MV devices, at Lattice's discretion, will utilize either a commercial grade only single-mark or a dual-mark format in conjunction with the slower industrial speed grade (-75).

Conventional Packaging

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	141	C
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	141	C
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	141	C
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	149	C
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	149	C
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	193	C
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	193	C
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	253	C
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	253	C