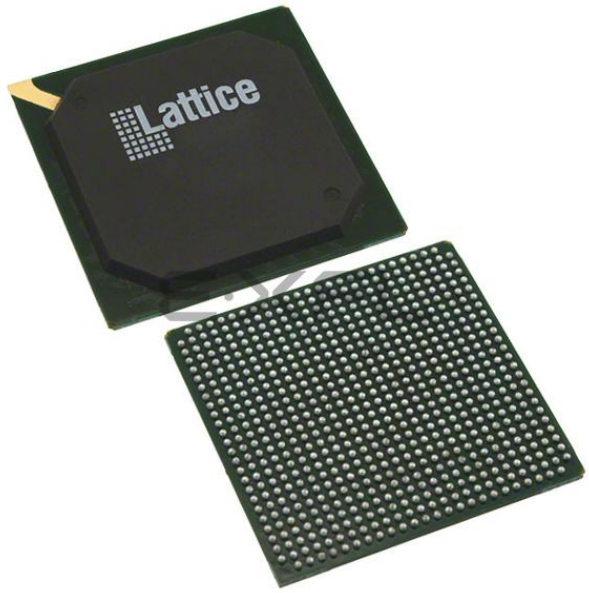
Lattice Semiconductor Corporation - LC51024MV-75F672C Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

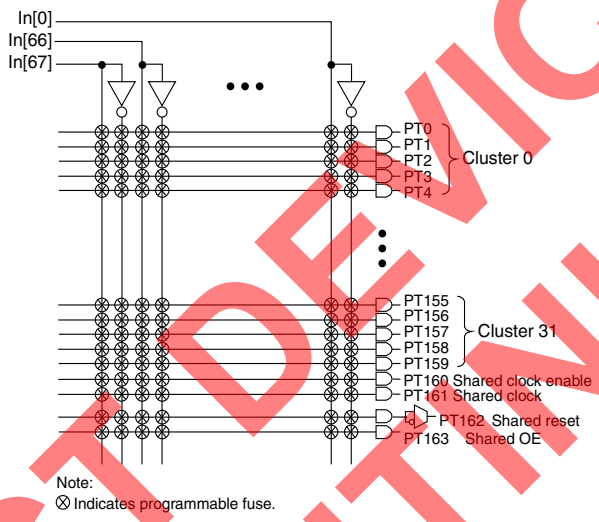
Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	381
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024mv-75f672c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC51024MV	LC51024MV-52F484C	Active / Orderable	
	LC51024MV-52FN484C		
	LC51024MV-75F484C		
	LC51024MV-75FN484C		
	LC51024MV-75F484I		
	LC51024MV-75FN484I		
	LC51024MV-52F672C		
	LC51024MV-52FN672C		
	LC51024MV-75F672C		
	LC51024MV-75FN672C		
	LC51024MV-75F672I		
	LC51024MV-75FN672I		
LC51024MB	LC51024MB-52F484C	**Discontinued**	PCN#09-10
	LC51024MB-52FN484C		
	LC51024MB-75F484C		
	LC51024MB-75FN484C		
	LC51024MB-75F484I		
	LC51024MB-75FN484I		
	LC51024MB-52F672C		
	LC51024MB-52FN672C		
	LC51024MB-75F672C		
	LC51024MB-75FN672C		
	LC51024MB-75F672I		
	LC51024MB-75FN672I		
LC51024MC	LC51024MC-52F484C	**Discontinued**	PCN#09-10
	LC51024MC-52FN484C		
	LC51024MC-75F484C		
	LC51024MC-75FN484C		
	LC51024MC-75F484I		
	LC51024MC-75FN484I		
	LC51024MC-52F672C		
	LC51024MC-52FN672C		
	LC51024MC-75F672C		
	LC51024MC-75FN672C		
	LC51024MC-75F672I		
	LC51024MC-75FN672I		

AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array



Dual-OR Array (Including Arithmetic Support)

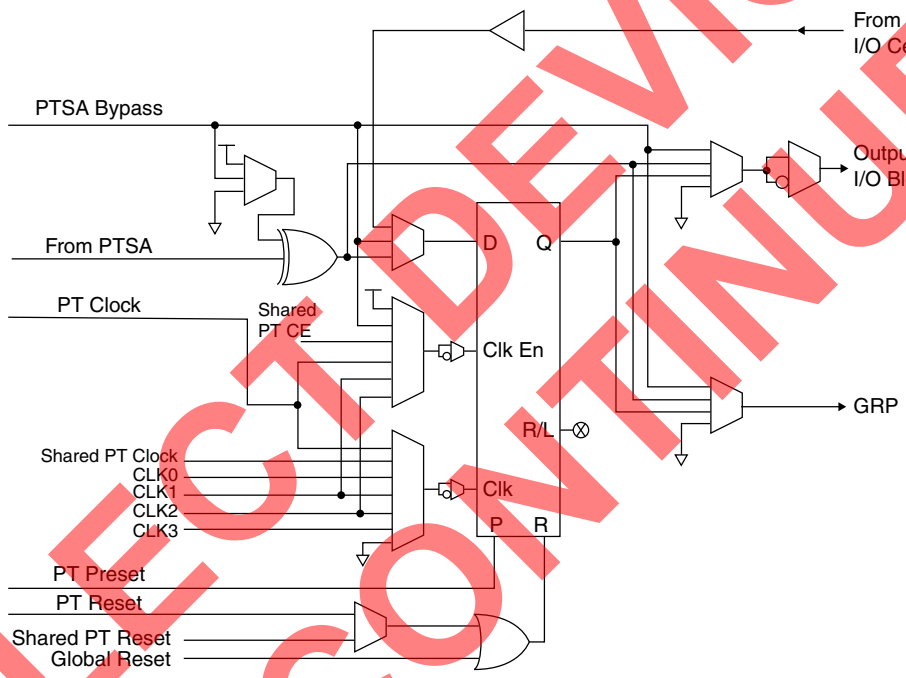
The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in TN1030, Using Memory in ispXPLD 5000MX Devices.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

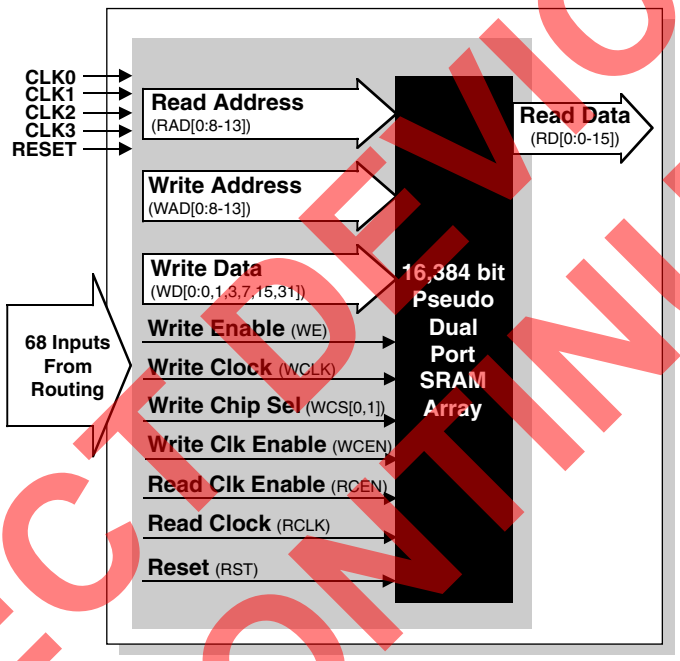


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor style interface (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more information on the sysCONFIG capability, refer to TN1026, ispXP Configuration Usage Guidelines.

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For information on estimating power consumption, refer to TN1031 Power Estimation in ispXPLD 5000MX Devices.

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings[1, 2, 3]

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IHMAX} +2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95	V
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7	V
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6	V
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95	V
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7	V
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6	V
T_J	Junction Temperature (Commercial Operation)	0	90	C
	Junction Temperature (Industrial Operation)	-40	105	C

E²CMOS Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	0 ð V_{IN} ð 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO}þð 1.0V. For V_{CCO} > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and $V_{CCO,}$ provided (V_{IN} - V_{CCO})þð 3.6V.
2. 0 ð V_{CC} ð V_{CC} (MAX), 0 ð V_{CCO} ð V_{CCO} (MAX)
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.
4. LVTTL, LVCMOS only.

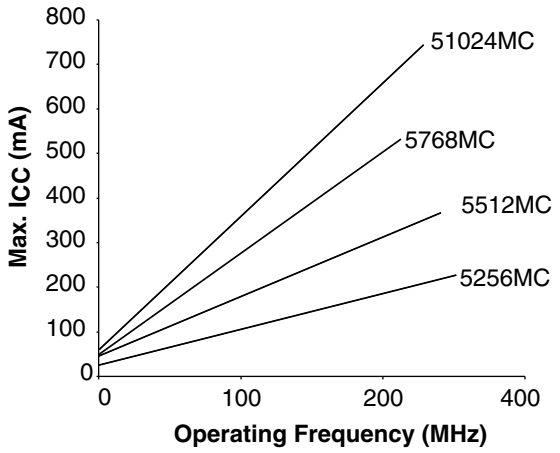
ispXPLD 5000MX Family External Switching Characteristics [1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Output Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX} [4]	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
f_{MAX} (Ext.)	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
f_{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
f_{MAX} (CAMC)[5]	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
f_{MAX} (CAM)[5]	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

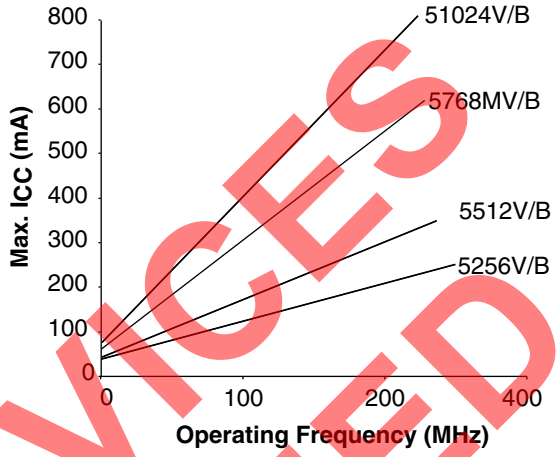
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Power Estimation Equations

ICC = ICC_DC + IMFB_CPLD + IMFB_ SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL_D

ICC_DC
Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) from the data sheet.

IMFB_CPLD
= ((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** * CPLD GRP from IFB) * AF+ **K4**) * FREQ / 1000µA/mA

IMFB_CAM
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

IMFB_ SRAM/PDPRAM/FIFO
= (WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (**K1** + 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * SRAM/PDPRAM/FIFO Memory MFBs * FREQ / 1000µA/mA

IMFB_ DPRAM
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs * FREQ / 1000µA/mA

IPLL_D
= **K5** * PLL_FREQ * number of PLLs used. IPPL_D is the PLL digital component of the VCC supply current.

Analog portion of PLL supply current consumption, from PLL power pin:

IPLL_A = (**K6** * PLL_FREQ + **K7**) * number of PLLs used

Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	B4
0	109P	O28	O10	P16	O29	1	E4	A4
0	110N	O26	M17	O17	O27	2	B1	B3
0	110P	O24	M16	O16	O25	3	C1	A3
0	111N	O22	M15	O15	O23	4	D3	F5
—	—	V_{CCO0}	—	—	—	5	V_{CCO0}	V_{CCO0}
0	111P	O20	M14	O14	O21	6	C2	G6
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	GND (Bank 0)
0	112N	O18	M13	O13	O19	8	E3	H6
0	112P	O16	M12	O12	O17	9	D2	G5
0	113N	O14	O9	P14	O15	—	—	D3
0	113P	O12	O8	P12	O13	—	—	D2
0	114N	O10	O7	P10	O11	—	—	E4
0	114P	O8	O6	P8	O9	—	—	E3
0	115N	O6	O5	P6	O7	—	—	F4
0	115P	O4	O4	P4	O5	—	—	G4
0	116N	O2	O3	P2	O3	—	—	C2
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	V_{CCO0}
0	116P	O0	O2	P0	O1	—	—	C1
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	117N	P30	O1	—	P31	—	D1	F3
0	117P	P28	O0	—	P29	—	E1	G3
0	118N	P26	O31	—	P27	—	F4	H4
—	—	V_{CC}	—	—	—	10	V_{CC}	V_{CC}
0	118P	P24	O30	—	P25	—	F5	J4
0	119N	P22	M11	O11	P23	11	E2	H5
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	J5
0	120N	P18	M9	O9	P19	13	F1	E2
0	120P	P16	M8	O8	P17	14	G1	F2
—	—	GND	—	—	—	15	GND	GND
0	121N	P14	M7	O7	P15	16	F3	D1
—	—	V_{CCO0}	—	—	—	17	V_{CCO0}	V_{CCO0}
0	121P	P12	M6	O6	P13	18	G5	E1
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	GND (Bank 0)
0	122N	P10	M5	O5	P11	20	H5	J3
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	H2
0	123N	P6	—	—	P7	22	G3	G2
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	G1
0	124N	P2	—	—	P3	24	G2	H1
0	124P	P0	—	—	P1	25	H1	J1
—	GCLK0P	GCLK0	—	—	—	26	H2	N7
—	—	V_{CCJ}	—	—	—	See Power Supply and NC Connections Table		

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	V_{CCO2}
2	29N	E10	F5	H5	E11	86	M10	U12
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	GND (Bank 2)
2	30P	E12	F6	H6	E13	88	M11	AB13
2	30N	E16	F7	H7	E17	89	T13	Y13
2	31P	E18	—	—	E19	90	P11	V13
2	31N	E20/V_{REF2}	—	—	E21	91	T14	W13
2	32P	E22	F8	H8	E23	92	R12	V14
2	32N	E24	F9	H9	E25	93	R13	W14
2	33P	E26	F10	H10	E27	94	N11	Y14
2	33N	E28	F11	H11	E29	95	T15	AB14
2	34P	F0	F12	H12	F1	96	R14	AB15
2	34N	F2	F13	H13	F3	97	N12	AA15
2	35P	F4	F14	H14	F5	98	P12	U13
—	—	V_{CCO2}	—	—	—	—	V_{CCO2}	V_{CCO2}
2	35N	F6	F15	H15	F7	99	R15	U14
—	—	GND (Bank 2)	—	—	—	—	GND (Bank 2)	GND (Bank 2)
2	36P	F8	E0	—	F9	—	—	W15
2	36N	F10	E2	—	F11	—	—	W16
2	37P	F12	E4	—	F13	—	—	Y16
2	37N	F16	E6	—	F17	—	—	AA16
2	38P	F18	E8	—	F19	—	—	AB16
2	38N	F20	E10	—	F21	—	—	AA17
2	39P	F22	E12	—	F23	—	—	Y17
2	39N	F24	E16	—	F25	—	—	AA18
2	40P	F26	E20	—	F27	—	—	W17
2	40N	F28	E22	—	F29	—	—	W18
2	41P	G0	—	—	G1	—	—	V15
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	V_{CCO2}
2	41N	G2	—	—	G3	—	—	U15
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	GND (Bank 2)
2	42P	G4	—	—	G5	102	P13	Y18
2	42N	G6	—	—	G7	103	P15	V17
2	43P	G8	—	—	G9	—	M13	V16
2	43N	G10	—	—	G11	—	P14	U16
2	44P	G12	—	—	G13	—	—	AB18
2	44N	G14	—	—	G15	—	—	AB19
2	45P	G16	—	—	G17	—	—	U18
2	45N	G18	—	—	G19	—	—	T17
2	46P	G20	—	—	G21	104	R16	AB20
2	46N	G22	—	—	G23	105	P16	AA20
2	47P	G24	—	—	G25	106	N15	Y19
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	V_{CCO2}

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	V19
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	—	—	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	—	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10[1]	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	46N	G6	H19	-	G7	—	AB19
2	47P	G8	H20	-	G9	—	AA19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	47N	G10	H21	-	G11	—	U17
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	48P	G12	H22	-	G13	—	V18
2	48N	G14	H23	-	G15	—	AB21
2	49P	G16	H24	-	G17	—	U18
2	49N	G18	H25	-	G19	—	T17
2	50P	G20	H26	-	G21	R16	AB20
2	50N	G22	H27	-	G23	P16	AA20
2	51P	G24	H28	-	G25	N15	Y19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	51N	G26	H29	-	G27	N14	V19
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	52P	G28	F16	H16	G29	N16	T18
2	52N	G30	F17	H17	G31	M16	R17
2	53P	H0	F18	H18	H1	M14	U19
2	53N	H2	F19	H19	H3	M15	T19
2	54P	H4	H30	E24	H5	—	V20
-	-	VCC	-	-	-	VCC	VCC
2	54N	H6	H31	E26	H7	—	U20
2	55P	H8	F20	H20	H9	L13	W20
2	55N	H10	F21	H21	H11	L12	Y21
2	56P	H12	F22	H22	H13	L15	R18
2	56N	H14	F23	H23	H15	L16	R19
-	-	GND	-	-	-	GND	GND
2	57P	H16	F24	H24	H17	L14	W21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	57N	H18	F25	H25	H19	K15	Y22
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	58P	H20	F26	H26	H21	K14	R20
2	58N	H22	F27	H27	H23	K12	P20
2	59P	H24	F28	H28	H25	K13	T21
2	59N	H26	F29	H29	H27	J13	R21
2	60P	H28	F30	H30	H29	J14	U21
2	60N	H30	F31	H31	H31	J12	V21
-	-	TOE	-	-	-	J15	W22
-	-	RESET	-	-	-	J11	V22
-	-	GOE0	-	-	-	H11	T22
-	-	GOE1	-	-	-	H13	R22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	T1	P3
-	-	TDO	-	-	-	V1	P2
1	0P	A30	A0	C0	A31	—	P1
1	0N	A28	A1	C1	A29	—	R1
1	1P	A26	A2	C2	A27	—	P6
1	1N	A24	A3	C3	A25	—	R6
1	2P	A22	A4	C4	A23	—	P7
1	2N	A20	A5	C5	A21	—	R7
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18	A6	C6	A19	—	R4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16	A7	C7	A17	—	R5
-	-	GND	-	-	-	GND	GND
1	4P	A14	A8	C8	A15	—	R3
-	-	VCC	-	-	-	VCC	VCC
1	4N	A12	A9	C9	A13	—	R2
1	5P	A10	A10	C10	A11	—	T2
1	5N	A8	A11	C11	A9	—	T3
1	6P	A6	A12	C12	A7	—	T4
1	6N	A4	A13	C13	A5	—	T5
1	7P	A2	A14	C14	A3	—	U2
1	7N	A0	A15	C15	A1	—	U3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	8P	C30	A16	C16	C31	—	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	8N	C28	A17	C17	C29	—	U5
1	9P	C26	A18	C18	C27	—	T6
1	9N	C24	A19	C19	C25	—	U6
1	10P	C22	A20	C20	C23	—	T7
1	10N	C20	A21	C21	C21	—	U7
1	11P	C18	A22	C22	C19	—	U1
1	11N	C16	A23	C23	C17	—	V1
1	12P	C14	A24	C24	C15	—	V2
1	12N	C12	A25	C25	C13	—	V3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	13P	C10	A26	C26	C11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	13N	C8	A27	C27	C9	—	V4
-	-	GND	-	-	-	GND	GND
1	14P	C6	A28	C28	C7	—	W2
-	-	VCC	-	-	-	VCC	VCC
1	14N	C4	A29	C29	C5	—	W3
1	15P	C2	A30	C30	C3	—	W4

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3P	GCLK3	-	-	-	N16	N24
3	93N	R0	T31	R31	R1	J22	N23
3	93P	R2	T30	R30	R3	H22	N22
3	94N	R4	T29	R29	R5	N19	M26
3	94P	R6	T28	R28	R7	P15	M25
3	95N	R8	T27	R27	R9	P21	M23
3	95P	R10	T26	R26	R11	N15	M22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	96N	R12	T25	R25	R13	M15	N20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	96P	R14	T24	R24	R15	N20	M20
-	-	GND	-	-	-	GND	GND
3	97N	R16	T23	R23	R17	P22	N21
3	97P	R18	T22	R22	R19	N21	M21
3	98N	R20	T21	R21	R21	N17	M24
3	98P	R22	T20	R20	R23	M20	L24
3	99N	R24	T19	R19	R25	P17	L23
-	-	VCC	-	-	-	VCC	VCC
3	99P	R26	T18	R18	R27	P18	L22
3	100N	R28	T17	R17	R29	M21	L25
3	100P	R30	T16	R16	R31	M17	K26
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	101N	T0	T15	R15	T1	L20	K25
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	101P	T2	T14	R14	T3	N18	K24
3	102N	T4	T13	R13	T5	L21	K23
3	102P	T6	T12	R12	T7	M18	K22
3	103N	T8	T11	R11	T9	L22	J25
3	103P	T10	T10	R10	T11	L17	J24
3	104N	T12	T9	R9	T13	K22	L21
3	104P	T14	T8	R8	T15	L18	K21
3	105N	T16	T7	R7	T17	K21	L20
3	105P	T18	T6	R6	T19	K18	K20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	T20	T5	R5	T21	K20	J23
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	T22	T4	R4	T23	K17	J22
3	107N	T24	T3	R3	T25	K19	J26
3	107P	T26	T2	R2	T27	J17	H26
3	108N	T28	T1	R1	T29	E22	H25
3	108P	T30/PLL_FBK1	T0	R0	T31	E21	H24
3	109N	U0/PLL_RST1	X27	V27	U1	G22	H23
3	109P	U2	X26	V26	U3	F21	H22

Lead-Free Packaging

ispXPLD 5000MC (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4FN256C	256	1.8	4.0	Lead-free fpBGA	256	141	C
	LC5256MC-5FN256C	256	1.8	5.0	Lead-free fpBGA	256	141	C
	LC5256MC-75FN256C	256	1.8	7.5	Lead-free fpBGA	256	141	C
LC5512MC	LC5512MC-45QN208C	512	1.8	4.5	Lead-free PQFP	208	149	C
	LC5512MC-75QN208C	512	1.8	7.5	Lead-free PQFP	208	149	C
	LC5512MC-45FN256C	512	1.8	4.5	Lead-free fpBGA	256	193	C
	LC5512MC-75FN256C	512	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5512MC-45FN484C	512	1.8	4.5	Lead-free fpBGA	484	253	C
	LC5512MC-75FN484C	512	1.8	7.5	Lead-free fpBGA	484	253	C
LC5768MC	LC5768MC-5FN256C	768	1.8	5.0	Lead-free fpBGA	256	193	C
	LC5768MC-75FN256C	768	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5768MC-5FN484C	768	1.8	5.0	Lead-free fpBGA	484	317	C
	LC5768MC-75FN484C	768	1.8	7.5	Lead-free fpBGA	484	317	C
LC51024MC	LC51024MC-52FN484C	1024	1.8	5.2	Lead-free fpBGA	484	317	C
	LC51024MC-75FN484C	1024	1.8	7.5	Lead-free fpBGA	484	317	C
	LC51024MC-52FN672C	1024	1.8	5.2	Lead-free fpBGA	672	381	C
	LC51024MC-75FN672C	1024	1.8	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5FN256I	256	1.8	5.0	Lead-free fpBGA	256	141	I
	LC5256MC-75FN256I	256	1.8	7.5	Lead-free fpBGA	256	141	I
LC5512MC	LC5512MC-75QN208I	512	1.8	7.5	Lead-free PQFP	208	149	I
	LC5512MC-75FN256I	512	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5512MC-75FN484I	512	1.8	7.5	Lead-free fpBGA	484	253	I
LC5768MC	LC5768MC-75FN256I	768	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5768MC-75FN484I	768	1.8	7.5	Lead-free fpBGA	484	317	I
LC51024MC	LC51024MC-75FN484I	1024	1.8	7.5	Lead-free fpBGA	484	317	I
	LC51024MC-75FN672I	1024	1.8	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MB (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4FN256C	256	2.5	4.0	Lead-free fpBGA	256	141	C
	LC5256MB-5FN256C	256	2.5	5.0	Lead-free fpBGA	256	141	C
	LC5256MB-75FN256C	256	2.5	7.5	Lead-free fpBGA	256	141	C
LC5512MB	LC5512MB-45QN208C	512	2.5	4.5	Lead-free PQFP	208	149	C
	LC5512MB-75QN208C	512	2.5	7.5	Lead-free PQFP	208	149	C
	LC5512MB-45FN256C	512	2.5	4.5	Lead-free fpBGA	256	193	C
	LC5512MB-75FN256C	512	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5512MB-45FN484C	512	2.5	4.5	Lead-free fpBGA	484	253	C
	LC5512MB-75FN484C	512	2.5	7.5	Lead-free fpBGA	484	253	C
LC5768MB	LC5768MB-5FN256C	768	2.5	5.0	Lead-free fpBGA	256	193	C
	LC5768MB-75FN256C	768	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5768MB-5FN484C	768	2.5	5.0	Lead-free fpBGA	484	317	C
	LC5768MB-75FN484C	768	2.5	7.5	Lead-free fpBGA	484	317	C
LC51024MB	LC51024MB-52FN484C	1024	2.5	5.2	Lead-free fpBGA	484	317	C
	LC51024MB-75FN484C	1024	2.5	7.5	Lead-free fpBGA	484	317	C
	LC51024MB-52FN672C	1024	2.5	5.2	Lead-free fpBGA	672	381	C
	LC51024MB-75FN672C	1024	2.5	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5FN256I	256	2.5	5.0	Lead-free fpBGA	256	141	I
	LC5256MB-75FN256I	256	2.5	7.5	Lead-free fpBGA	256	141	I
LC5512MB	LC5512MB-75QN208I	512	2.5	7.5	Lead-free PQFP	208	149	I
	LC5512MB-75FN256I	512	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5512MB-75FN484I	512	2.5	7.5	Lead-free fpBGA	484	253	I
LC5768MB	LC5768MB-75FN256I	768	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5768MB-75FN484I	768	2.5	7.5	Lead-free fpBGA	484	317	I
LC51024MB	LC51024MB-75FN484I	1024	2.5	7.5	Lead-free fpBGA	484	317	I
	LC51024MB-75FN672I	1024	2.5	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4FN256C	256	3.3	4.0	Lead-free fpBGA	256	141	C
	LC5256MV-5FN256C	256	3.3	5.0	Lead-free fpBGA	256	141	C
	LC5256MV-75FN256C	256	3.3	7.5	Lead-free fpBGA	256	141	C

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5512MV	LC5512MV-45QN208C	512	3.3	4.5	Lead-free PQFP	208	149	C
	LC5512MV-75QN208C	512	3.3	7.5	Lead-free PQFP	208	149	C
	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	193	C
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	253	C
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	253	C
LC5768MV	LC5768MV-5FN256C	768	3.3	5.0	Lead-free fpBGA	256	193	C
	LC5768MV-75FN256C	768	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5768MV-5FN484C	768	3.3	5.0	Lead-free fpBGA	484	317	C
	LC5768MV-75FN484C	768	3.3	7.5	Lead-free fpBGA	484	317	C
LC51024MV	LC51024MV-52FN484C	1024	3.3	5.2	Lead-free fpBGA	484	317	C
	LC51024MV-75FN484C	1024	3.3	7.5	Lead-free fpBGA	484	317	C
	LC51024MV-52FN672C	1024	3.3	5.2	Lead-free fpBGA	672	381	C
	LC51024MV-75FN672C	1024	3.3	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5FN256I	256	3.3	5.0	Lead-free fpBGA	256	141	I
	LC5256MV-75FN256I	256	3.3	7.5	Lead-free fpBGA	256	141	I
LC5512MV	LC5512MV-75QN208I	512	3.3	7.5	Lead-free PQFP	208	149	I
	LC5512MV-75FN256I	512	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5512MV-75FN484I	512	3.3	7.5	Lead-free fpBGA	484	253	I
LC5768MV	LC5768MV-75FN256I	768	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5768MV-75FN484I	768	3.3	7.5	Lead-free fpBGA	484	317	I
LC51024MV	LC51024MV-75FN484I	1024	3.3	7.5	Lead-free fpBGA	484	317	I
	LC51024MV-75FN672I	1024	3.3	7.5	Lead-free fpBGA	672	381	I

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- TN1000 – sysIO Usage Guidelines for Lattice Devices
- TN1003 – sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices
- TN1031 – Power Estimation in ispXPLD 5000MX Devices
- TN1030 – Using Memory in ispXPLD 5000MX Devices
- TN1026 – ispXP Configuration Usage Guidelines