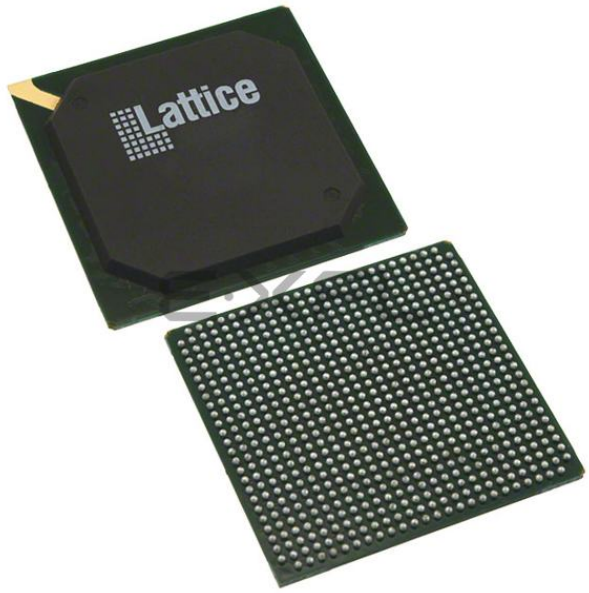
Lattice Semiconductor Corporation - LC51024MV-75FN672I Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	381
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024mv-75fn672i

ispXPLD™ 5000MX Family

3.3V, 2.5V and 1.8V In-System Programmable
eXpanded Programmable Logic Device XPLD™ Family

February 2010 **Data Sheet**

Features

- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
  - LVTTL
- **Expanded In-System Programmability (ispXP™)**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
  - Design security
- **High Speed Operation**
  - 4.0ns pin-to-pin delays, 300MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Typical static power: 20 to 50mA (1.8V), 30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - IEEE 1149.1 interface for boundary scan testing
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging
  - Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	3.7ns
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	250MHz
Functional Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Figure 1. ispXPLD 5000MX Block Diagram

Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

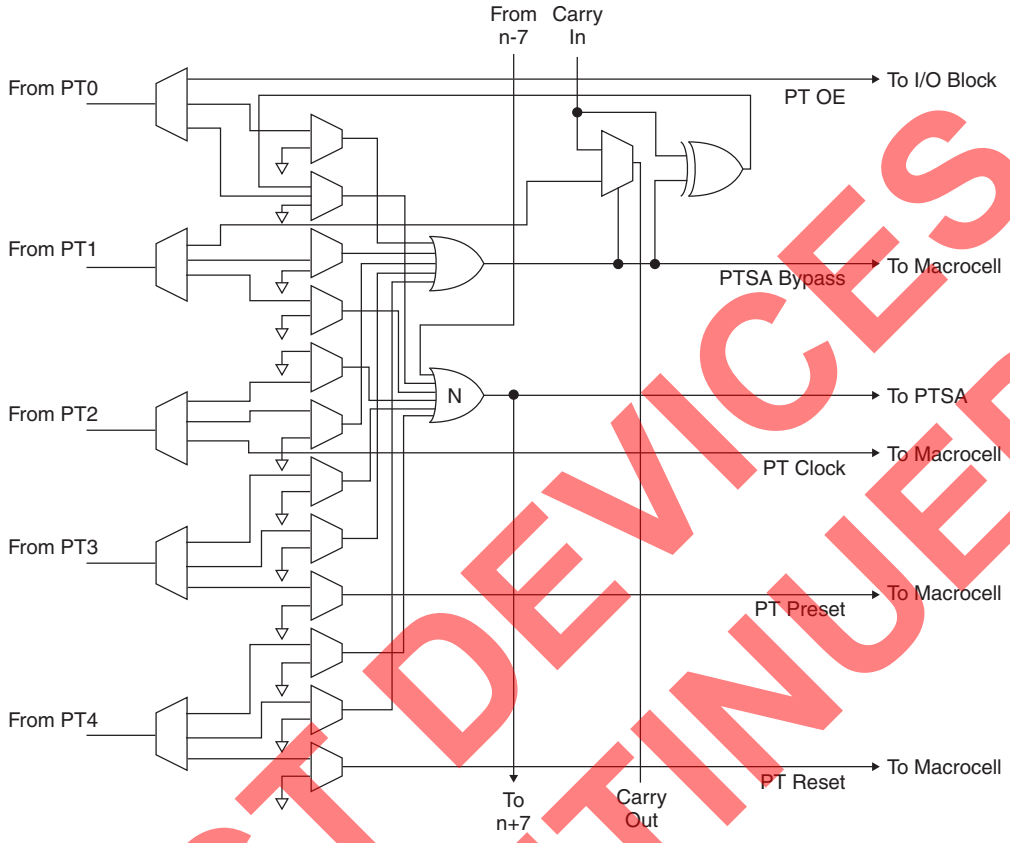
The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

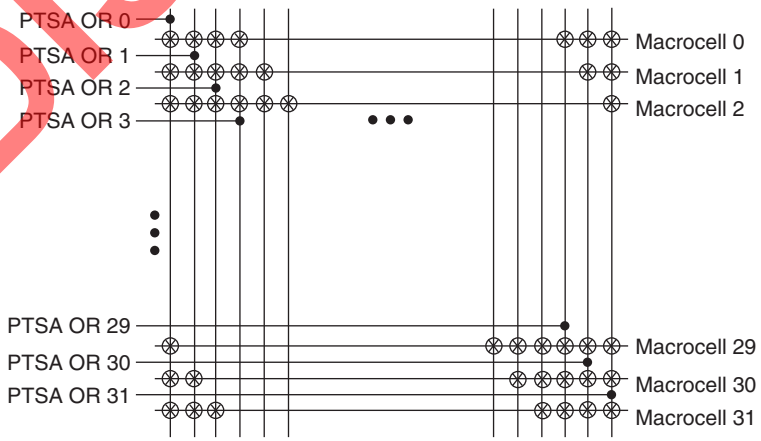
Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

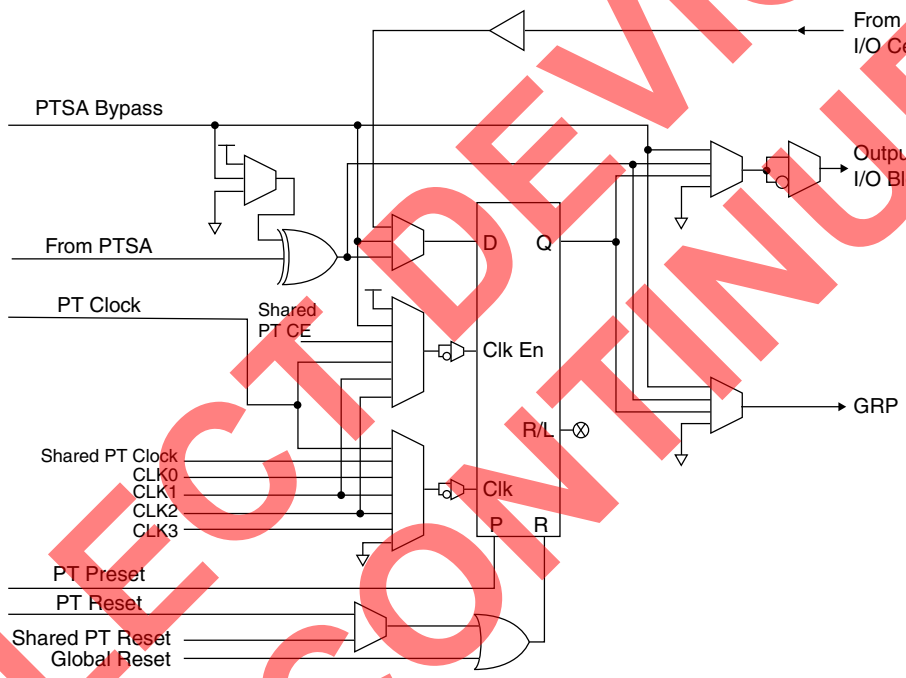
Figure 7. Product Term Sharing Array (PTSA)



Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in TN1030, Using Memory in ispXPLD 5000MX Devices.

True Dual-Port SRAM Mode

In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two independent read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are supported by the MFB. Figure 9 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Resets are asynchronous. All inputs on the same port share the same clock, clock enable, and reset selections. All outputs on the same port share the same clock, clock enable, and reset selections. Selections may be made independently between both inputs and outputs and ports. Table 5 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 9. Dual-Port SRAM Block Diagram

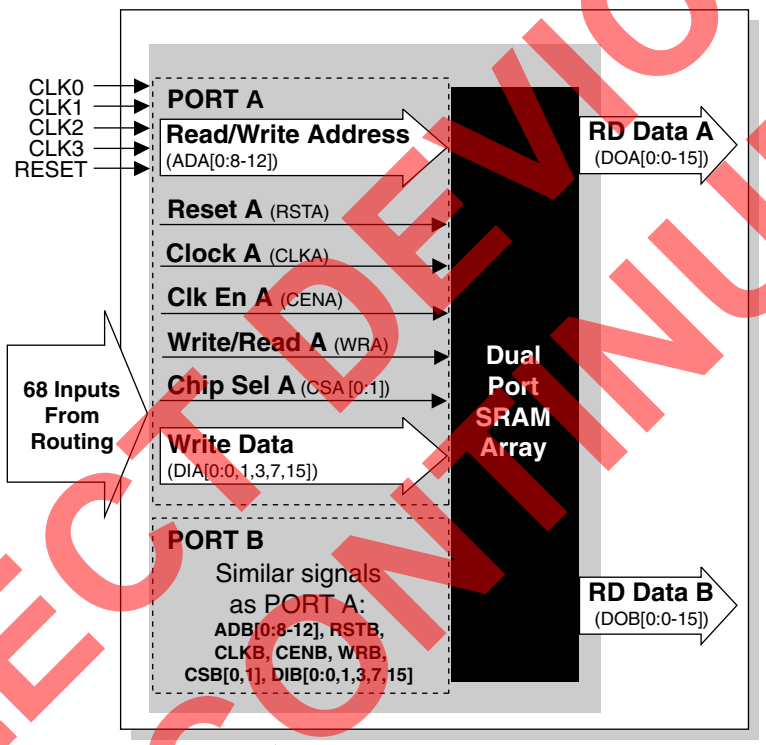


Table 5. Register Clock, Clock Enable, and Reset in Dual-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLKA (CLKB) or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	CENA (CENB) or one of the global clocks (CLK1 - CLK 2). The selected signal can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RSTA (RSTB). RSTA (RSTB) can be inverted is desired.

Figure 15. PLL Block Diagram

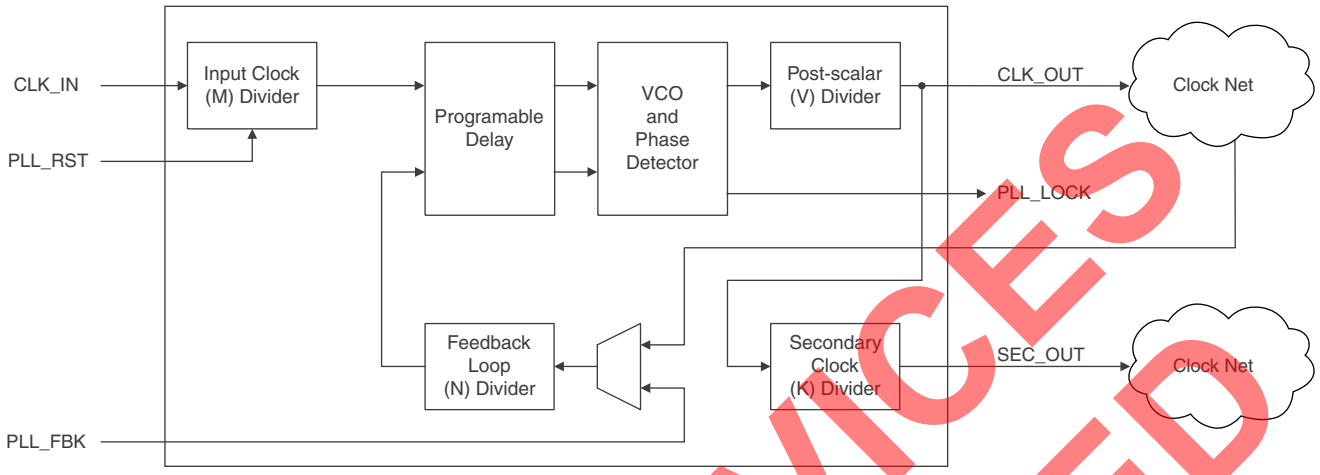
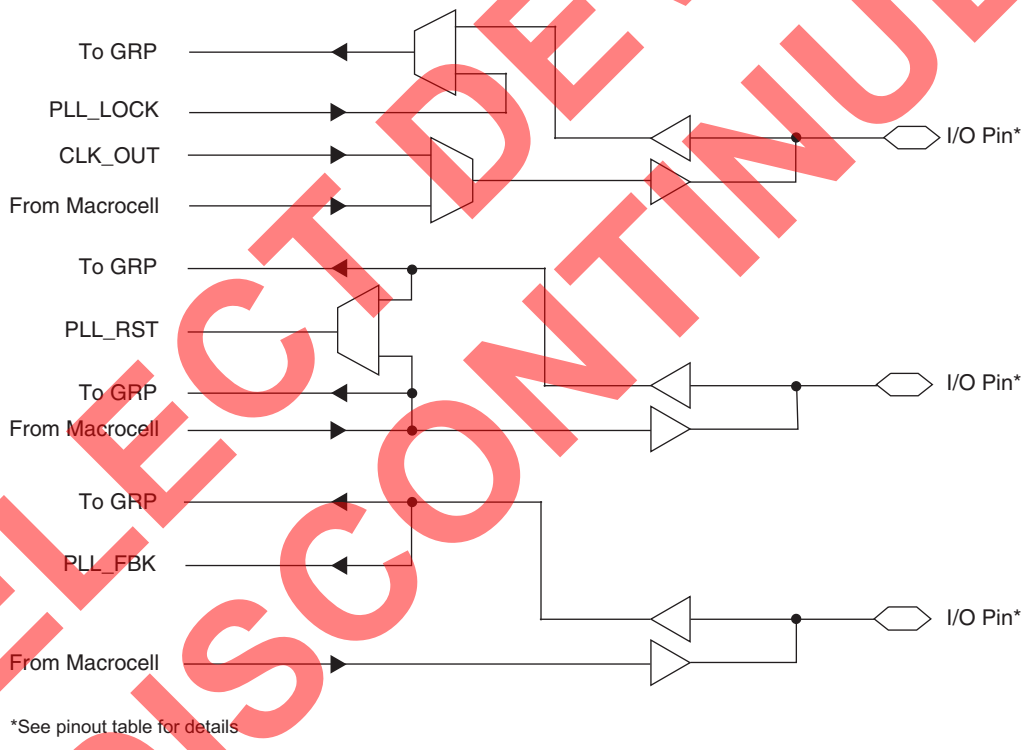


Figure 16. Connection of Optional PLL Inputs and Outputs



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

Programmable Slew Rate

The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices support two slew rates. This allows system noise and performance to be balanced in a design.

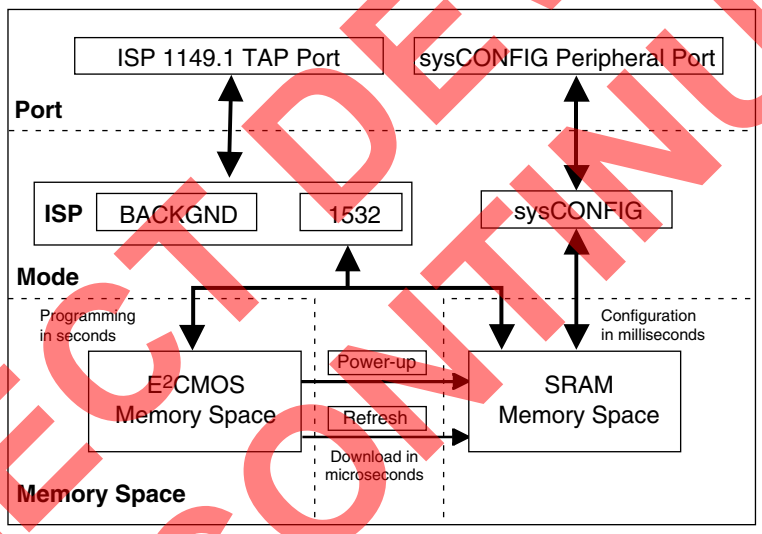
Programmable Bus-Maintenance

All general-purpose inputs have programmable bus maintenance circuitry. These are intended to maintain a valid logic level into a device when driving devices go into the tri-state mode. Four options are available for users: pull-up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device. Figure 18 shows the different ports and modes that are used in the configuration and programming of the ispXPLD 5000MX devices.

Figure 18. ispXP Block Diagram



IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfiguration of the SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during the testing of a circuit board.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

ispXPLD 5000MX Family External Switching Characteristics [1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Output Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX} [4]	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
f_{MAX} (Ext.)	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
f_{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
f_{MAX} (CAMC)[5]	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
f_{MAX} (CAM)[5]	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—	1.33	ns
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—	0.66	ns
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—	0.19	ns
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—	4.91	ns
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	2.89	—	3.21	—	3.34	—	4.82	ns
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—	1.50	ns
Optional Adjusters													
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—	0.07	ns
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—	0.99	ns
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—	0.94	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—	0.91	ns
t_{INEXP}	MFB Input Extender	t_{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—	1.16	ns
Input and Output Buffer Delays													
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables										ns
t_{IOO}	Output Buffer Selection Adder	t_{BUF}											ns
FIFO													
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—	4.00	ns
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—	8.54	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
Dual Port RAM													
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84	—	ns
t_{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDAS}$	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDAH}$	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATAAS}$	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATAAH}$	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IOI} Input Adjusters													
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t_{IOO} Output Adjusters – Output Signal Modifiers													
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t_{IOO} Output Adjusters – Output Configurations													
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
1	4N	A16/CSB	A9	B9	A17	L5
1	5P	A18/READ	A10	B10	A19	N1
1	5N	A20/CCLK	A11	B11	A21	M2
-	-	VCC	-	-	-	VCC
-	-	DONE	-	-	-	M4
1	6P	A22	A12	B12	A23	N3
1	6N	A24	A13	B13	A25	P4
1	7P	A26	A14	B14	A27	N5
1	7N	A28	A15	B15	A29	M6
-	-	PROGRAMB	-	-	-	R3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
-	-	VCCO1	-	-	-	VCC01
-	-	CFG0	-	-	-	L8
1	8P	B2	A16	B16	B3	T7
1	8N	B4	A17	B17	-	R7
1	9P	B5	A18	B18	-	N7
1	9N	B6	A19	B19	B7	P7
1	10P	B8	A20	B20	B9	T8
1	10N	B10	A21	B21	B11	R8
1	11P	B12	A22	B22	B13	M8
1	11N	B14	A23	B23	B15	P8
1	-	B16/VREF1	-	-	B17	L9
1	12P	B18	A24	B24	B19	N8
1	12N	B20	A25	B25	-	M9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	13P	B21	A26	B26	-	N10
-	-	VCCO1	-	-	-	VCCO1
1	13N	B22	A27	B27	B23	T9
1	14P	B24	A28	B28	B25	T10
1	14N	B26	A29	B29	B27	R9
-	-	VCC	-	-	-	VCC
1	15P	B28	A30	B30	B29	P9
1	15N	B30	A31	B31	B31	N9
2	16P	C0	C0	D0	C1	T11
2	16N	C2	C1	D1	C3	T12
2	17P	C4	C2	D2	-	P10
2	17N	C5	C3	D3	-	R10
2	18P	C6	C4	D4	C7	R11
-	-	VCCO2	-	-	-	VCCO2
2	18N	C8	C5	D5	C9	M10
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	19P	C10	C6	D6	C11	M11
2	19N	C12	C7	D7	C13	T13

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	GCLK0N	GCLK1	—	—	—	28	J2	P7
—	—	GND	—	—	—	29	GND	GND
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	V_{CCO1}
1	3N	A14/DATA7	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	—	—	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	—	P1[1]	V3
1	7P	A28	—	—	A29	—	M3	Y2
1	7N	A30	—	—	A31	—	L4	W3
1	8P	B0	A0	—	B1	—	N2	U5
1	8N	B2	A2	—	B3	—	P2	T5
—	—	GND (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	—	R1	U4
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	9N	B5	A6	—	—	—	R2	V4
1	10P	B6	A8	—	B7	—	T2	AA3
1	10N	B8	A10	—	B9	—	T3	AB3
1	—	B10	A12	—	B11	—	—	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	—	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7[1]	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	—	AA6
1	18N	C12	-	-	C13	—	AA7
1	19P	C10	-	-	C11	—	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	76P	L30/PLL_FBK1	L0	J0	L31	F15	E21
3	77N	M0/PLL_RST1	P27	N27	M1	H12	G22
3	77P	M2	P26	N26	M3	G14	F21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	78N	M4	P25	N25	M5	F16	H21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	78P	M6	P24	N24	-	E16	G21
-	-	GND	-	-	-	GND	GND
3	79N	M8	P23	N23	M9	G13	D22
3	79P	M10	P22	N22	M11	G12	D21
3	80N	M12	P21	N21	M13	F14	J20
3	80P	M14/CLK_OUT1	P20	N20	M15	E15	J19
3	81N	M16	N31	-	M17	F12	E20
-	-	VCC	-	-	-	VCC	VCC
3	81P	M18	N30	M30	M19	F13	F20
3	82N	M20	N29	M28	M21	D16	H17
3	82P	M22	N28	M26	M23	D15	H18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	83N	M24	N27	-	M25	—	J18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	83P	M26	N26	-	M27	—	H19
3	84N	M28	N25	-	M29	—	G20
3	84P	M30	N24	-	M31	—	G19
-	-	GND	-	-	-	GND	GND
3	85N	N0	N23	-	N1	—	C22
-	-	VCC	-	-	-	VCC	VCC
3	85P	N2	N22	-	N3	—	C21
3	86N	N4	N21	-	-	—	D20
3	86P	N6	N20	-	-	—	C19
3	87N	N8	N19	-	N9	C16	F19
3	87P	N10	N18	-	N11	B16	E19
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	88N	N12	N17	-	N13	C15	G18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	88P	N14	N16	-	N15	B15	F18
3	89N	N16	N15	-	N17	E14	B20
3	89P	N18	N14	-	N19	D14	B19
3	90N	N20	N13	-	N21	E13	A20
3	90P	N22	N12	-	N23	A15	A19
3	91N	N24	P19	N19	N25	D12	D18
3	91P	N26	P18	N18	N27	B14	C18
3	92N	N28	P17	N17	N29	C13	G17
3	92P	N30	P16	N16	N31	A14	F16

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	T1	P3
-	-	TDO	-	-	-	V1	P2
1	0P	A30	A0	C0	A31	—	P1
1	0N	A28	A1	C1	A29	—	R1
1	1P	A26	A2	C2	A27	—	P6
1	1N	A24	A3	C3	A25	—	R6
1	2P	A22	A4	C4	A23	—	P7
1	2N	A20	A5	C5	A21	—	R7
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18	A6	C6	A19	—	R4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16	A7	C7	A17	—	R5
-	-	GND	-	-	-	GND	GND
1	4P	A14	A8	C8	A15	—	R3
-	-	VCC	-	-	-	VCC	VCC
1	4N	A12	A9	C9	A13	—	R2
1	5P	A10	A10	C10	A11	—	T2
1	5N	A8	A11	C11	A9	—	T3
1	6P	A6	A12	C12	A7	—	T4
1	6N	A4	A13	C13	A5	—	T5
1	7P	A2	A14	C14	A3	—	U2
1	7N	A0	A15	C15	A1	—	U3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	8P	C30	A16	C16	C31	—	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	8N	C28	A17	C17	C29	—	U5
1	9P	C26	A18	C18	C27	—	T6
1	9N	C24	A19	C19	C25	—	U6
1	10P	C22	A20	C20	C23	—	T7
1	10N	C20	A21	C21	C21	—	U7
1	11P	C18	A22	C22	C19	—	U1
1	11N	C16	A23	C23	C17	—	V1
1	12P	C14	A24	C24	C15	—	V2
1	12N	C12	A25	C25	C13	—	V3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	13P	C10	A26	C26	C11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	13N	C8	A27	C27	C9	—	V4
-	-	GND	-	-	-	GND	GND
1	14P	C6	A28	C28	C7	—	W2
-	-	VCC	-	-	-	VCC	VCC
1	14N	C4	A29	C29	C5	—	W3
1	15P	C2	A30	C30	C3	—	W4

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.