Lattice Semiconductor Corporation - LC5256MB-4F256C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	8
Number of Macrocells	256
Number of Gates	-
Number of I/O	141
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5256mb-4f256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram

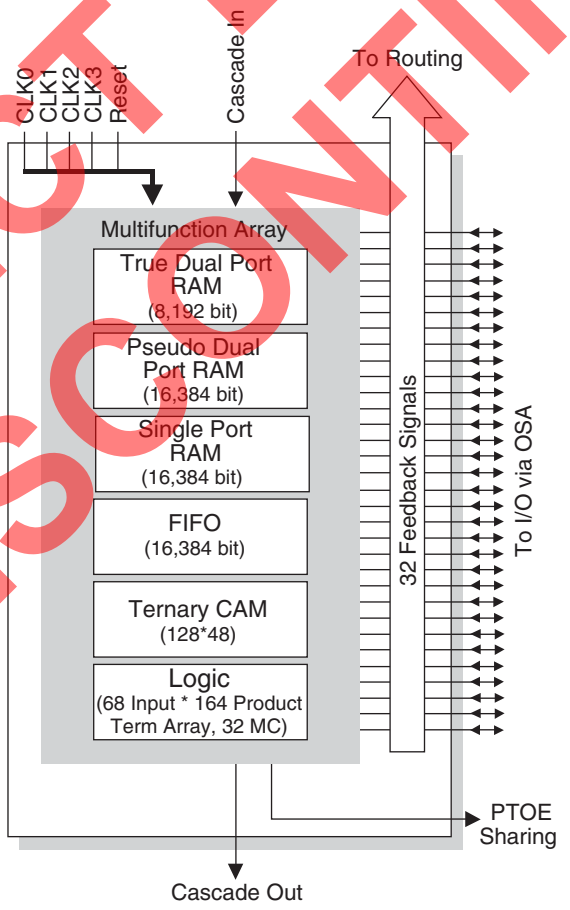


Figure 3. MFB in SuperWIDE Logic Mode†

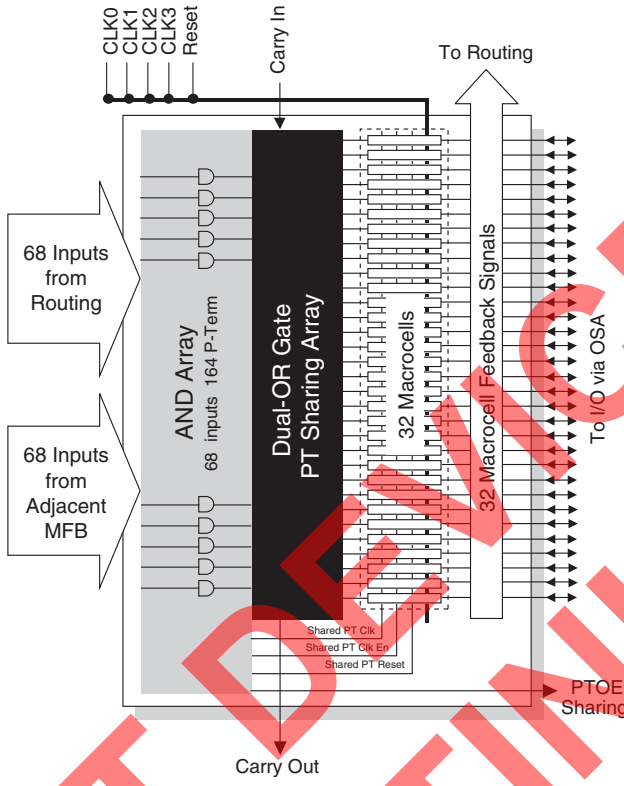


Figure 4. Macrocell Slice in Logic Mode AND-Array

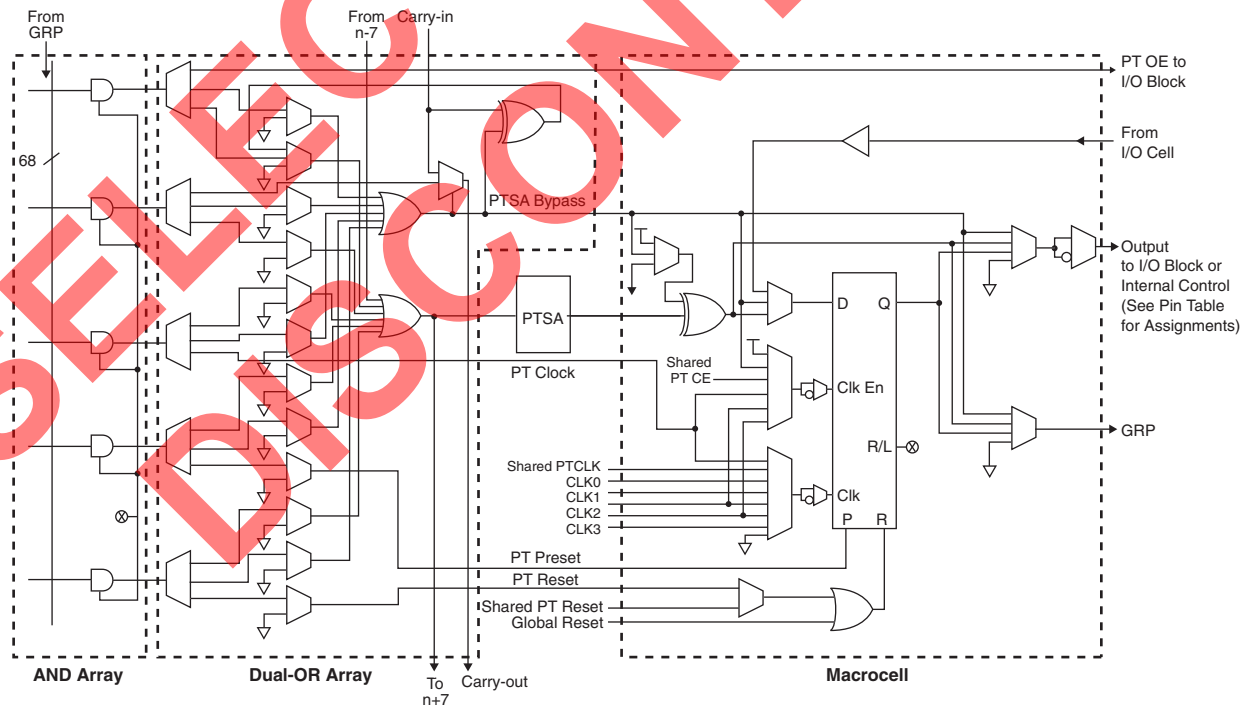


Figure 15. PLL Block Diagram

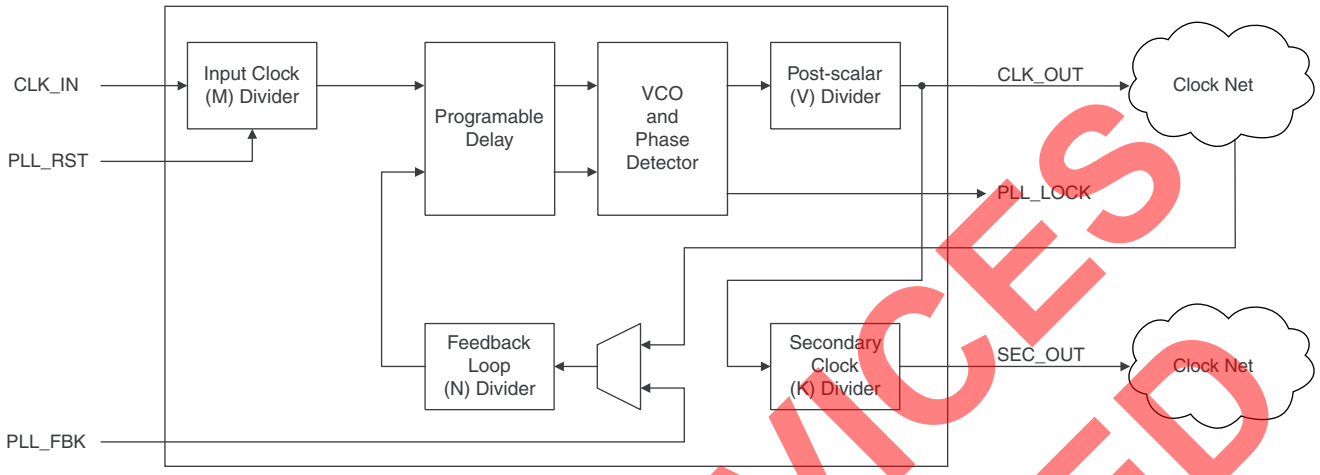
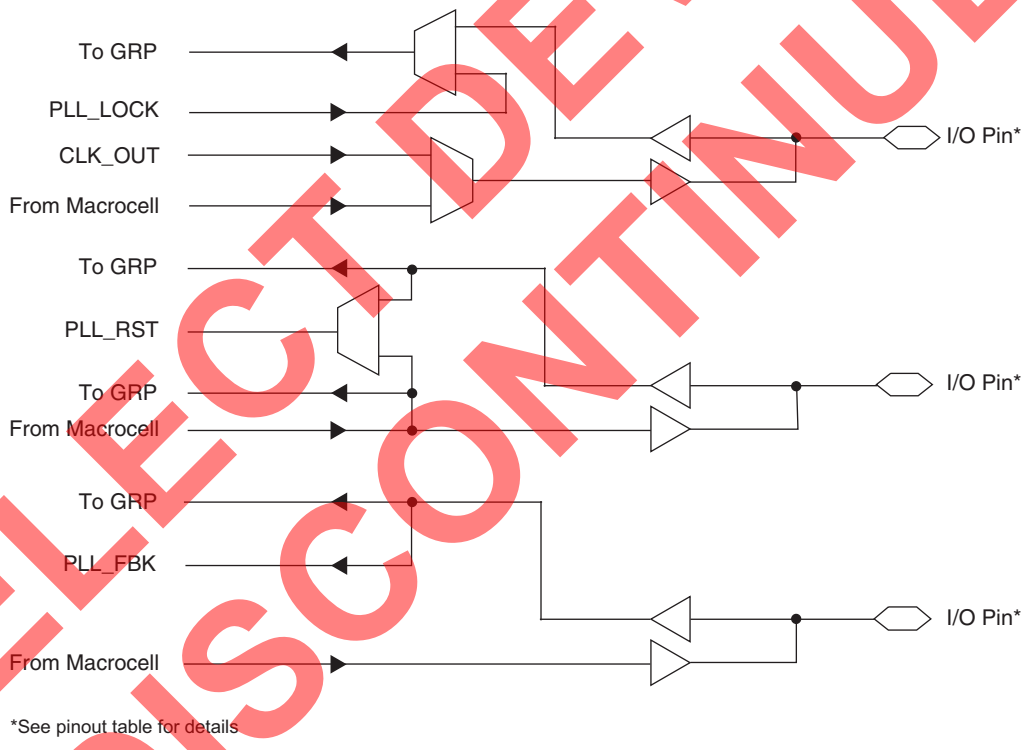


Figure 16. Connection of Optional PLL Inputs and Outputs



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

Supply Current (Continued)

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 51024						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	75	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	75	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	55	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

1. Device configured with 16-bit counters.
2. ICC varies with specific device configuration and operating frequency.
3. T_A = 25°C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[2]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	—	—	—
LVCMOS 2.5	2.3	2.5	2.7	—	—	—
LVCMOS 1.8[1]	1.65	1.8	1.95	—	—	—
LVTTL	3.0	3.3	3.6	—	—	—
PCI 3.3	3.0	3.3	3.6	—	—	—
AGP-1X	3.15	3.3	3.45	—	—	—
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	—	0.9	—
HSTL Class IV	1.4	1.5	1.6	—	0.9	—
GTL+	1.4	—	3.6	0.882	1.0	1.122
LVDS	2.3	2.5/3.3	3.6	—	—	—

1. Design tools default setting.
2. Inputs are independent of V_{CCO} setting. However, V_{CCO} must be set within the valid operating range for one of the supported standards.

ispXPLD 5000MX Family External Switching Characteristics (Continued)[1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (RAM)[5]	Clock Frequency to RAM in:											
	Single Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Dual Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—	106	MHz
f_{MAX} (FIFO)[5]	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—	132	MHz
t_{PWR_ON}	Power-on Time	—	200	—	200	—	200	—	200	—	200	µs

Timing v.1.8

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_out	Using HSTL 2.5V, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns

Timing v.1.8

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
1	4N	A16/CSB	A9	B9	A17	L5
1	5P	A18/READ	A10	B10	A19	N1
1	5N	A20/CCLK	A11	B11	A21	M2
-	-	VCC	-	-	-	VCC
-	-	DONE	-	-	-	M4
1	6P	A22	A12	B12	A23	N3
1	6N	A24	A13	B13	A25	P4
1	7P	A26	A14	B14	A27	N5
1	7N	A28	A15	B15	A29	M6
-	-	PROGRAMB	-	-	-	R3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
-	-	VCCO1	-	-	-	VCC01
-	-	CFG0	-	-	-	L8
1	8P	B2	A16	B16	B3	T7
1	8N	B4	A17	B17	-	R7
1	9P	B5	A18	B18	-	N7
1	9N	B6	A19	B19	B7	P7
1	10P	B8	A20	B20	B9	T8
1	10N	B10	A21	B21	B11	R8
1	11P	B12	A22	B22	B13	M8
1	11N	B14	A23	B23	B15	P8
1	-	B16/VREF1	-	-	B17	L9
1	12P	B18	A24	B24	B19	N8
1	12N	B20	A25	B25	-	M9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	13P	B21	A26	B26	-	N10
-	-	VCCO1	-	-	-	VCCO1
1	13N	B22	A27	B27	B23	T9
1	14P	B24	A28	B28	B25	T10
1	14N	B26	A29	B29	B27	R9
-	-	VCC	-	-	-	VCC
1	15P	B28	A30	B30	B29	P9
1	15N	B30	A31	B31	B31	N9
2	16P	C0	C0	D0	C1	T11
2	16N	C2	C1	D1	C3	T12
2	17P	C4	C2	D2	-	P10
2	17N	C5	C3	D3	-	R10
2	18P	C6	C4	D4	C7	R11
-	-	VCCO2	-	-	-	VCCO2
2	18N	C8	C5	D5	C9	M10
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	19P	C10	C6	D6	C11	M11
2	19N	C12	C7	D7	C13	T13

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
2	20P	C14	-	-	C15	P11
2	20N	C16/VREF2	-	-	C17	T14
2	21P	C18	C8	D8	C19	R12
2	21N	C20	C9	D9	-	R13
2	22P	C21	C10	D10	-	N11
2	22N	C22	C11	D11	C23	T15
2	23P	C24	C12	D12	C25	R14
2	23N	C26	C13	D13	C27	N12
2	24P	C28	C14	D14	C29	P12
2	24N	C30	C15	D15	C31	R15
-	-	VCCO2	-	-	-	VCCO2
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	25P	D0	-	-	D1	N15
2	25N	D2	-	-	D3	N14
2	26P	D4	C16	D16	-	N16
2	26N	D5	C17	D17	-	M16
2	27P	D6	C18	D18	D7	M14
2	27N	D8	C19	D19	D9	M15
-	-	VCC	-	-	-	VCC
2	28P	D10	C20	D20	D11	L13
2	28N	D12	C21	D21	D13	L12
2	29P	D14	C22	D22	D15	L15
2	29N	D16	C23	D23	D17	L16
-	-	GND	-	-	-	GND
2	30P	D18	C24	D24	D19	L14
-	-	VCCO2	-	-	-	VCCO2
2	30N	D20	C25	D25	-	K15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	31P	D21	C26	D26	-	K14
2	31N	D22	C27	D27	D23	K12
2	32P	D24	C28	D28	D25	K13
2	32N	D26	C29	D29	D27	J13
2	33P	D28	C30	D30	D29	J14
2	33N	D30	C31	D31	D31	J12
-	-	TOE	-	-	-	J15
-	-	RESET	-	-	-	J11
-	-	GOE0	-	-	-	H11
-	-	GOE1	-	-	-	H13
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3N	GCLK2	-	-	-	H15
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3P	GCLK3	-	-	-	H16

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	—	AA6
1	18N	C12	-	-	C13	—	AA7
1	19P	C10	-	-	C11	—	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	76P	L30/PLL_FBK1	L0	J0	L31	F15	E21
3	77N	M0/PLL_RST1	P27	N27	M1	H12	G22
3	77P	M2	P26	N26	M3	G14	F21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	78N	M4	P25	N25	M5	F16	H21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	78P	M6	P24	N24	-	E16	G21
-	-	GND	-	-	-	GND	GND
3	79N	M8	P23	N23	M9	G13	D22
3	79P	M10	P22	N22	M11	G12	D21
3	80N	M12	P21	N21	M13	F14	J20
3	80P	M14/CLK_OUT1	P20	N20	M15	E15	J19
3	81N	M16	N31	-	M17	F12	E20
-	-	VCC	-	-	-	VCC	VCC
3	81P	M18	N30	M30	M19	F13	F20
3	82N	M20	N29	M28	M21	D16	H17
3	82P	M22	N28	M26	M23	D15	H18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	83N	M24	N27	-	M25	—	J18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	83P	M26	N26	-	M27	—	H19
3	84N	M28	N25	-	M29	—	G20
3	84P	M30	N24	-	M31	—	G19
-	-	GND	-	-	-	GND	GND
3	85N	N0	N23	-	N1	—	C22
-	-	VCC	-	-	-	VCC	VCC
3	85P	N2	N22	-	N3	—	C21
3	86N	N4	N21	-	-	—	D20
3	86P	N6	N20	-	-	—	C19
3	87N	N8	N19	-	N9	C16	F19
3	87P	N10	N18	-	N11	B16	E19
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	88N	N12	N17	-	N13	C15	G18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	88P	N14	N16	-	N15	B15	F18
3	89N	N16	N15	-	N17	E14	B20
3	89P	N18	N14	-	N19	D14	B19
3	90N	N20	N13	-	N21	E13	A20
3	90P	N22	N12	-	N23	A15	A19
3	91N	N24	P19	N19	N25	D12	D18
3	91P	N26	P18	N18	N27	B14	C18
3	92N	N28	P17	N17	N29	C13	G17
3	92P	N30	P16	N16	N31	A14	F16

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	T1	P3
-	-	TDO	-	-	-	V1	P2
1	0P	A30	A0	C0	A31	—	P1
1	0N	A28	A1	C1	A29	—	R1
1	1P	A26	A2	C2	A27	—	P6
1	1N	A24	A3	C3	A25	—	R6
1	2P	A22	A4	C4	A23	—	P7
1	2N	A20	A5	C5	A21	—	R7
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18	A6	C6	A19	—	R4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16	A7	C7	A17	—	R5
-	-	GND	-	-	-	GND	GND
1	4P	A14	A8	C8	A15	—	R3
-	-	VCC	-	-	-	VCC	VCC
1	4N	A12	A9	C9	A13	—	R2
1	5P	A10	A10	C10	A11	—	T2
1	5N	A8	A11	C11	A9	—	T3
1	6P	A6	A12	C12	A7	—	T4
1	6N	A4	A13	C13	A5	—	T5
1	7P	A2	A14	C14	A3	—	U2
1	7N	A0	A15	C15	A1	—	U3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	8P	C30	A16	C16	C31	—	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	8N	C28	A17	C17	C29	—	U5
1	9P	C26	A18	C18	C27	—	T6
1	9N	C24	A19	C19	C25	—	U6
1	10P	C22	A20	C20	C23	—	T7
1	10N	C20	A21	C21	C21	—	U7
1	11P	C18	A22	C22	C19	—	U1
1	11N	C16	A23	C23	C17	—	V1
1	12P	C14	A24	C24	C15	—	V2
1	12N	C12	A25	C25	C13	—	V3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	13P	C10	A26	C26	C11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	13N	C8	A27	C27	C9	—	V4
-	-	GND	-	-	-	GND	GND
1	14P	C6	A28	C28	C7	—	W2
-	-	VCC	-	-	-	VCC	VCC
1	14N	C4	A29	C29	C5	—	W3
1	15P	C2	A30	C30	C3	—	W4

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3P	GCLK3	-	-	-	N16	N24
3	93N	R0	T31	R31	R1	J22	N23
3	93P	R2	T30	R30	R3	H22	N22
3	94N	R4	T29	R29	R5	N19	M26
3	94P	R6	T28	R28	R7	P15	M25
3	95N	R8	T27	R27	R9	P21	M23
3	95P	R10	T26	R26	R11	N15	M22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	96N	R12	T25	R25	R13	M15	N20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	96P	R14	T24	R24	R15	N20	M20
-	-	GND	-	-	-	GND	GND
3	97N	R16	T23	R23	R17	P22	N21
3	97P	R18	T22	R22	R19	N21	M21
3	98N	R20	T21	R21	R21	N17	M24
3	98P	R22	T20	R20	R23	M20	L24
3	99N	R24	T19	R19	R25	P17	L23
-	-	VCC	-	-	-	VCC	VCC
3	99P	R26	T18	R18	R27	P18	L22
3	100N	R28	T17	R17	R29	M21	L25
3	100P	R30	T16	R16	R31	M17	K26
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	101N	T0	T15	R15	T1	L20	K25
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	101P	T2	T14	R14	T3	N18	K24
3	102N	T4	T13	R13	T5	L21	K23
3	102P	T6	T12	R12	T7	M18	K22
3	103N	T8	T11	R11	T9	L22	J25
3	103P	T10	T10	R10	T11	L17	J24
3	104N	T12	T9	R9	T13	K22	L21
3	104P	T14	T8	R8	T15	L18	K21
3	105N	T16	T7	R7	T17	K21	L20
3	105P	T18	T6	R6	T19	K18	K20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	T20	T5	R5	T21	K20	J23
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	T22	T4	R4	T23	K17	J22
3	107N	T24	T3	R3	T25	K19	J26
3	107P	T26	T2	R2	T27	J17	H26
3	108N	T28	T1	R1	T29	E22	H25
3	108P	T30/PLL_FBK1	T0	R0	T31	E21	H24
3	109N	U0/PLL_RST1	X27	V27	U1	G22	H23
3	109P	U2	X26	V26	U3	F21	H22

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.