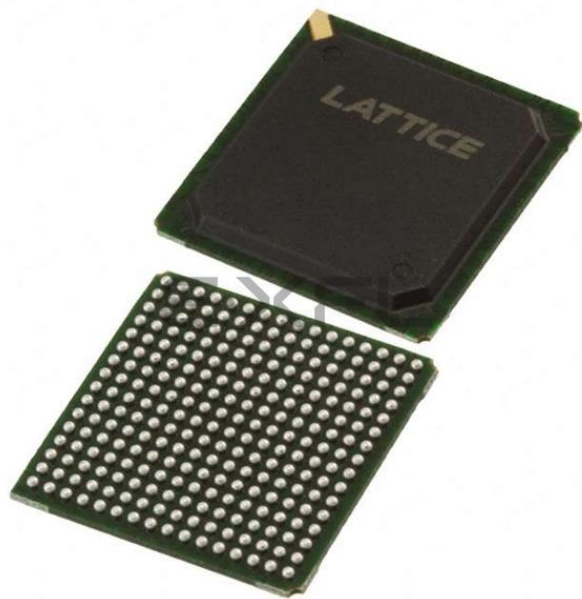




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	8
Number of Macrocells	256
Number of Gates	-
Number of I/O	141
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5256mb-5fn256i



Product Line	Ordering Part Number	Product Status	Reference PCN
LC51024MV	LC51024MV-52F484C	Active / Orderable	
	LC51024MV-52FN484C		
	LC51024MV-75F484C		
	LC51024MV-75FN484C		
	LC51024MV-75F484I		
	LC51024MV-75FN484I		
	LC51024MV-52F672C		
	LC51024MV-52FN672C		
	LC51024MV-75F672C		
	LC51024MV-75FN672C		
	LC51024MV-75F672I		
	LC51024MV-75FN672I		
LC51024MB	LC51024MB-52F484C	Discontinued	PCN#09-10
	LC51024MB-52FN484C		
	LC51024MB-75F484C		
	LC51024MB-75FN484C		
	LC51024MB-75F484I		
	LC51024MB-75FN484I		
	LC51024MB-52F672C		
	LC51024MB-52FN672C		
	LC51024MB-75F672C		
	LC51024MB-75FN672C		
	LC51024MB-75F672I		
	LC51024MB-75FN672I		
LC51024MC	LC51024MC-52F484C	Discontinued	PCN#09-10
	LC51024MC-52FN484C		
	LC51024MC-75F484C		
	LC51024MC-75FN484C		
	LC51024MC-75F484I		
	LC51024MC-75FN484I		
	LC51024MC-52F672C		
	LC51024MC-52FN672C		
	LC51024MC-75F672C		
	LC51024MC-75FN672C		
	LC51024MC-75F672I		
	LC51024MC-75FN672I		

Features

■ Flexible Multi-Function Block (MFB)

Architecture

- SuperWIDE™ logic (up to 136 inputs)
- Arithmetic capability
- Single- or Dual-port SRAM
- FIFO
- Ternary CAM

■ sysCLOCK™ PLL Timing Control

- Multiply and divide between 1 and 32
- Clock shifting capability
- External feedback capability

■ sysIO™ Interfaces

- LVCMOS 1.8, 2.5, 3.3V
 - Programmable impedance
 - Hot-socketing
 - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
 - Open drain operation
- SSTL 2, 3 (I & II)
- HSTL (I, III, IV)
- PCI 3.3
- GTL+
- LVDS
- LVPECL
- LVTTTL

■ Expanded In-System Programmability (ispXP™)

- Instant-on capability
- Single chip convenience
- In-System Programmable via IEEE 1532 Interface
- Infinitely reconfigurable via IEEE 1532 or sys-CONFIG™ microprocessor interface
- Design security

■ High Speed Operation

- 4.0ns pin-to-pin delays, 300MHz f_{MAX}
- Deterministic timing

■ Low Power Consumption

- Typical static power: 20 to 50mA (1.8V), 30 to 60mA (2.5/3.3V)
- 1.8V core for low dynamic power

■ Easy System Integration

- 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
- 5V tolerant I/O for LVCMOS 3.3 and LVTTTL interfaces
- IEEE 1149.1 interface for boundary scan testing
- sysIO quick configuration
- Density migration
- Multiple density and package options
- PQFP and fine pitch BGA packaging
- Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	3.7ns
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	250MHz
Functional Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Figure 1. ispXPLD 5000MX Block Diagram



Introduction

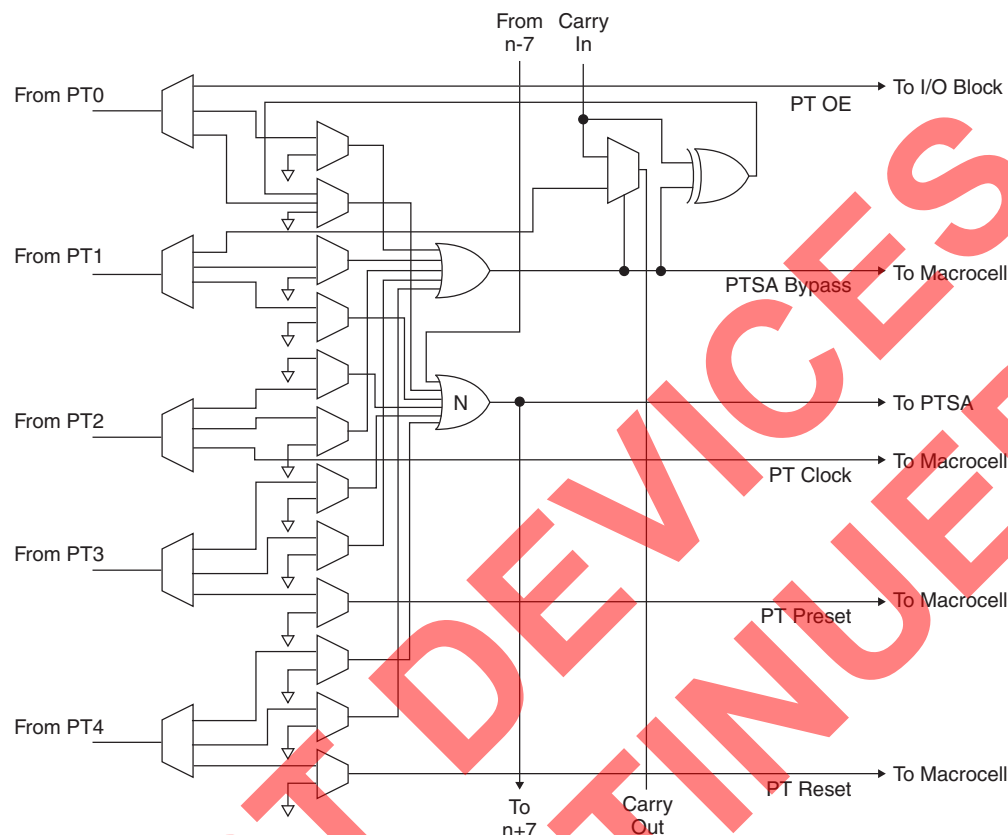
The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

Figure 6. Dual-OR PT Sharing Array

Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

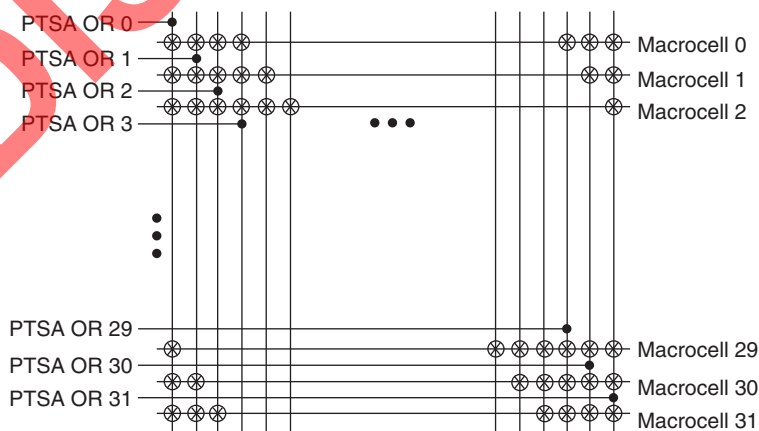
Figure 7. Product Term Sharing Array (PTSA)

Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size ¹
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output

The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation

In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width

Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching

All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

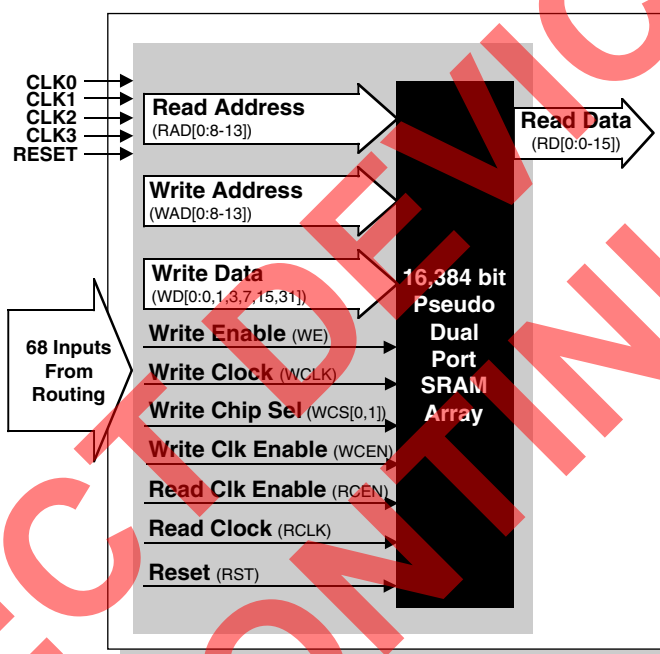


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

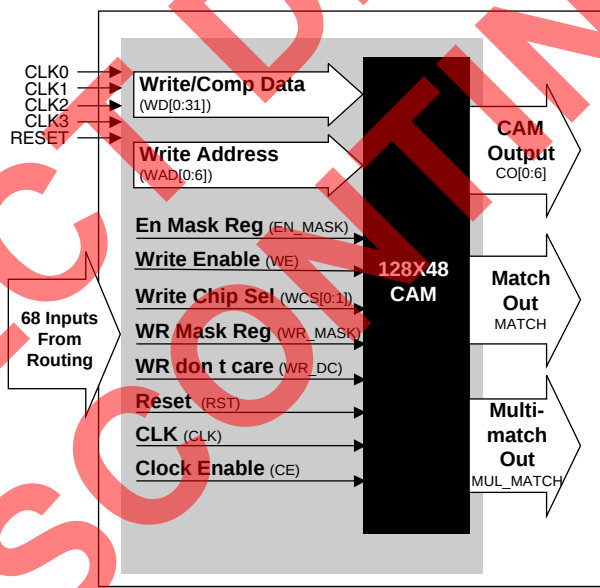


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

ispXPLD 5000MX Family External Switching Characteristics^{1, 2, 3}

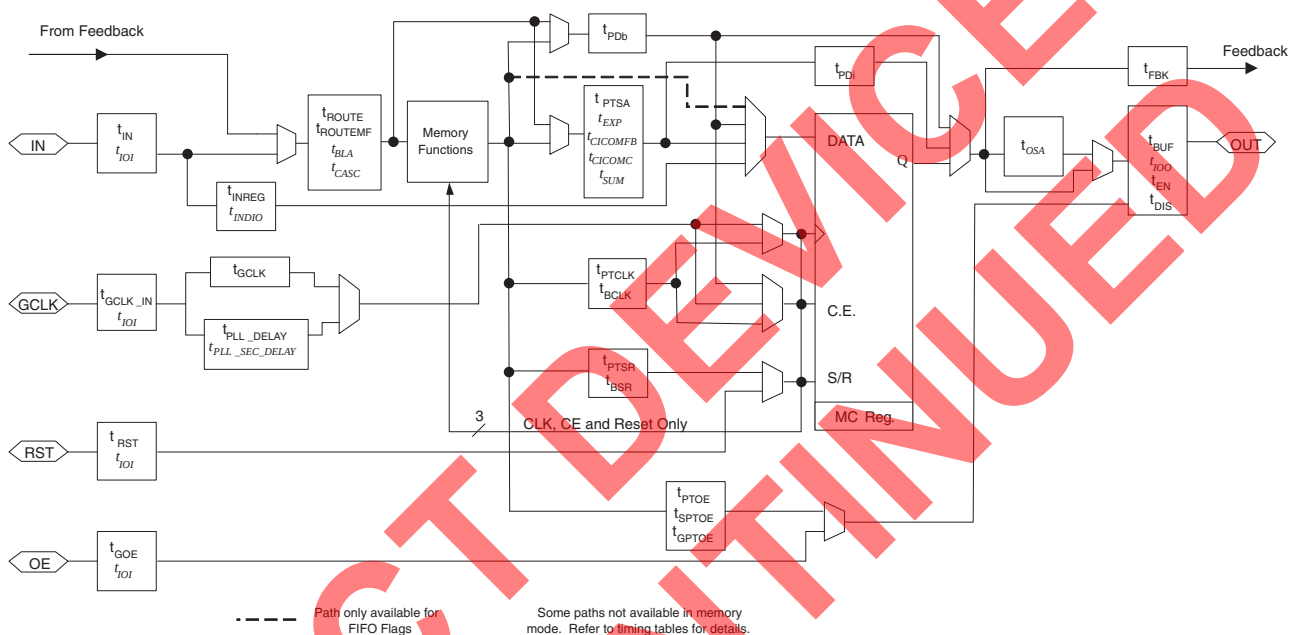
Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Out-put Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX}^4	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
$f_{MAX} (Ext.)$	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
$f_{MAX} (Tog.)$	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
$f_{MAX} (CAMC)^5$	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
$f_{MAX} (CAM)^5$	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model shown in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{FIFOWES}	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
t _{FIFOWEH}	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{FIFORES}	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
t _{FIFOREH}	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
t _{FIFORSTO}	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
t _{FIFORSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
t _{FIFORSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
t _{FIFORCLKO}	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t _{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t _{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMENMSKS}	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMENMSKH}	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMADDS}	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMADDH}	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMDATAS}	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
t _{CAMDATAH}	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMDACS}	“Don’t Care” Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMDCH}	“Don’t Care” Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t _{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVC MOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
LVC MOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVC MOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVC MOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVC MOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVC MOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVC MOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVC MOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVC MOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVC MOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
GTL+_out	Using GTL+	t_{IOBUF} , t_{IOEN} , t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Power Estimation Equations

$$ICC = ICC_DC + IMFB_CPLD + IMFB_SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL_D$$

ICC_DC

Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) from the data sheet.

IMFB_CPLD

$$= ((K0 * CPLD \text{ MFB inputs} + K1 * CPLD \text{ Logical Product Terms} + K2 * CPLD \text{ GRP from MFB} + K3 * CPLD \text{ GRP from IFB}) * AF + K4) * \text{FREQ} / 1000\mu\text{A}/\text{mA}$$

IMFB_CAM

$$= \text{CAM Memory MFBs} * ((\text{FREQ} * K8) + K9) \text{ (CAM operating in typical mode)}$$

IMFB_SRAM/PDPRAM/FIFO

$$= (\text{WR_PERCENT} * (K1 + \text{WR_PERCENT} * 8 * K0 + K10 + K11) + \text{RD_PERCENT} * (K1 + 128 * \text{RD_PERCENT} * K0 + 8 * \text{OSW_PERCENT} * K2)) * \text{SRAM/PDPRAM/FIFO Memory MFBs} * \text{FREQ} / 1000\mu\text{A}/\text{mA}$$

IMFB_DPRAM

$$= (\text{WR_PERCENT} * (2 * K1 + 2 * \text{WR_PERCENT} * 8 * K0 + K10 + K11) + \text{RD_PERCENT} * (2 * K1 + 2 * 128 * \text{RD_PERCENT} * K0 + 8 * \text{OSW_PERCENT} * K2)) * \text{DPRAM Memory MFBs} * \text{FREQ} / 1000\mu\text{A}/\text{mA}$$

IPLL_D

$$= K5 * \text{PLL_FREQ} * \text{number of PLLs used. IPLL_D is the PLL digital component of the VCC supply current.}$$

Analog portion of PLL supply current consumption, from PLL power pin:

$$IPLL_A = (K6 * \text{PLL_FREQ} + K7) * \text{number of PLLs used}$$

Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	B4
0	109P	O28	O10	P16	O29	1	E4	A4
0	110N	O26	M17	O17	O27	2	B1	B3
0	110P	O24	M16	O16	O25	3	C1	A3
0	111N	O22	M15	O15	O23	4	D3	F5
—	—	V _{CC00}	—	—	—	5	V _{CC00}	V _{CC00}
0	111P	O20	M14	O14	O21	6	C2	G6
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	GND (Bank 0)
0	112N	O18	M13	O13	O19	8	E3	H6
0	112P	O16	M12	O12	O17	9	D2	G5
0	113N	O14	O9	P14	O15	—	—	D3
0	113P	O12	O8	P12	O13	—	—	D2
0	114N	O10	O7	P10	O11	—	—	E4
0	114P	O8	O6	P8	O9	—	—	E3
0	115N	O6	O5	P6	O7	—	—	F4
0	115P	O4	O4	P4	O5	—	—	G4
0	116N	O2	O3	P2	O3	—	—	C2
—	—	V _{CC00}	—	—	—	—	V _{CC00}	V _{CC00}
0	116P	O0	O2	P0	O1	—	—	C1
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	117N	P30	O1	—	P31	—	D1	F3
0	117P	P28	O0	—	P29	—	E1	G3
0	118N	P26	O31	—	P27	—	F4	H4
—	—	V _{CC}	—	—	—	10	V _{CC}	V _{CC}
0	118P	P24	O30	—	P25	—	F5	J4
0	119N	P22	M11	O11	P23	11	E2	H5
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	J5
0	120N	P18	M9	O9	P19	13	F1	E2
0	120P	P16	M8	O8	P17	14	G1	F2
—	—	GND	—	—	—	15	GND	GND
0	121N	P14	M7	O7	P15	16	F3	D1
—	—	V _{CC00}	—	—	—	17	V _{CC00}	V _{CC00}
0	121P	P12	M6	O6	P13	18	G5	E1
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	GND (Bank 0)
0	122N	P10	M5	O5	P11	20	H5	J3
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	H2
0	123N	P6	—	—	P7	22	G3	G2
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	G1
0	124N	P2	—	—	P3	24	G2	H1
0	124P	P0	—	—	P1	25	H1	J1
—	GCLK0P	GCLK0	—	—	—	26	H2	N7
—	—	V _{CCJ}	—	—	—	See Power Supply and NC Connections Table		

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	V19
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	—	—	V20
—	—	V _{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	—	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V _{CCO2}	—	—	—	121	V _{CCO2}	V _{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V _{CCP}	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	V _{CCO3}	—	—	—	146	V _{CCO3}	V _{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	61N	I14	I23	K23	I15	149	G13	D22
3	61P	I12	I22	K22	I13	150	G12	D21
3	62N	I10	I21	K21	I11	151	F14	J20
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	J19
3	63N	I6	K31	—	I7	—	F12	E20
—	—	V _{CC}	—	—	—	153	V _{CC}	V _{CC}
3	63P	I4	K30	L30	I5	—	F13	F20
3	64N	I2	K29	L28	I3	—	D16	H17
3	64P	I0	K28	L26	I1	—	D15	H18
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	65N	J30	K27	—	J31	—	—	J18
—	—	V _{CCO3}	—	—	—	—	V _{CCO3}	V _{CCO3}
3	65P	J28	K26	—	J29	—	—	H19
3	66N	J26	K25	—	J27	—	—	G20
3	66P	J24	K24	—	J25	—	—	G19
3	67N	J22	K23	—	J23	—	—	C22
3	67P	J20	K22	—	J21	—	—	C21
3	68N	J18	K21	—	J19	—	—	D20
3	68P	J16	K20	—	J17	—	—	C19
3	69N	J14	K19	—	J15	—	C16	F19
3	69P	J12	K18	—	J13	—	B16	E19
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	70N	J10	K17	—	J11	—	C15	G18
—	—	V _{CCO3}	—	—	—	—	V _{CCO3}	V _{CCO3}
3	70P	J8	K16	—	J9	—	B15	F18
3	71N	J6	K15	—	J7	—	E14	B20
3	71P	J4	K14	—	J5	—	D14	B19
3	72N	J2	K13	—	J3	—	E13	A20
3	72P	J0	K12	—	J1	—	A15	A19
3	73N	K30	I19	K19	K31	154	D12	D18
3	73P	K28	I18	K18	K29	155	B14	C18
3	74N	K26	I17	K17	K27	156	C13	G17
3	74P	K24	I16	K16	K25	157	A14	F16
3	75N	K22	I31	K31	K23	158	A13	E17
3	75P	K21	I30	K30	—	159	B13	D17
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	GND (Bank 3)
3	76N	K20	K11	L21	—	—	D11	B18
—	—	V _{CCO3}	—	—	—	161	V _{CCO3}	V _{CCO3}
3	76P	K18	K10	L20	K19	—	B12	A18
3	77N	K16	K9	L18	K17	—	C12	C17
3	77P	K14	K8	L16	K15	—	E11	B17
3	78N	K12	K7	L12	K13	—	—	C16
3	78P	K10	K6	L10	K11	—	—	B16

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	J6	T1
-	-	TDO	-	-	-	K2	V1
1	0P	A30/DATA0	C0	A0	A31	K3	W1
1	0N	A28/DATA1	C1	A1	A29	J3	Y1
1	1P	A26/DATA2	C2	A2	A27	J5	P3
1	1N	A24/DATA3	C3	A3	A25	J4	R3
1	2P	A22/DATA4	C4	A4	A23	L2	T2
1	2N	A20/DATA5	C5	A5	A21	M1	U2
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18/DATA6	C6	A6	A19	K4	V2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16/DATA7	C7	A7	A17	L3	W2
-	-	GND	-	-	-	GND	GND
1	4P	A14/INITB	C8	A8	A15	K5	R4
1	4N	A12/CSB	C9	A9	A13	L5	T4
1	5P	A10/READ	C10	A10	A11	N1	R6
1	5N	A8/CCLK	C11	A11	A9	M2	R5
1	6P	A6	-	-	A7	—	U3
-	-	VCC	-	-	-	VCC	VCC
1	6N	A4	-	-	A5	P1	V3
1	7P	A2	-	-	A3	M3	Y2
1	7N	A0	-	-	A1	L4	W3
1	8P	B30	D0	-	B31	N2	U5
1	8N	B28	D2	-	B29	P2	T5
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	9P	B26	D4	-	B27	R1	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	9N	B24	D6	-	B25	R2	V4
1	10P	B22	D8	-	B23	T2	AA3
1	10N	B20	D10	-	B21	T3	AB3
1	-	B18	D12	-	B19	—	Y4
-	-	DONE	-	-	-	M4	AA4
1	11P	B14	-	-	B15	—	AB2
1	11N	B12	-	-	B13	—	U6
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	12P	B10	-	-	B11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	12N	B8	-	-	B9	—	W6
1	13P	B6	C12	A12	B7	N3	AB4
1	13N	B4	C13	A13	B5	P4	AB5
1	14P	B2	C14	A14	B3	N5	T6
1	14N	B0	C15	A15	B1	M6	U7
-	-	PROGRAMB	-	-	-	R3	W5

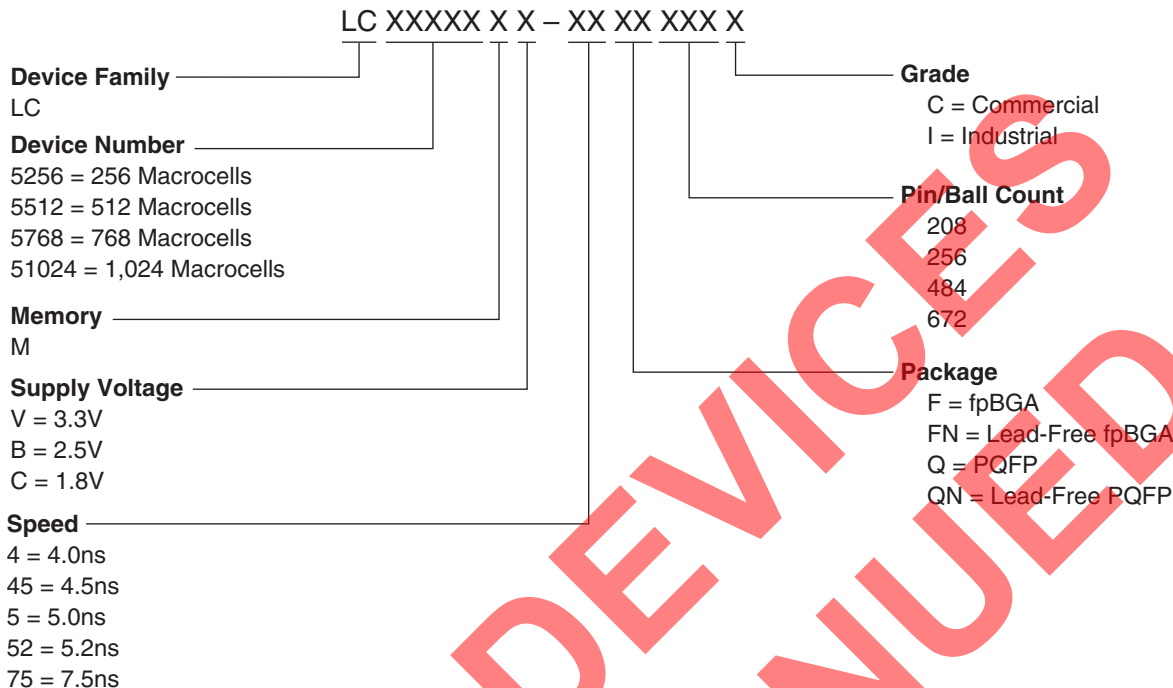
ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	110N	U4	X25	V25	U5	H21	J21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	110P	U6	X24	V24	U7	G21	H21
-	-	GND	-	-	-	GND	GND
3	111N	U8	X23	V23	U9	D22	G25
3	111P	U10	X22	V22	U11	D21	G24
3	112N	U12	X21	V21	U13	J20	G23
3	112P	U14/CLK_OUT1	X20	V20	U15	J19	G22
3	113N	U16	V31	-	U17	E20	J20
-	-	VCC	-	-	-	VCC	VCC
3	113P	U18	V30	U30	U19	F20	H20
3	114N	U20	V29	U28	U21	H17	G26
3	114P	U22	V28	U26	U23	H18	F25
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	115N	U24	V27	-	U25	J18	F24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	115P	U26	V26	-	U27	H19	F23
3	116N	U28	V25	-	U29	G20	G21
3	116P	U30	V24	-	U31	G19	F22
-	-	GND	-	-	-	GND	GND
3	117N	V0	V23	-	V1	C22	F26
-	-	VCC	-	-	-	VCC	VCC
3	117P	V2	V22	-	V3	C21	E26
3	118N	V4	V21	-	V5	D20	E25
3	118P	V6	V20	-	V7	C19	E24
3	119N	V8	V19	-	V9	F19	E23
3	119P	V10	V18	-	V11	E19	E22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	120N	V12	V17	-	V13	G18	D26
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	120P	V14	V16	-	V15	F18	D25
3	121N	V16	V15	-	V17	B20	D24
3	121P	V18	V14	-	V19	B19	D23
3	122N	V20	V13	-	V21	A20	C26
3	122P	V22	V12	-	V23	A19	C25
3	123N	V24	X19	V19	V25	D18	G19
3	123P	V26	X18	V18	V27	C18	F19
3	124N	V28	X17	V17	V29	G17	G18
3	124P	V30	X16	V16	V31	F16	F18
3	125N	W0	X31	V31	W1	E17	F20
3	125P	W2	X30	V30	W3	D17	E20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)

Part Number Description



Ordering Information

Note: For voltage families offered in industrial temperature grades and for all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -45XXXXC is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only. In addition, the fastest commercial speed grade (-5) for the LC5768MB/MV devices, at Lattice's discretion, will utilize either a commercial grade only single-mark or a dual-mark format in conjunction with the slower industrial speed grade (-75).

Conventional Packaging

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	141	C
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	141	C
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	141	C
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	149	C
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	149	C
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	193	C
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	193	C
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	253	C
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	253	C

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193	I
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193	C
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193	C
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317	C
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193	I
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I