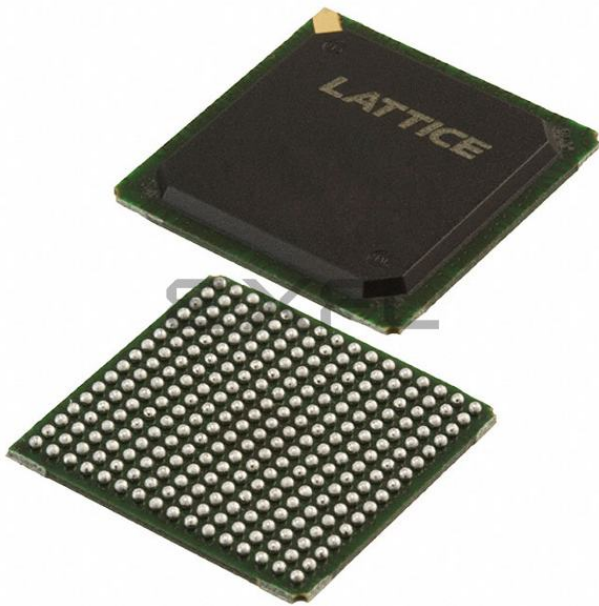




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	256
Number of Gates	-
Number of I/O	141
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5256mv-5f256c

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram

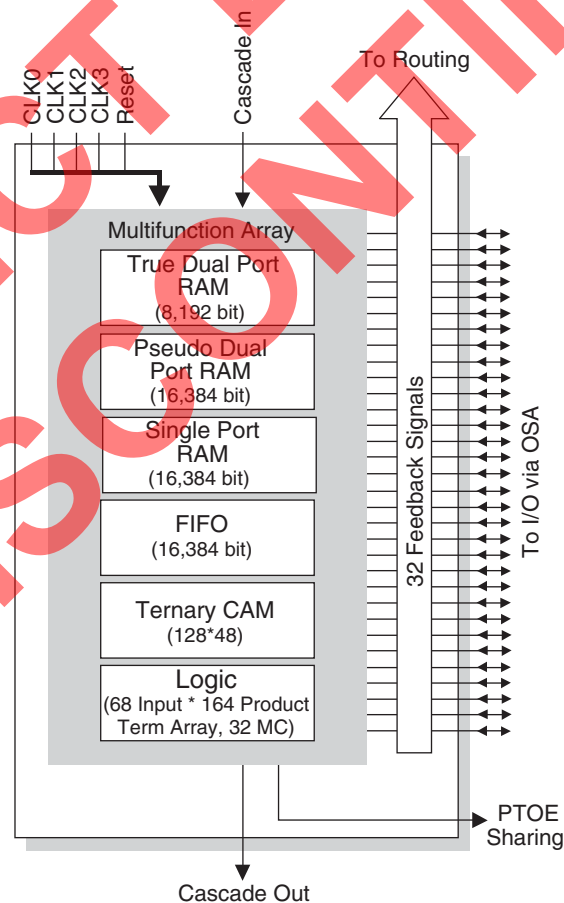
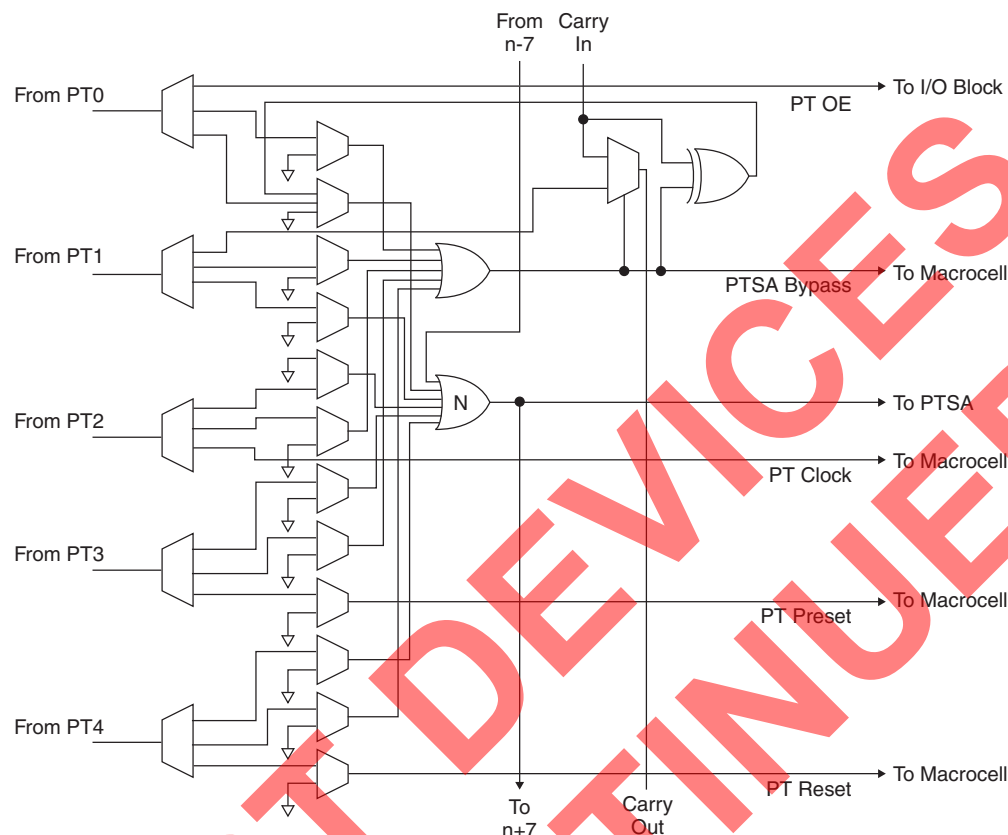


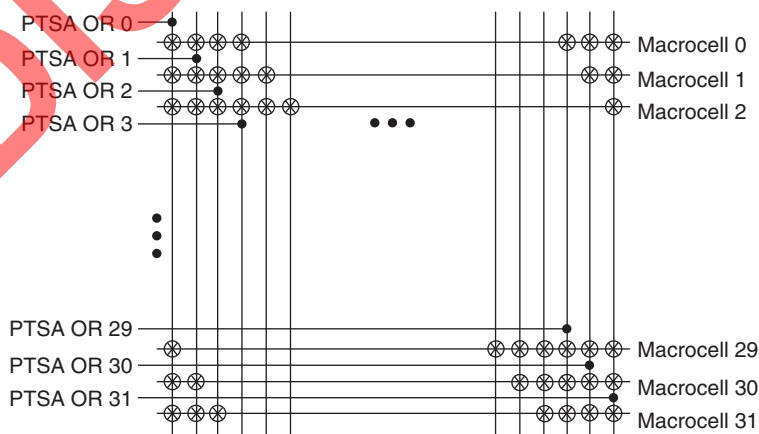
Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

Figure 7. Product Term Sharing Array (PTSA)



Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

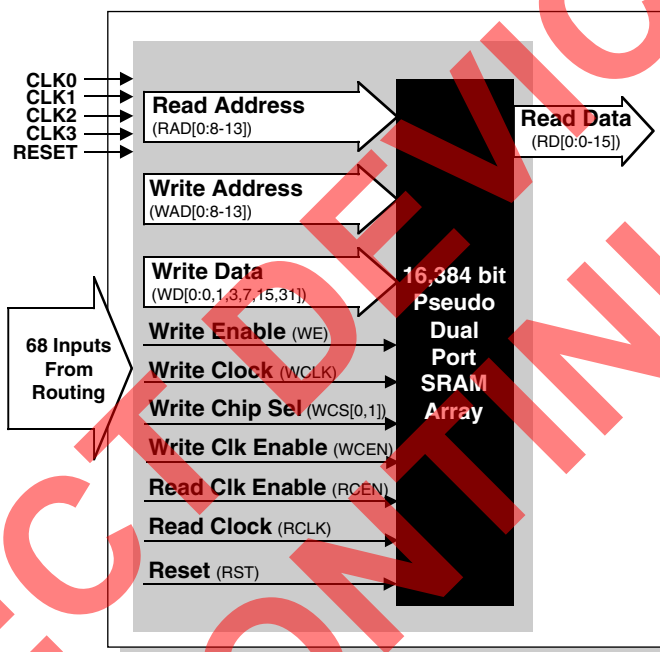


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

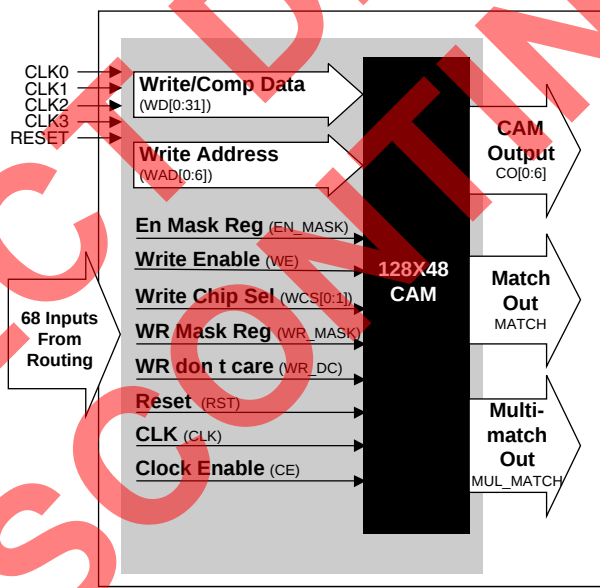
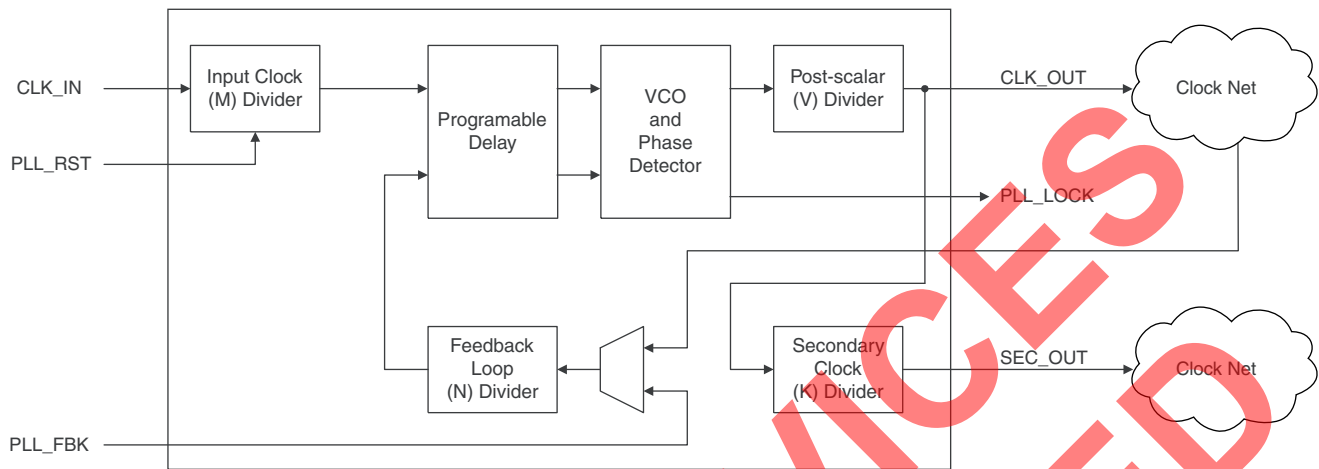
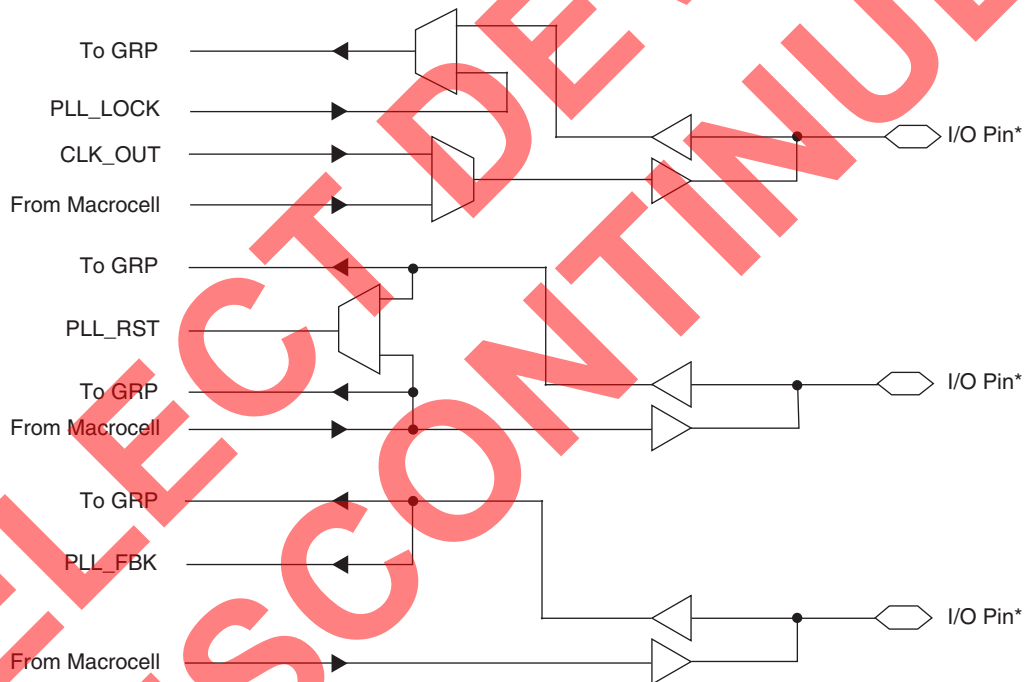


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

Figure 15. PLL Block Diagram**Figure 16. Connection of Optional PLL Inputs and Outputs**

*See pinout table for details

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, [sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices](#).

Figure 17. I/O Cell



Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 12 lists the sysIO standards with the typical values for V_{CCO} , V_{REF} and V_{TT} . For more information on the sysIO capability, refer to TN1000, [sysIO Usage Guidelines for Lattice Devices](#).

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

Programmable Slew Rate

The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices support two slew rates. This allows system noise and performance to be balanced in a design.

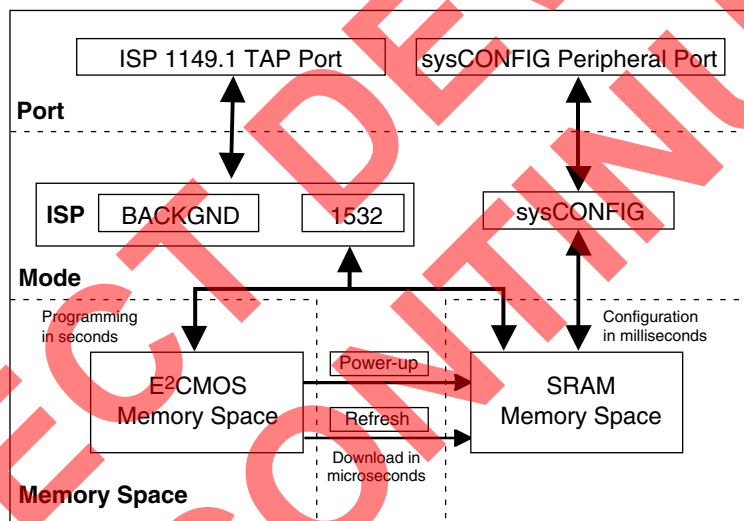
Programmable Bus-Maintenance

All general-purpose inputs have programmable bus maintenance circuitry. These are intended to maintain a valid logic level into a device when driving devices go into the tri-state mode. Four options are available for users: pull-up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device. Figure 18 shows the different ports and modes that are used in the configuration and programming of the ispXPLD 5000MX devices.

Figure 18. ispXP Block Diagram



IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfiguration of the SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during the testing of a circuit board.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}^1	Input or I/O Leakage	$0 \leq V_{IN} \leq (V_{CCO} - 0.2V)$	—	—	10	μA
		$(V_{CCO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	40	μA
I_{IH}^4	Input High Leakage Current	$3.6V < V_{IN} \leq 5.5V$ and $3.0V \leq V_{CCO} \leq 3.6V$	—	—	3	mA
I_{PU}^3	I/O Active Pullup Current	$0 \leq V_{IN} \leq 0.7 V_{CCO}$	-30	—	-150	μA
I_{PD}	I/O Active Pulldown Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	μA
C1	I/O Capacitance ²	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C2	Clock Capacitance ²	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf
C3	Global Input Capacitance ²	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. $T_A = 25^\circ C$, $f = 1.0MHz$

3. I_{PU} on JTAG pins has a maximum of $-175\mu A$ for 5512MX devices.

4. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \leq V_{CCO} \leq 3.6V$. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

ispXPLD 5000MX Family External Switching Characteristics (Continued)^{1, 2, 3}**Over Recommended Operating Conditions**

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (RAM) ⁵	Clock Frequency to RAM in:											
	Single Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Dual Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—	106	MHz
f_{MAX} (FIFO) ⁵	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—	132	MHz
$t_{\text{PWR_ON}}$	Power-on Time	—	200	—	200	—	200	—	200	—	200	μs

Timing v.1.8

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—	1.33	ns
t _{CICOMFB}	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—	0.66	ns
t _{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—	0.19	ns
t _{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—	4.91	ns
t _{FLAGEXP}	Additional Flag Delay when Expanding Data Widths	t _{FLAGFULL} , t _{FLAGAFULL} , t _{FLAGEMPTY} , t _{FLAGAEMPTY}	—	2.57	—	2.89	—	3.21	—	3.34	—	4.82	ns
t _{SUM}	Counter Sum Delay	t _{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—	1.50	ns
Optional Adjusters													
t _{BLA}	Block Loading Adder	t _{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—	0.07	ns
t _{EXP}	PT Expander Adder	t _{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—	0.99	ns
t _{INDIO}	Additional Delay for the Input Register	t _{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—	0.94	ns
t _{PLL_SEC_DELAY}	Secondary PLL Output Delay	t _{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—	0.91	ns
t _{INEXP}	MFB Input Extender	t _{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—	1.16	ns
Input and Output Buffer Delays													
t _{IOI}	Input Buffer Selection Adder	t _{GCLK_IN} , t _{IN} , t _{GOE} , t _{RST}	Refer to sysIO Adjuster Tables										ns
t _{IOO}	Output Buffer Selection Adder	t _{BUF}											ns
FIFO													
t _{FIFOWCLKS}	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{FIFOWCLKH}	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{FIFOCLKSKEW}	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	ns
t _{FIFOFULL}	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—	4.00	ns
t _{FIFOAFULL}	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
t _{FIFOEMPTY}	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
t _{FIFOAEMPTY}	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{IOI} Input Adjusters													
LVTTTL_in	Using 3.3V TTL	t _{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS_18_in	Using 1.8V CMOS	t _{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS_25_in	Using 2.5V CMOS	t _{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS_33_in	Using 3.3V CMOS	t _{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t _{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t _{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t _{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t _{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t _{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t _{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t _{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Volt- age Differential Signaling (LVDS)	t _{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t _{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t _{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t _{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t _{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t _{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t _{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t _{IOO} Output Adjusters – Output Signal Modifiers													
Slow Slew	Using Slow Slew (LVTTTL and LVC MOS Outputs Only)	t _{IOBUF} , t _{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t _{IOO} Output Adjusters – Output Configurations													
LVTTTL_out	Using 3.3V TTL Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVC MOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVC MOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTTL and LVCMOS Standards



Table 14. Test Fixture Required Components

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	V _{CCO} /2	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = V _{CCO} /2	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = V _{CCO} /2	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	V _{CCO} /2	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	V _{CCO} /2	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V _{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V _{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPLD 5256MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
0	61N	H30	G17	H17	H31	B1
0	61P	H28	G16	H16	H29	C1
0	62N	H26	G15	H15	H27	D3
0	62P	H24	G14	H14	H25	C2
0	63N	H22	G13	H13	H23	E3
0	63P	H21	G12	H12	-	D2
-	-	VCC	-	-	-	VCC
0	64N	H20	G11	H11	-	E2
0	64P	H18/CLK_OUT0	G10	H10	H19	F2
0	65N	H16	G9	H9	H17	F1
0	65P	H14	G8	H8	H15	G1
-	-	GND	-	-	-	GND
0	66N	H12	G7	H7	H13	F3
-	-	VCCO0	-	-	-	VCCO0
0	66P	H10	G6	H6	H11	G5
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	67N	H8	G5	H5	H9	H5
0	67P	H6/PLL_RST0	G4	H4	H7	G4
0	68N	H5	-	-	-	G3
0	68P	H4/PLL_FBK0	-	-	-	H3
0	69N	H2	-	-	H3	G2
0	69P	H0	-	-	H1	H1
-	GCLK0P	GCLK0	-	-	-	H2
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table
-	GCLK0N	GCLK1	-	-	-	J2
-	-	GND	-	-	-	GND
-	-	TDI	-	-	-	H6
-	-	TMS	-	-	-	H4
-	-	TCK	-	-	-	J6
-	-	TDO	-	-	-	K2
1	0P	A0/DATA0	A0	B0	A1	K3
1	0N	A2/DATA1	A1	B1	A3	J3
1	1P	A4/DATA2	A2	B2	-	J5
1	1N	A5/DATA3	A3	B3	-	J4
1	2P	A6/DATA4	A4	B4	A7	L2
1	2N	A8/DATA5	A5	B5	A9	M1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	3P	A10/DATA6	A6	B6	A11	K4
-	-	VCCO1	-	-	-	VCCO1
1	3N	A12/DATA7	A7	B7	A13	L3
-	-	GND	-	-	-	GND
1	4P	A14/INITB	A8	B8	A15	K5

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
2	20P	C14	-	-	C15	P11
2	20N	C16/VREF2	-	-	C17	T14
2	21P	C18	C8	D8	C19	R12
2	21N	C20	C9	D9	-	R13
2	22P	C21	C10	D10	-	N11
2	22N	C22	C11	D11	C23	T15
2	23P	C24	C12	D12	C25	R14
2	23N	C26	C13	D13	C27	N12
2	24P	C28	C14	D14	C29	P12
2	24N	C30	C15	D15	C31	R15
-	-	VCCO2	-	-	-	VCCO2
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	25P	D0	-	-	D1	N15
2	25N	D2	-	-	D3	N14
2	26P	D4	C16	D16	-	N16
2	26N	D5	C17	D17	-	M16
2	27P	D6	C18	D18	D7	M14
2	27N	D8	C19	D19	D9	M15
-	-	VCC	-	-	-	VCC
2	28P	D10	C20	D20	D11	L13
2	28N	D12	C21	D21	D13	L12
2	29P	D14	C22	D22	D15	L15
2	29N	D16	C23	D23	D17	L16
-	-	GND	-	-	-	GND
2	30P	D18	C24	D24	D19	L14
-	-	VCCO2	-	-	-	VCCO2
2	30N	D20	C25	D25	-	K15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	31P	D21	C26	D26	-	K14
2	31N	D22	C27	D27	D23	K12
2	32P	D24	C28	D28	D25	K13
2	32N	D26	C29	D29	D27	J13
2	33P	D28	C30	D30	D29	J14
2	33N	D30	C31	D31	D31	J12
-	-	TOE	-	-	-	J15
-	-	RESET	-	-	-	J11
-	-	GOE0	-	-	-	H11
-	-	GOE1	-	-	-	H13
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3N	GCLK2	-	-	-	H15
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3P	GCLK3	-	-	-	H16

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10 ¹	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V _{CCO3}	—	—	—	—	V _{CCO3}	V _{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V _{CCO3}	—	—	—	176	V _{CCO3}	V _{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V _{CCO0}	—	—	—	189	V _{CCO0}	V _{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V _{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	-	AA6
1	18N	C12	-	-	C13	-	AA7
1	19P	C10	-	-	C11	-	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	46N	G6	H19	-	G7	—	AB19
2	47P	G8	H20	-	G9	—	AA19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	47N	G10	H21	-	G11	—	U17
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	48P	G12	H22	-	G13	—	V18
2	48N	G14	H23	-	G15	—	AB21
2	49P	G16	H24	-	G17	—	U18
2	49N	G18	H25	-	G19	—	T17
2	50P	G20	H26	-	G21	R16	AB20
2	50N	G22	H27	-	G23	P16	AA20
2	51P	G24	H28	-	G25	N15	Y19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	51N	G26	H29	-	G27	N14	V19
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	52P	G28	F16	H16	G29	N16	T18
2	52N	G30	F17	H17	G31	M16	R17
2	53P	H0	F18	H18	H1	M14	U19
2	53N	H2	F19	H19	H3	M15	T19
2	54P	H4	H30	E24	H5	—	V20
-	-	VCC	-	-	-	VCC	VCC
2	54N	H6	H31	E26	H7	—	U20
2	55P	H8	F20	H20	H9	L13	W20
2	55N	H10	F21	H21	H11	L12	Y21
2	56P	H12	F22	H22	H13	L15	R18
2	56N	H14	F23	H23	H15	L16	R19
-	-	GND	-	-	-	GND	GND
2	57P	H16	F24	H24	H17	L14	W21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	57N	H18	F25	H25	H19	K15	Y22
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	58P	H20	F26	H26	H21	K14	R20
2	58N	H22	F27	H27	H23	K12	P20
2	59P	H24	F28	H28	H25	K13	T21
2	59N	H26	F29	H29	H27	J13	R21
2	60P	H28	F30	H30	H29	J14	U21
2	60N	H30	F31	H31	H31	J12	V21
-	-	TOE	-	-	-	J15	W22
-	-	RESET	-	-	-	J11	V22
-	-	GOE0	-	-	-	H11	T22
-	-	GOE1	-	-	-	H13	R22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	93N	O0	P31	N31	O1	A13	E17
3	93P	O2	P30	N30	O3	B13	D17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	94N	O4	N11	M21	O5	D11	B18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	94P	O6	N10	M20	O7	B12	A18
-	-	GND	-	-	-	GND	GND
3	95N	O8	N9	M18	O9	C12	C17
-	-	VCC	-	-	-	VCC	VCC
3	95P	O10	N8	M16	O11	E11	B17
3	96N	O12	N7	M12	O13	—	C16
3	96P	O14	N6	M10	O15	—	B16
3	97N	O16	N5	M8	O17	—	F13
3	97P	O18	N4	M6	O19	—	F15
3	98N	O20	N3	M5	O21	—	D16
3	98P	O22	N2	M4	O23	E10	E16
3	99N	O24	N1	M2	O25	A12	A16
3	99P	O26	N0	M0	O27	A11	A15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	100N	O28	P15	N15	O29	B11	B15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	100P	O30	P14	N14	O31	C11	A14
3	101N	P0	P13	N13	P1	B10	D15
3	101P	P2	P12	N12	P3	A10	E15
3	102N	P4	P11	N11	P5	C10	D14
3	102P	P6	P10	N10	P7	D10	F14
3	103N	P8	P9	N9	P9	C9	A13
3	103P	P10	P8	N8	P11	E9	B13
3	104N	P12/VREF3	P29	N29	P13	D9	C14
3	104P	P14	P28	N28	P15	F9	E14
3	105N	P16	P7	N7	P17	A9	E13
3	105P	P18	P6	N6	P19	F8	F12
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	P20	P5	N5	P21	E8	D13
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	P22	P4	N4	P23	A8	C13
3	107N	P24	P3	N3	P25	B9	E12
-	-	GND	-	-	-	GND	GND
3	107P	P26	P2	N2	P27	D8	C12
-	-	VCC	-	-	-	VCC	VCC
3	108N	P28	P1	N1	P29	B8	B12
3	108P	P30	P0	N0	P31	C8	A12
0	109N	Q30	Q31	S31	Q31	B7	E11

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18