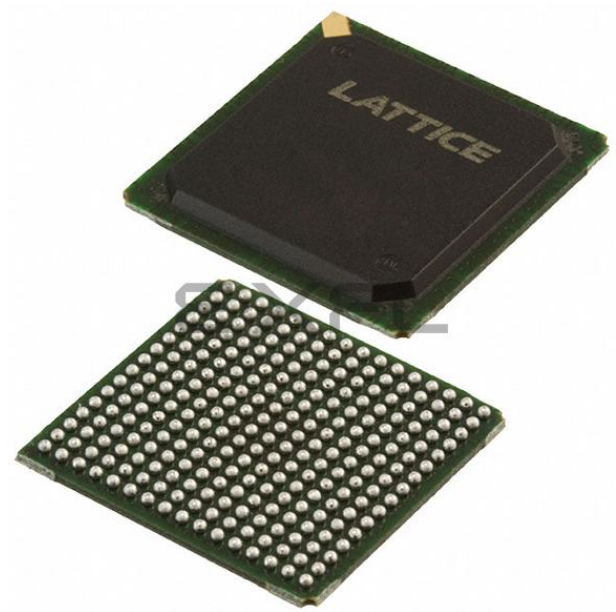
Lattice Semiconductor Corporation - LC5256MV-75F256C Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	256
Number of Gates	-
Number of I/O	141
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5256mv-75f256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

ispXPLD™ 5000MX Family

3.3V, 2.5V and 1.8V In-System Programmable
eXpanded Programmable Logic Device XPLD™ Family

February 2010 **Data Sheet**

Features

- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
  - LVTTL
- **Expanded In-System Programmability (ispXP™)**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
  - Design security
- **High Speed Operation**
  - 4.0ns pin-to-pin delays, 300MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Typical static power: 20 to 50mA (1.8V), 30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - IEEE 1149.1 interface for boundary scan testing
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging
  - Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	3.7ns
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	250MHz
Functional Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor style interface (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more information on the sysCONFIG capability, refer to TN1026, ispXP Configuration Usage Guidelines.

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For information on estimating power consumption, refer to TN1031 Power Estimation in ispXPLD 5000MX Devices.

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

ispXPLD 5000MX Family External Switching Characteristics [1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Output Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX} [4]	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
f_{MAX} (Ext.)	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
f_{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
f_{MAX} (CAMC)[5]	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
f_{MAX} (CAM)[5]	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CAMWMSKS}$	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t_{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t_{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	Output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 250	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 150	ps
$T_{JIT(PERIOD)}$[2]	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 300	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 150	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	600	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		—	1.8	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay (t_{PLL_DELAY})		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specification.
2. Accumulated jitter measured over 10,000 waveform samples.
3. Internal timing for reference only.

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

ispXPLD 5000MX Power Supply and NC Connections[1]

Signals	208 PQFP[4]	256 fpBGA[3, 5]	484 fpBGA, 5[3]	672 fpBGA[3, 5]
VCC	10, 49, 76, 114, 153, 180	D4, D13, F6, F11, L6, L11, N4, N13	A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4	AA21, AA6, F21, F6, G20, G7, J13, J14, K13, K14, L13, L14, M13, M14, N10, N11, N12, N15, N16, N17, N18, N9, P10, P11, P12, P15, P16, P17, P18, P9, R13, R14, T13, T14, U13, U14, V13, V14, Y20, Y7
VCCO0	5, 17, 189, 204	A1, F7, G6	B9, C3, G8, G9, H7, J2, J7, P4	H10, H11, H8, H9, J8, J9, K8, L8, M8, N8
VCCO1	42, 57, 72	K6, L7, T1	AA9, R7, T3, T8, Y3	P8, R8, T8, U8, V8, V9, W10, W11, W8, W9
VCCO2	85, 100, 107, 121	K11, L10, T16	AA14, R16, T15, T20, Y20	P19, R19, T19, U19, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19
VCCO3	146, 161, 176	A16, F10, G11	B14, C20, G14, G15, H16, J16, J21, P19	H12, H13, H14, H15, H16, H17, H18, H19, J18, J19, K19, L19, M19, N19
VCCP	136	J16	M22	N25
VCCJ	27	J1	M1	N4
GND	15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174	K1, C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3	N1, A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8	A11, A16, A2, A25, AE1, AE2, AE25, AE26, AF11, AF16, AF2, AF25, B1, B2, B25, B26, J10, J11, J12, J15, J16, J17, K10, K11, K12, K15, K16, K17, K18, K9, L1, L10, L11, L12, L15, L16, L17, L18, L26, L9, M10, M11, M12, M15, M16, M17, M18, M9, N13, N14, P13, P14, R10, R11, R12, R15, R16, R17, R18, R9, T1, T10, T11, T12, T15, T16, T17, T18, T26, T9, U10, U11, U12, U15, U16, U17, U18, U9, V10, V11, V12, V15, V16, V17
GNDP	134	K16	N22	P26
NC[2]	—	**5256MX**: A2, A11, A12, A15, B2, B12, B15, B16, C4, C12, C15, C16, D1, D11, D14, D15, D16, E1, E4, E10, E11, E13, E14, F4, F5, F12, F13, L1, L4, M3, M7, M13, N2, N6, P1, P2, P5, P6, P13, P14, P15, P16, R1, R2, R4, R5, R6, R16, T2, T3, T4, T5, T6 **5512MX/5768MX**: L1	**5512MX**: P1, AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6 **5768MX/51024MX**: None	A12, A13, A14, A15, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA7, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AD11, AD12, AD13, AD14, AD15, AD16, AE11, AE12, AE13, AE14, AE15, AE16, AF12, AF13, AF14, AF15, B11, B12, B13, B14, B15, B16, C11, C12, C13, C14, C15, C16, C3, D10, D11, D12, D13, D14, D15, D16, D17, E10, E11, E12, E13, E14, E15, E16, E17, E6, E7, E8, F10, F11, F12, F13, F14, F15, F16, F17, G10, G11, G12, G13, G14, G15, G16, G17, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOX} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. Pin orientation follows the conventional counter-clockwise order from pin 1 marking of the topside view.
5. Internal GNDs and I/O GNDs (Bank 0 - Bank 3)þare connected inside package. V_{CCO} balls connect to four power planes within the package, one each for V_{CCOX}.

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	GCLK0N	GCLK1	—	—	—	28	J2	P7
—	—	GND	—	—	—	29	GND	GND
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	V_{CCO1}
1	3N	A14/DATA7	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	—	—	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	—	P1[1]	V3
1	7P	A28	—	—	A29	—	M3	Y2
1	7N	A30	—	—	A31	—	L4	W3
1	8P	B0	A0	—	B1	—	N2	U5
1	8N	B2	A2	—	B3	—	P2	T5
—	—	GND (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	—	R1	U4
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	9N	B5	A6	—	—	—	R2	V4
1	10P	B6	A8	—	B7	—	T2	AA3
1	10N	B8	A10	—	B9	—	T3	AB3
1	—	B10	A12	—	B11	—	—	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	—	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7[1]	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	V_{CCO2}
2	29N	E10	F5	H5	E11	86	M10	U12
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	GND (Bank 2)
2	30P	E12	F6	H6	E13	88	M11	AB13
2	30N	E16	F7	H7	E17	89	T13	Y13
2	31P	E18	—	—	E19	90	P11	V13
2	31N	E20/V_{REF2}	—	—	E21	91	T14	W13
2	32P	E22	F8	H8	E23	92	R12	V14
2	32N	E24	F9	H9	E25	93	R13	W14
2	33P	E26	F10	H10	E27	94	N11	Y14
2	33N	E28	F11	H11	E29	95	T15	AB14
2	34P	F0	F12	H12	F1	96	R14	AB15
2	34N	F2	F13	H13	F3	97	N12	AA15
2	35P	F4	F14	H14	F5	98	P12	U13
—	—	V_{CCO2}	—	—	—	—	V_{CCO2}	V_{CCO2}
2	35N	F6	F15	H15	F7	99	R15	U14
—	—	GND (Bank 2)	—	—	—	—	GND (Bank 2)	GND (Bank 2)
2	36P	F8	E0	—	F9	—	—	W15
2	36N	F10	E2	—	F11	—	—	W16
2	37P	F12	E4	—	F13	—	—	Y16
2	37N	F16	E6	—	F17	—	—	AA16
2	38P	F18	E8	—	F19	—	—	AB16
2	38N	F20	E10	—	F21	—	—	AA17
2	39P	F22	E12	—	F23	—	—	Y17
2	39N	F24	E16	—	F25	—	—	AA18
2	40P	F26	E20	—	F27	—	—	W17
2	40N	F28	E22	—	F29	—	—	W18
2	41P	G0	—	—	G1	—	—	V15
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	V_{CCO2}
2	41N	G2	—	—	G3	—	—	U15
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	GND (Bank 2)
2	42P	G4	—	—	G5	102	P13	Y18
2	42N	G6	—	—	G7	103	P15	V17
2	43P	G8	—	—	G9	—	M13	V16
2	43N	G10	—	—	G11	—	P14	U16
2	44P	G12	—	—	G13	—	—	AB18
2	44N	G14	—	—	G15	—	—	AB19
2	45P	G16	—	—	G17	—	—	U18
2	45N	G18	—	—	G19	—	—	T17
2	46P	G20	—	—	G21	104	R16	AB20
2	46N	G22	—	—	G23	105	P16	AA20
2	47P	G24	—	—	G25	106	N15	Y19
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	V_{CCO2}

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	B4
0	127P	S20	S10	T16	S21	E4	A4
0	128N	S18	Q17	S17	S19	B1	B3
0	128P	S16	Q16	S16	S17	C1	A3
0	129N	S14	Q15	S15	S15	D3	F5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	129P	S12	Q14	S14	S13	C2	G6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	130N	S10	Q13	S13	S11	E3	H6
0	130P	S8	Q12	S12	S9	D2	G5
0	131N	S6	S9	T14	S7	—	D3
0	131P	S4	S8	T12	S5	—	D2
0	132N	S2	S7	T10	S3	—	E4
-	-	VCC	-	-	-	VCC	VCC
0	132P	S0	S6	T8	S1	—	E3
-	-	GND	-	-	-	GND	GND
0	133N	T30	S5	T6	T31	—	F4
0	133P	T28	S4	T4	T29	—	G4
0	134N	T26	S3	T2	T27	—	C2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	134P	T24	S2	T0	T25	—	C1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	135N	T22	S1	-	T23	D1	F3
0	135P	T20	S0	-	T21	E1	G3
0	136N	T18	S31	-	T19	F4	H4
-	-	VCC	-	-	-	VCC	VCC
0	136P	T16	S30	-	T17	F5	J4
0	137N	T14	Q11	S11	T15	E2	H5
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	J5
0	138N	T10	Q9	S9	T11	F1	E2
0	138P	T8	Q8	S8	T9	G1	F2
-	-	GND	-	-	-	GND	GND
0	139N	T6	Q7	S7	T7	F3	D1
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	139P	T4	Q6	S6	T5	G5	E1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	140N	T2	Q5	S5	T3	H5	J3
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	H2
0	141N	U30	U31	W31	U31	G3	G2
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	G1
0	142N	U26	U29	W29	U27	—	J6
0	142P	U24	U28	W28	U25	—	K4

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	—	AA6
1	18N	C12	-	-	C13	—	AA7
1	19P	C10	-	-	C11	—	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	93N	O0	P31	N31	O1	A13	E17
3	93P	O2	P30	N30	O3	B13	D17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	94N	O4	N11	M21	O5	D11	B18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	94P	O6	N10	M20	O7	B12	A18
-	-	GND	-	-	-	GND	GND
3	95N	O8	N9	M18	O9	C12	C17
-	-	VCC	-	-	-	VCC	VCC
3	95P	O10	N8	M16	O11	E11	B17
3	96N	O12	N7	M12	O13	—	C16
3	96P	O14	N6	M10	O15	—	B16
3	97N	O16	N5	M8	O17	—	F13
3	97P	O18	N4	M6	O19	—	F15
3	98N	O20	N3	M5	O21	—	D16
3	98P	O22	N2	M4	O23	E10	E16
3	99N	O24	N1	M2	O25	A12	A16
3	99P	O26	N0	M0	O27	A11	A15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	100N	O28	P15	N15	O29	B11	B15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	100P	O30	P14	N14	O31	C11	A14
3	101N	P0	P13	N13	P1	B10	D15
3	101P	P2	P12	N12	P3	A10	E15
3	102N	P4	P11	N11	P5	C10	D14
3	102P	P6	P10	N10	P7	D10	F14
3	103N	P8	P9	N9	P9	C9	A13
3	103P	P10	P8	N8	P11	E9	B13
3	104N	P12/VREF3	P29	N29	P13	D9	C14
3	104P	P14	P28	N28	P15	F9	E14
3	105N	P16	P7	N7	P17	A9	E13
3	105P	P18	P6	N6	P19	F8	F12
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	P20	P5	N5	P21	E8	D13
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	P22	P4	N4	P23	A8	C13
3	107N	P24	P3	N3	P25	B9	E12
-	-	GND	-	-	-	GND	GND
3	107P	P26	P2	N2	P27	D8	C12
-	-	VCC	-	-	-	VCC	VCC
3	108N	P28	P1	N1	P29	B8	B12
3	108P	P30	P0	N0	P31	C8	A12
0	109N	Q30	Q31	S31	Q31	B7	E11

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	79N	N10	P5	N5	N11	—	V26
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	80P	N12	P6	N6	N13	—	V22
2	80N	N14	P7	N7	N15	—	V23
2	81P	N16	P8	N8	N17	—	V24
2	81N	N18	P9	N9	N19	—	V25
2	82P	N20	P10	N10	N21	—	U20
2	82N	N22	P11	N11	N23	—	T20
2	83P	N24	P12	N12	N25	—	U26
2	83N	N26	P13	N13	N27	—	U25
2	84P	N28	P14	N14	N29	—	U21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	84N	N30	P15	N15	N31	—	T21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	85P	P0	P16	N16	P1	—	U22
2	85N	P2	P17	N17	P3	—	U23
2	86P	P4	P18	N18	P5	—	U24
2	86N	P6	P19	N19	P7	—	T24
2	87P	P8	P20	N20	P9	—	T23
2	87N	P10	P21	N21	P11	—	T22
2	88P	P12	P22	N22	P13	—	T25
-	-	VCC	-	-	-	VCC	VCC
2	88N	P14	P23	N23	P15	—	R26
-	-	GND	-	-	-	GND	GND
2	89P	P16	P24	N24	P17	—	R25
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	89N	P18	P25	N25	P19	—	R24
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	90P	P20	P26	N26	P21	—	R21
2	90N	P22	P27	N27	P23	—	P21
2	91P	P24	P28	N28	P25	—	R22
2	91N	P26	P29	N29	P27	—	R23
2	92P	P28	P30	N30	P29	—	R20
2	92N	P30	P31	N31	P31	—	P20
-	-	TOE	-	-	-	W22	P25
-	-	RESET	-	-	-	V22	P24
-	-	GOE0	-	-	-	T22	P23
-	-	GOE1	-	-	-	R22	P22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3N	GCLK2	-	-	-	P16	N26
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3P	GCLK3	-	-	-	N16	N24
3	93N	R0	T31	R31	R1	J22	N23
3	93P	R2	T30	R30	R3	H22	N22
3	94N	R4	T29	R29	R5	N19	M26
3	94P	R6	T28	R28	R7	P15	M25
3	95N	R8	T27	R27	R9	P21	M23
3	95P	R10	T26	R26	R11	N15	M22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	96N	R12	T25	R25	R13	M15	N20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	96P	R14	T24	R24	R15	N20	M20
-	-	GND	-	-	-	GND	GND
3	97N	R16	T23	R23	R17	P22	N21
3	97P	R18	T22	R22	R19	N21	M21
3	98N	R20	T21	R21	R21	N17	M24
3	98P	R22	T20	R20	R23	M20	L24
3	99N	R24	T19	R19	R25	P17	L23
-	-	VCC	-	-	-	VCC	VCC
3	99P	R26	T18	R18	R27	P18	L22
3	100N	R28	T17	R17	R29	M21	L25
3	100P	R30	T16	R16	R31	M17	K26
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	101N	T0	T15	R15	T1	L20	K25
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	101P	T2	T14	R14	T3	N18	K24
3	102N	T4	T13	R13	T5	L21	K23
3	102P	T6	T12	R12	T7	M18	K22
3	103N	T8	T11	R11	T9	L22	J25
3	103P	T10	T10	R10	T11	L17	J24
3	104N	T12	T9	R9	T13	K22	L21
3	104P	T14	T8	R8	T15	L18	K21
3	105N	T16	T7	R7	T17	K21	L20
3	105P	T18	T6	R6	T19	K18	K20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	T20	T5	R5	T21	K20	J23
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	T22	T4	R4	T23	K17	J22
3	107N	T24	T3	R3	T25	K19	J26
3	107P	T26	T2	R2	T27	J17	H26
3	108N	T28	T1	R1	T29	E22	H25
3	108P	T30/PLL_FBK1	T0	R0	T31	E21	H24
3	109N	U0/PLL_RST1	X27	V27	U1	G22	H23
3	109P	U2	X26	V26	U3	F21	H22

ispXPLD 5000MB (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4FN256C	256	2.5	4.0	Lead-free fpBGA	256	141	C
	LC5256MB-5FN256C	256	2.5	5.0	Lead-free fpBGA	256	141	C
	LC5256MB-75FN256C	256	2.5	7.5	Lead-free fpBGA	256	141	C
LC5512MB	LC5512MB-45QN208C	512	2.5	4.5	Lead-free PQFP	208	149	C
	LC5512MB-75QN208C	512	2.5	7.5	Lead-free PQFP	208	149	C
	LC5512MB-45FN256C	512	2.5	4.5	Lead-free fpBGA	256	193	C
	LC5512MB-75FN256C	512	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5512MB-45FN484C	512	2.5	4.5	Lead-free fpBGA	484	253	C
	LC5512MB-75FN484C	512	2.5	7.5	Lead-free fpBGA	484	253	C
LC5768MB	LC5768MB-5FN256C	768	2.5	5.0	Lead-free fpBGA	256	193	C
	LC5768MB-75FN256C	768	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5768MB-5FN484C	768	2.5	5.0	Lead-free fpBGA	484	317	C
	LC5768MB-75FN484C	768	2.5	7.5	Lead-free fpBGA	484	317	C
LC51024MB	LC51024MB-52FN484C	1024	2.5	5.2	Lead-free fpBGA	484	317	C
	LC51024MB-75FN484C	1024	2.5	7.5	Lead-free fpBGA	484	317	C
	LC51024MB-52FN672C	1024	2.5	5.2	Lead-free fpBGA	672	381	C
	LC51024MB-75FN672C	1024	2.5	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5FN256I	256	2.5	5.0	Lead-free fpBGA	256	141	I
	LC5256MB-75FN256I	256	2.5	7.5	Lead-free fpBGA	256	141	I
LC5512MB	LC5512MB-75QN208I	512	2.5	7.5	Lead-free PQFP	208	149	I
	LC5512MB-75FN256I	512	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5512MB-75FN484I	512	2.5	7.5	Lead-free fpBGA	484	253	I
LC5768MB	LC5768MB-75FN256I	768	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5768MB-75FN484I	768	2.5	7.5	Lead-free fpBGA	484	317	I
LC51024MB	LC51024MB-75FN484I	1024	2.5	7.5	Lead-free fpBGA	484	317	I
	LC51024MB-75FN672I	1024	2.5	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4FN256C	256	3.3	4.0	Lead-free fpBGA	256	141	C
	LC5256MV-5FN256C	256	3.3	5.0	Lead-free fpBGA	256	141	C
	LC5256MV-75FN256C	256	3.3	7.5	Lead-free fpBGA	256	141	C

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5512MV	LC5512MV-45QN208C	512	3.3	4.5	Lead-free PQFP	208	149	C
	LC5512MV-75QN208C	512	3.3	7.5	Lead-free PQFP	208	149	C
	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	193	C
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	253	C
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	253	C
LC5768MV	LC5768MV-5FN256C	768	3.3	5.0	Lead-free fpBGA	256	193	C
	LC5768MV-75FN256C	768	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5768MV-5FN484C	768	3.3	5.0	Lead-free fpBGA	484	317	C
	LC5768MV-75FN484C	768	3.3	7.5	Lead-free fpBGA	484	317	C
LC51024MV	LC51024MV-52FN484C	1024	3.3	5.2	Lead-free fpBGA	484	317	C
	LC51024MV-75FN484C	1024	3.3	7.5	Lead-free fpBGA	484	317	C
	LC51024MV-52FN672C	1024	3.3	5.2	Lead-free fpBGA	672	381	C
	LC51024MV-75FN672C	1024	3.3	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5FN256I	256	3.3	5.0	Lead-free fpBGA	256	141	I
	LC5256MV-75FN256I	256	3.3	7.5	Lead-free fpBGA	256	141	I
LC5512MV	LC5512MV-75QN208I	512	3.3	7.5	Lead-free PQFP	208	149	I
	LC5512MV-75FN256I	512	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5512MV-75FN484I	512	3.3	7.5	Lead-free fpBGA	484	253	I
LC5768MV	LC5768MV-75FN256I	768	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5768MV-75FN484I	768	3.3	7.5	Lead-free fpBGA	484	317	I
LC51024MV	LC51024MV-75FN484I	1024	3.3	7.5	Lead-free fpBGA	484	317	I
	LC51024MV-75FN672I	1024	3.3	7.5	Lead-free fpBGA	672	381	I

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- TN1000 – sysIO Usage Guidelines for Lattice Devices
- TN1003 – sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices
- TN1031 – Power Estimation in ispXPLD 5000MX Devices
- TN1030 – Using Memory in ispXPLD 5000MX Devices
- TN1026 – ispXP Configuration Usage Guidelines

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
December 2003	07	Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers).
		Updated ispXPLD 5000MX timing numbers (version v.1.7).
		Added lead-free package designator.
		Removed ispXPLD 5000MC industrial temperature grade ordering part numbers.
January 2004	08	Lead-free package release for the ispXPLD 5000MC and 5000MV devices.
		Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers).
March 2004	08.1	Updated the MFB Cascade Chain table for the ispXPLD 5256MX device.
May 2004	09	Updated the ispXPLD 5000MX timig numbers (version v.1.8) ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release
		Updated typical supply current data and condition.
		ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14.
August 2004	10	Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ.
		Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free).
October 2004	10.1	Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer)
November 2004	11	Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers.
December 2004	11.1	Pin name RESETB has been updated to RESET.
March 2005	12	208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices.
April 2005	12.1	Page 23, clarification of footnote regarding IDK specification.
March 2006	12.2	Signal description for RESET has been updated.
April 2009	12.3	Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format.
February 2010	12.4	References to "system gates" changed to "functional gates."