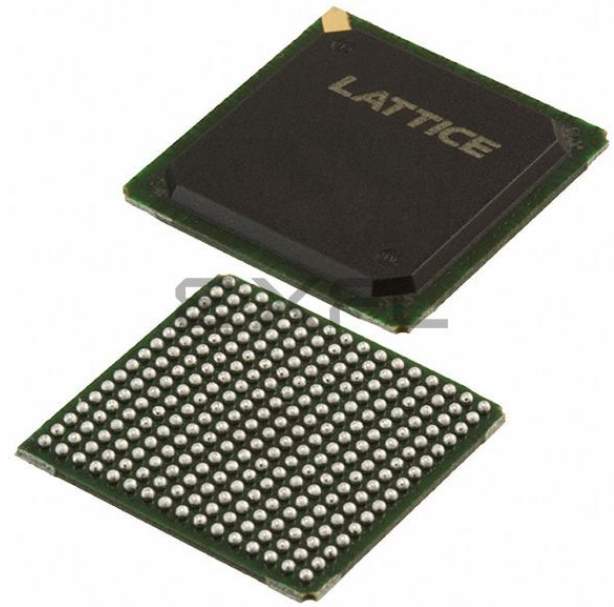
# Lattice Semiconductor Corporation - LC5256MV-75FN256C Datasheet

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

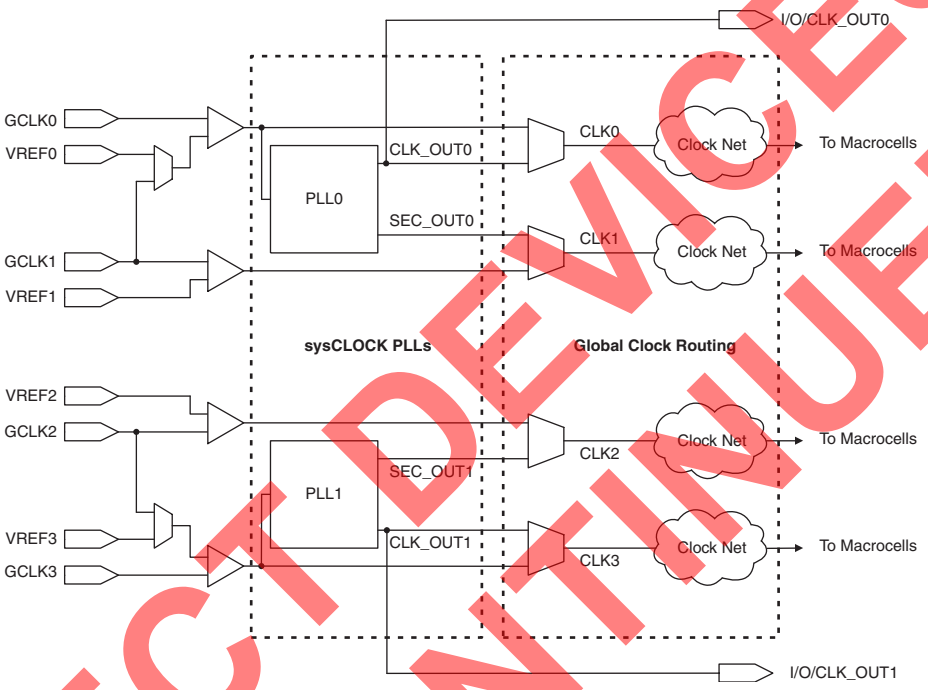
| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 141 |
| Operating Temperature | 0°C ~ 90°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5256mv-75fn256c |

| Product Line | Ordering Part Number | Product Status | Reference PCN |
|---|---|---|---|
| **LC5512MV** | LC5512MV-45Q208C | Active / Orderable | |
| | LC5512MV-45QN208C | | |
| | LC5512MV-75Q208C | | |
| | LC5512MV-75QN208C | | |
| | LC5512MV-75Q208I | | |
| | LC5512MV-75QN208I | | |
| | LC5512MV-45F256C | | |
| | LC5512MV-45FN256C | | |
| | LC5512MV-75F256C | | |
| | LC5512MV-75FN256C | | |
| | LC5512MV-75F256I | | |
| | LC5512MV-75FN256I | | |
| | LC5512MV-45F484C | | |
| | LC5512MV-45FN484C | | |
| | LC5512MV-75F484C | | |
| | LC5512MV-75FN484C | | |
| | LC5512MV-75F484I | | |
| | LC5512MV-75FN484I | | |
| **LC5512MB** | LC5512MB-45Q208C | **Discontinued** | PCN#09-10 |
| | LC5512MB-45QN208C | | |
| | LC5512MB-75Q208C | | |
| | LC5512MB-75QN208C | | |
| | LC5512MB-75Q208I | | |
| | LC5512MB-75QN208I | | |
| | LC5512MB-45F256C | Active / Orderable | |
| | LC5512MB-45FN256C | | |
| | LC5512MB-75F256C | | |
| | LC5512MB-75FN256C | | |
| | LC5512MB-75F256I | | |
| | LC5512MB-75FN256I | | |
| | LC5512MB-45F484C | **Discontinued** | PCN#09-10 |
| | LC5512MB-45FN484C | | |
| | LC5512MB-75F484C | | |
| | LC5512MB-75FN484C | | |
| | LC5512MB-75F484I | | |
| | LC5512MB-75FN484I | | |
| **LC5512MC** | LC5512MC-45Q208C | **Discontinued** | PCN#09-10 |
| | LC5512MC-45QN208C | | |
| | LC5512MC-75Q208C | | |
| | LC5512MC-75QN208C | | |
| | LC5512MC-75Q208I | | |
| | LC5512MC-75QN208I | | |
| | LC5512MC-45F256C | | |
| | LC5512MC-45FN256C | | |
| | LC5512MC-75F256C | | |
| | LC5512MC-75FN256C | | |
| | LC5512MC-75F256I | | |
| | LC5512MC-75FN256I | | |

## Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

***Figure 14. Clock Distribution Network***




## sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

*Figure 15. PLL Block Diagram*

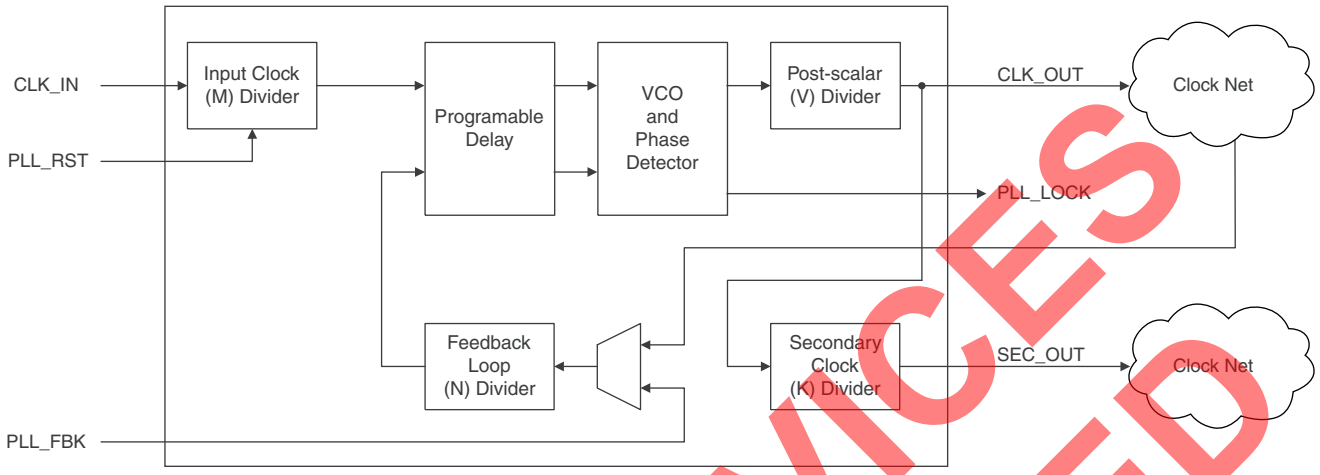
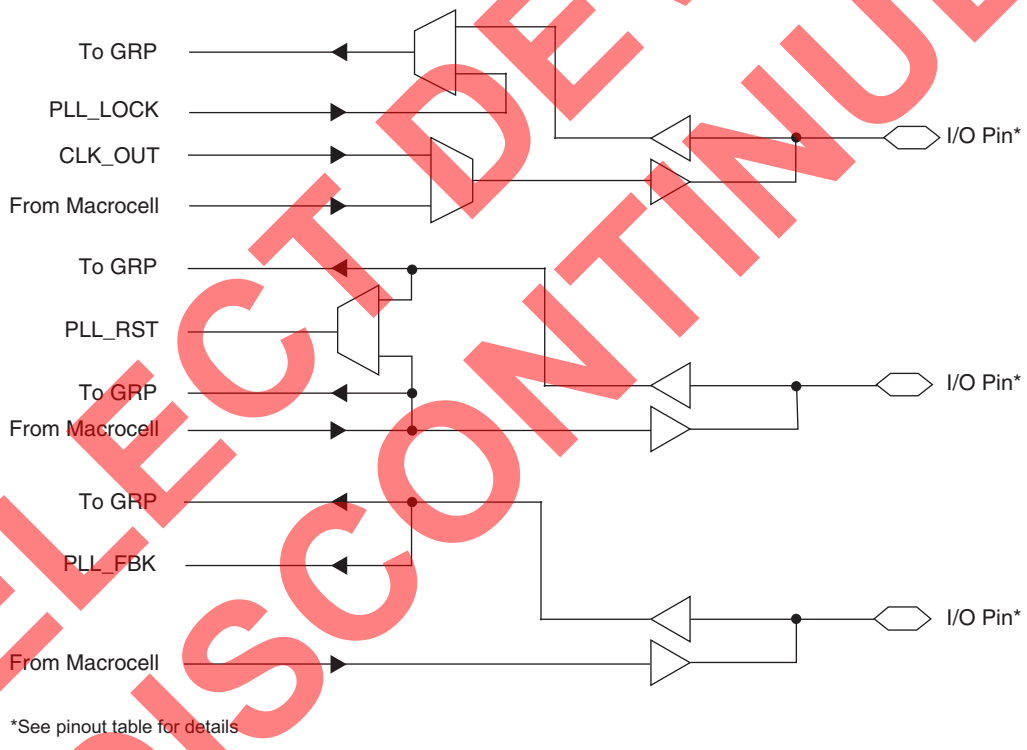



*Figure 16. Connection of Optional PLL Inputs and Outputs*






In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

# ispXPLD 5000MX Family Internal Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description | Base Parameter | -4 | | -45 | | -5 | | -52 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | | | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | — | 0.70 | — | 0.91 | — | 0.96 | — | 1.11 | — | 1.30 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | — | 0.40 | — | 0.35 | — | 0.35 | — | 0.35 | — | 0.55 | ns |
| $t_{RST}$ | Global RESET Pin Delay | — | — | 3.77 | — | 4.24 | — | 4.71 | — | 4.71 | — | 7.07 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | — | 1.98 | — | 2.66 | — | 2.34 | — | 2.87 | — | 3.27 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | — | 1.16 | — | 1.30 | — | 1.45 | — | 1.60 | — | 2.17 | ns |
| $t_{EN}$ | Output Enable Time | — | — | 2.52 | — | 2.84 | — | 3.16 | — | 3.63 | — | 4.23 | ns |
| $t_{DIS}$ | Output Disable Time | — | — | 1.92 | — | 2.40 | — | 2.40 | — | 2.40 | — | 3.60 | ns |
| **Routing Delays** | | | | | | | | | | | | | |
| $t_{ROUTE}$ | Delay through SRP | — | — | 1.95 | — | 2.06 | — | 2.34 | — | 2.24 | — | 3.66 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | — | 0.60 | — | 0.60 | — | 0.60 | — | 0.47 | — | 1.63 | ns |
| $t_{PTSA}$ | Product Term Sharing Array Delay | — | — | 0.50 | — | 0.50 | — | 0.53 | — | 0.83 | — | 1.34 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | — | 0.19 | — | 0.02 | — | 0.39 | — | 0.03 | — | 0.60 | ns |
| $t_{GCLK}$ | Global Clock Tree Delay | — | — | 0.52 | — | 0.32 | — | 0.72 | — | 0.82 | — | 0.78 | ns |
| $t_{BCLK}$ | Block PT Clock Delay | — | — | 0.12 | — | 0.14 | — | 0.15 | — | 0.15 | — | 0.23 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | — | — | 0.12 | — | 0.14 | — | 0.15 | — | 0.15 | — | 0.23 | ns |
| $t_{PLL\_DELAY}$ | Programmable PLL Delay Increment | — | — | 0.30 | — | 0.30 | — | 0.30 | — | 0.30 | — | 0.30 | ns |
| $t_{BSR}$ | Block PT Reset Delay | — | — | 0.72 | — | 0.81 | — | 0.90 | — | 0.94 | — | 1.35 | ns |
| $t_{PTSR}$ | Macrocell PT Set/ Reset Delay | — | — | 0.60 | — | 0.75 | — | 0.75 | — | 0.75 | — | 1.13 | ns |
| $t_{LPTOE}$ | Macrocell PT OE Delay | — | — | 0.83 | — | 1.19 | — | 1.04 | — | 1.52 | — | 1.31 | ns |
| $t_{SPTOE}$ | Segment PT OE Delay | — | — | 0.83 | — | 1.19 | — | 1.04 | — | 1.52 | — | 1.31 | ns |
| $t_{OSA}$ | Output Sharing Array Delay | — | — | 0.80 | — | 0.90 | — | 1.00 | — | 1.00 | — | 1.50 | ns |
| $t_{PTOE}$ | Global PT OE Delay | — | — | 0.83 | — | 1.04 | — | 1.04 | — | 1.04 | — | 1.56 | ns |
| $t_{PDB}$ | 5-PT Bypass Propagation Delay | — | — | 0.20 | — | 0.23 | — | 0.25 | — | 0.25 | — | 0.38 | ns |
| $t_{PDI}$ | Macrocell Propagation Delay | — | — | 0.50 | — | 0.93 | — | 0.72 | — | 0.72 | — | 1.04 | ns |

# ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Base Parameter | -4 | | -45 | | -5 | | -52 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PDPRWH}$ | R/W Hold time after Clock Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |
| $t_{PDPDATAS}$ | Data Setup before Clock Time | — | -0.27 | — | -0.27 | — | -0.22 | — | -0.22 | — | -0.21 | — | ns |
| $t_{PDPDATAH}$ | Data Hold time after Clock Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |
| $t_{PDPRCLKO}$ | Read Clock to Output Delay | — | — | 5.08 | — | 5.02 | — | 5.66 | — | 5.45 | — | 8.54 | ns |
| $t_{PDPCLKSKEW}$ | Opposite Clock Cycle Delay | — | 1.40 | — | 1.40 | — | 1.76 | — | 1.76 | — | 1.83 | — | ns |
| $t_{PDPRSTO}$ | Reset to RAM Output Delay | — | — | 3.30 | — | 3.30 | — | 4.13 | — | 4.13 | — | 4.29 | ns |
| $t_{PDPRSTR}$ | Reset Recovery Time | — | 1.20 | — | 1.20 | — | 1.50 | — | 1.50 | — | 1.56 | — | ns |
| $t_{PDPRSTPW}$ | Reset Pulse Width | — | 0.14 | — | 0.14 | — | 0.18 | — | 0.18 | — | 0.19 | — | ns |
| **Dual Port RAM** | | | | | | | | | | | | | |
| $t_{DPMSAS}$ | Memory Select A Setup Before R/W A Time | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.21 | — | ns |
| $t_{DPMSAH}$ | Memory Select Hold time after R/W A Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |
| $t_{DPCEAS}$ | Clock Enable A Setup before Clock A Time | — | 3.72 | — | 3.72 | — | 3.72 | — | 3.72 | — | 4.84 | — | ns |
| $t_{DPCEAH}$ | Clock Enable A Hold time after Clock A Time | — | -2.95 | — | -2.95 | — | -2.95 | — | -2.95 | — | -2.27 | — | ns |
| $t_{DPADDAS}$ | Address A Setup before Clock A Time | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.21 | — | ns |
| $t_{DPADDAH}$ | Address A Hold time after Clock A Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |
| $t_{DPRWAS}$ | R/W A Setup before Clock A Time | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.21 | — | ns |
| $t_{DPRWAH}$ | R/W A Hold time after Clock A Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |
| $t_{DPDATAAS}$ | Write Data A Setup before Clock A Time | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.21 | — | ns |
| $t_{DPDATAAH}$ | Write Data A Hold time after Clock A Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |
| $t_{DPMSBS}$ | Memory Select B Setup Before R/W B Time | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.27 | — | -0.21 | — | ns |
| $t_{DPMSBH}$ | Memory Select Hold time after R/W B Time | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | -0.01 | — | ns |

## ispXPLD 5000MX Family Timing Adders

| Parameter | Description | Base Param. | -4 | | -45 | | -5 | | -52 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **$t_{IOI}$ Input Adjusters** | | | | | | | | | | | | | |
| LVTTL_in | Using 3.3V TTL | $t_{IOIN}$ | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | ns |
| LVCMOS_18_in | Using 1.8V CMOS | $t_{IOIN}$ | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | ns |
| LVCMOS_25_in | Using 2.5V CMOS | $t_{IOIN}$ | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | ns |
| LVCMOS_33_in | Using 3.3V CMOS | $t_{IOIN}$ | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | ns |
| AGP_1X_in | Using AGP 1x | $t_{IOIN}$ | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | ns |
| CTT25_in | Using CTT 2.5V | $t_{IOIN}$ | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | ns |
| CTT33_in | Using CTT 3.3V | $t_{IOIN}$ | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | ns |
| GTL+_in | Using GTL+ | $t_{IOIN}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| HSTL_I_in | Using HSTL 2.5V, Class I | $t_{IOIN}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| HSTL_III_in | Using HSTL 2.5V, Class III | $t_{IOIN}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| HSTL_IV_in | Using HSTL 2.5V, Class IV | $t_{IOIN}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| LVDS_in | Using Low Voltage Differential Signaling (LVDS) | $t_{IOIN}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| LVPECL_in | Using Low Voltage PECL | $t_{IOIN}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| PCI_in | Using PCI | $t_{IOIN}$ | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | ns |
| SSTL2_I_in | Using SSTL 2.5V, Class I | $t_{IOIN}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| SSTL2_II_in | Using SSTL 2.5V, Class II | $t_{IOIN}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| SSTL3_I_in | Using SSTL 3.3V, Class I | $t_{IOIN}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| SSTL3_II_in | Using SSTL 3.3V, Class II | $t_{IOIN}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| **$t_{IOO}$ Output Adjusters – Output Signal Modifiers** | | | | | | | | | | | | | |
| Slow Slew | Using Slow Slew (LVTTL and LVCMOS Outputs Only) | $t_{IOBUF}$, $t_{IOEN}$ | — | 0.9 | — | 0.9 | — | 0.9 | — | 0.9 | — | 0.9 | ns |
| **$t_{IOO}$ Output Adjusters – Output Configurations** | | | | | | | | | | | | | |
| LVTTL_out | Using 3.3V TTL Drive | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 1.2 | — | 1.2 | — | 1.2 | — | 1.2 | — | 1.2 | ns |
| LVCMOS_18_4mA_out | Using 1.8V CMOS Standard, 4mA Drive | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | ns |
| LVCMOS_18_5.33mA_out | Using 1.8V CMOS Standard, 5.33mA Drive | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | ns |

## ispXPLD 5000MX Family Timing Adders (Continued)

| Parameter | Description | Base Param. | -4 | | -45 | | -5 | | -52 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| HSTL_I_out | Using HSTL 2.5V, Class I | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| HSTL_III_out | Using HSTL 2.5V, Class III | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| HSTL_IV_out | Using HSTL 2.5V, Class IV | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| LVDS_out | Using Low Voltage Differential Signaling (LVDS) | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | ns |
| LVPECL_out | Using Low Voltage PECL | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | ns |
| PCI_out | Using PCI Standard | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| SSTL2_I_out | Using SSTL 2.5V, Class I | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | ns |
| SSTL2_II_out | Using SSTL 2.5V, Class II | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| SSTL3_I_out | Using SSTL 3.3V, Class I | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.2 | — | 0.2 | — | 0.2 | — | 0.2 | — | 0.2 | ns |
| SSTL3_II_out | Using SSTL 3.3V, Class II | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.4 | — | 0.4 | — | 0.4 | — | 0.4 | — | 0.4 | ns |

Timing v.1.8

| Signals | 208 PQFP[4] | 256 fpBGA[3, 5] | 484 fpBGA, 5[3] | 672 fpBGA[3, 5] |
|---|---|---|---|---|
| VCC | 10, 49, 76, 114, 153, 180 | D4, D13, F6, F11, L6, L11, N4, N13 | A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4 | AA21, AA6, F21, F6, G20, G7, J13, J14, K13, K14, L13, L14, M13, M14, N10, N11, N12, N15, N16, N17, N18, N9, P10, P11, P12, P15, P16, P17, P18, P9, R13, R14, T13, T14, U13, U14, V13, V14, Y20, Y7 |
| VCCO0 | 5, 17, 189, 204 | A1, F7, G6 | B9, C3, G8, G9, H7, J2, J7, P4 | H10, H11, H8, H9, J8, J9, K8, L8, M8, N8 |
| VCCO1 | 42, 57, 72 | K6, L7, T1 | AA9, R7, T3, T8, Y3 | P8, R8, T8, U8, V8, V9, W10, W11, W8, W9 |
| VCCO2 | 85, 100, 107, 121 | K11, L10, T16 | AA14, R16, T15, T20, Y20 | P19, R19, T19, U19, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19 |
| VCCO3 | 146, 161, 176 | A16, F10, G11 | B14, C20, G14, G15, H16, J16, J21, P19 | H12, H13, H14, H15, H16, H17, H18, H19, J18, J19, K19, L19, M19, N19 |
| VCCP | 136 | J16 | M22 | N25 |
| VCCJ | 27 | J1 | M1 | N4 |
| GND | 15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174 | K1, C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3 | N1, A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8 | A11, A16, A2, A25, AE1, AE2, AE25, AE26, AF11, AF16, AF2, AF25, B1, B2, B25, B26, J10, J11, J12, J15, J16, J17, K10, K11, K12, K15, K16, K17, K18, K9, L1, L10, L11, L12, L15, L16, L17, L18, L26, L9, M10, M11, M12, M15, M16, M17, M18, M9, N13, N14, P13, P14, R10, R11, R12, R15, R16, R17, R18, R9, T1, T10, T11, T12, T15, T16, T17, T18, T26, T9, U10, U11, U12, U15, U16, U17, U18, U9, V10, V11, V12, V15, V16, V17 |
| GNDP | 134 | K16 | N22 | P26 |
| NC[2] | — | **5256MX**: A2, A11, A12, A15, B2, B12, B15, B16, C4, C12, C15, C16, D1, D11, D14, D15, D16, E1, E4, E10, E11, E13, E14, F4, F5, F12, F13, L1, L4, M3, M7, M13, N2, N6, P1, P2, P5, P6, P13, P14, P15, P16, R1, R2, R4, R5, R6, R16, T2, T3, T4, T5, T6<br>**5512MX/5768MX**: L1 | **5512MX**: P1, AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6<br>**5768MX/51024MX**: None | A12, A13, A14, A15, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA7, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AD11, AD12, AD13, AD14, AD15, AD16, AE11, AE12, AE13, AE14, AE15, AE16, AF12, AF13, AF14, AF15, B11, B12, B13, B14, B15, B16, C11, C12, C13, C14, C15, C16, C3, D10, D11, D12, D13, D14, D15, D16, D17, E10, E11, E12, E13, E14, E15, E16, E17, E6, E7, E8, F10, F11, F12, F13, F14, F15, F16, F17, G10, G11, G12, G13, G14, G15, G16, G17, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17 |

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, $V_{CC}$ or GND.
3. Balls for GND, $V_{CC}$ and $V_{CCOX}$ are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. Pin orientation follows the conventional counter-clockwise order from pin 1 marking of the topside view.
5. Internal GNDs and I/O GNDs (Bank 0 - Bank 3)þare connected inside package. $V_{CCO}$ balls connect to four power planes within the package, one each for $V_{CCOX}$.

## ispXPLD 5256MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 256 fpBGA Ball Number |
|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | |
| 3 | 34N | E30 | - | - | E31 | H14 |
| 3 | 34P | E28 | - | - | E29 | G16 |
| 3 | 35N | E26 | - | - | E27 | G15 |
| 3 | 35P | E24/PLL_FBK1 | - | - | E25 | F15 |
| 3 | 36N | E22/PLL_RST1 | E27 | F27 | E23 | H12 |
| 3 | 36P | E21 | E26 | F26 | - | G14 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) |
| 3 | 37N | E20 | E25 | F25 | - | F16 |
| - | - | VCCO3 | - | - | - | VCCO3 |
| 3 | 37P | E18 | E24 | F24 | E19 | E16 |
| - | - | GND | - | - | - | GND |
| 3 | 38N | E16 | E23 | F23 | E17 | G13 |
| 3 | 38P | E14 | E22 | F22 | E15 | G12 |
| 3 | 39N | E12 | E21 | F21 | E13 | F14 |
| 3 | 39P | E10/CLK_OUT1 | E20 | F20 | E11 | E15 |
| - | - | VCC | - | - | - | VCC |
| 3 | 40N | E8 | E19 | F19 | E9 | D12 |
| 3 | 40P | E6 | E18 | F18 | E7 | B14 |
| 3 | 41N | E5 | E17 | F17 | - | C13 |
| 3 | 41P | E4 | E16 | F16 | - | A14 |
| 3 | 42N | E2 | E31 | F31 | E3 | A13 |
| 3 | 42P | E0 | E30 | F30 | E1 | B13 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) |
| - | - | VCCO3 | - | - | - | VCCO3 |
| 3 | 43N | F30 | E15 | F15 | F31 | B11 |
| 3 | 43P | F28 | E14 | F14 | F29 | C11 |
| 3 | 44N | F26 | E13 | F13 | F27 | B10 |
| 3 | 44P | F24 | E12 | F12 | F25 | A10 |
| 3 | 45N | F22 | E11 | F11 | F23 | C10 |
| 3 | 45P | F21 | E10 | F10 | - | D10 |
| 3 | 46N | F20 | E9 | F9 | - | C9 |
| 3 | 46P | F18 | E8 | F8 | F19 | E9 |
| 3 | 47N | F16/VREF3 | E29 | F29 | F17 | D9 |
| 3 | 47P | F14 | E28 | F28 | F15 | F9 |
| 3 | 48N | F12 | E7 | F7 | F13 | A9 |
| 3 | 48P | F10 | E6 | F6 | F11 | F8 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) |
| 3 | 49N | F8 | E5 | F5 | F9 | E8 |
| - | - | VCCO3 | - | - | - | VCCO3 |
| 3 | 49P | F6 | E4 | F4 | F7 | A8 |
| 3 | 50N | F5 | E3 | F3 | - | B9 |
| 3 | 50P | F4 | E2 | F2 | - | D8 |
| - | - | VCC | - | - | - | VCC |

## ispXPLD 5256MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 256 fpBGA Ball Number |
|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | |
| 3 | 51N | F2 | E1 | F1 | F3 | B8 |
| 3 | 51P | F0 | E0 | F0 | F1 | C8 |
| 0 | 52N | G30 | G31 | H31 | G31 | B7 |
| 0 | 52P | G28 | G30 | H30 | G29 | A7 |
| - | - | GND | - | - | - | NC |
| 0 | 53N | G26 | G29 | H29 | G27 | D7 |
| 0 | 53P | G24 | G28 | H28 | G25 | C7 |
| 0 | 54N | G22 | G27 | H27 | G23 | B6 |
| - | - | VCCO0 | - | - | - | VCCO0 |
| 0 | 54P | G21 | G26 | H26 | - | E7 |
| - | - | GND (Bank 0) | - | - | - | GND (Bank 0) |
| 0 | 55N | G20 | G25 | H25 | - | E6 |
| 0 | 55P | G18 | G24 | H24 | G19 | A6 |
| 0 | 56N | G16/VREF0 | G3 | H3 | G17 | A5 |
| 0 | 56P | G14 | G2 | H2 | G15 | A4 |
| 0 | 57N | G12 | G23 | H23 | G13 | B5 |
| 0 | 57P | G10 | G22 | H22 | G11 | A3 |
| 0 | 58N | G8 | G21 | H21 | G9 | B4 |
| 0 | 58P | G6 | G20 | H20 | G7 | B3 |
| 0 | 59N | G5 | G19 | H19 | - | C5 |
| 0 | 59P | G4 | G18 | H18 | - | C6 |
| 0 | 60N | G2 | G1 | H1 | G3 | D5 |
| 0 | 60P | G0 | G0 | H0 | G1 | D6 |
| - | - | VCCO0 | - | - | - | VCCO0 |
| - | - | GND (Bank 0) | - | - | - | GND (Bank 0) |

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

## ispXPLD 5512MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 208 PQFP Pin Number | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | | |
| 1 | 13P | B24 | A16 | — | B25 | — | T4 | V6 |
| — | — | $V_{CCO1}$ | — | — | — | 57 | $V_{CCO1}$ | $V_{CCO1}$ |
| 1 | 13N | B26 | A18 | — | B27 | — | T5 | V7 |
| 1 | 14P | B28 | A20 | — | B29 | — | R4 | Y5 |
| 1 | 14N | B30 | A22 | — | B31 | — | N6 | AA5 |
| 1 | 15P | C0 | — | — | C1 | — | R5 | Y6 |
| 1 | 15N | C2 | — | — | C3 | — | P6 | Y7 |
| 1 | 16P | C4 | — | — | C5 | — | — | AA6 |
| 1 | 16N | C8 | — | — | C9 | — | — | AA7 |
| 1 | 17P | C10 | — | — | C11 | — | — | W7 |
| 1 | 17N | C12 | — | — | C13 | — | M7[1] | V8 |
| 1 | 18P | C16 | — | — | C17 | — | T6 | W8 |
| 1 | 18N | C18 | — | — | C19 | — | R6 | U9 |
| — | — | GND0 (Bank 1) | — | — | — | — | GND (Bank 1) | GND (Bank 1) |
| — | — | CFG0 | — | — | — | 58 | L8 | U10 |
| — | — | $V_{CCO1}$ | — | — | — | — | $V_{CCO1}$ | $V_{CCO1}$ |
| 1 | 19P | C24 | B16 | D16 | C25 | 59 | T7 | AB7 |
| 1 | 19N | C26 | B17 | D17 | C27 | 60 | R7 | AA8 |
| 1 | 20P | C28 | B18 | D18 | C29 | 61 | N7 | AB8 |
| 1 | 20N | D0 | B19 | D19 | D1 | 62 | P7 | AB9 |
| 1 | 21P | D2 | B20 | D20 | D3 | 63 | T8 | W9 |
| 1 | 21N | D4 | B21 | D21 | D5 | 64 | R8 | Y9 |
| 1 | 22P | D6 | B22 | D22 | D7 | 65 | M8 | AB10 |
| 1 | 22N | D8 | B23 | D23 | D9 | 66 | P8 | AA10 |
| 1 | — | D10/$V_{REF1}$ | — | — | D11 | 67 | L9 | W10 |
| 1 | 23P | D12 | B24 | D24 | D13 | 68 | N8 | Y10 |
| 1 | 23N | D16 | B25 | D25 | D17 | 69 | M9 | Y11 |
| — | — | GND (Bank 1) | — | — | — | 70 | GND (Bank 1) | GND (Bank 1) |
| 1 | 24P | D18 | B26 | D26 | D19 | 71 | N10 | V9 |
| — | — | VCCO1 | — | — | — | 72 | $V_{CCO1}$ | $V_{CCO1}$ |
| 1 | 24N | D20 | B27 | D27 | D21 | 73 | T9 | V10 |
| 1 | 25P | D22 | B28 | D28 | D23 | 74 | T10 | AA11 |
| 1 | 25N | D24 | B29 | D29 | D25 | 75 | R9 | AB11 |
| — | — | VCC | — | — | — | 76 | VCC | VCC |
| 1 | 26P | D26 | B30 | D30 | D27 | 77 | P9 | U11 |
| 1 | 26N | D28 | B31 | D31 | D29 | 78 | N9 | V11 |
| 2 | 27P | E0 | F0 | H0 | E1 | 79 | T11 | AB12 |
| 2 | 27N | E2 | F1 | H1 | E3 | 80 | T12 | AA12 |
| — | — | GND | — | — | — | 81 | NC | GND |
| — | — | GND | — | — | — | — | GND | GND |
| 2 | 28P | E4 | F2 | H2 | E5 | 82 | P10 | Y12 |
| 2 | 28N | E6 | F3 | H3 | E7 | 83 | R10 | AA13 |
| 2 | 29P | E8 | F4 | H4 | E9 | 84 | R11 | V12 |

## ispXPLD 5512MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 208 PQFP Pin Number | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | | |
| 2 | 47N | G26 | — | — | G27 | 108 | N14 | V19 |
| — | — | GND (Bank 2) | — | — | — | 109 | GND (Bank 2) | GND (Bank 2) |
| 2 | 48P | G28 | F16 | H16 | G29 | 110 | N16 | T18 |
| 2 | 48N | G30 | F17 | H17 | G31 | 111 | M16 | R17 |
| 2 | 49P | H0 | F18 | H18 | H1 | 112 | M14 | U19 |
| 2 | 49N | H2 | F19 | H19 | H3 | 113 | M15 | T19 |
| 2 | 50P | H4 | E24 | — | H5 | — | — | V20 |
| — | — | $V_{CC}$ | — | — | — | 114 | VCC | VCC |
| 2 | 50N | H6 | E26 | — | H7 | — | NC | U20 |
| 2 | 51P | H8 | F20 | H20 | H9 | 115 | L13 | W20 |
| 2 | 51N | H10 | F21 | H21 | H11 | 116 | L12 | Y21 |
| 2 | 52P | H12 | F22 | H22 | H13 | 117 | L15 | R18 |
| 2 | 52N | H14 | F23 | H23 | H15 | 118 | L16 | R19 |
| — | — | GND | — | — | — | 119 | GND | GND |
| 2 | 53P | H16 | F24 | H24 | H17 | 120 | L14 | W21 |
| — | — | $V_{CCO2}$ | — | — | — | 121 | $V_{CCO2}$ | $V_{CCO2}$ |
| 2 | 53N | H18 | F25 | H25 | H19 | 122 | K15 | Y22 |
| — | — | GND (Bank 2) | — | — | — | 123 | GND (Bank 2) | GND (Bank 2) |
| 2 | 54P | H20 | F26 | H26 | H21 | 124 | K14 | R20 |
| 2 | 54N | H22 | F27 | H27 | H23 | 125 | K12 | P20 |
| 2 | 55P | H24 | F28 | H28 | H25 | 126 | K13 | T21 |
| 2 | 55N | H26 | F29 | H29 | H27 | 127 | J13 | R21 |
| 2 | 56P | H28 | F30 | H30 | H29 | 128 | J14 | U21 |
| 2 | 56N | H30 | F31 | H31 | H31 | 129 | J12 | V21 |
| — | — | TOE | — | — | — | 130 | J15 | W22 |
| — | — | RESET | — | — | — | 131 | J11 | V22 |
| — | — | GOE0 | — | — | — | 132 | H11 | T22 |
| — | — | GOE1 | — | — | — | 133 | H13 | R22 |
| — | — | GNDP | — | — | — | See Power Supply and NC Connections Table | | |
| — | GCLK3N | GCLK2 | — | — | — | 135 | H15 | P16 |
| — | — | $V_{CCP}$ | — | — | — | See Power Supply and NC Connections Table | | |
| — | GCLK3P | GCLK3 | — | — | — | 137 | H16 | N16 |
| 3 | 57N | I30 | — | — | I31 | 138 | H14 | J22 |
| 3 | 57P | I28 | — | — | I29 | 139 | G16 | H22 |
| 3 | 58N | I26 | — | — | I27 | 140 | G15 | E22 |
| 3 | 58P | I24/PLL_FBK1 | — | — | I25 | 141 | F15 | E21 |
| 3 | 59N | I22/PLL_RST1 | I27 | K27 | I23 | 142 | H12 | G22 |
| 3 | 59P | I20 | I26 | K26 | I21 | 143 | G14 | F21 |
| — | — | GND (Bank 3) | — | — | — | 144 | GND (Bank 3) | GND (Bank 3) |
| 3 | 60N | I18 | I25 | K25 | I19 | 145 | F16 | H21 |
| — | — | VCCO3 | — | — | — | 146 | $V_{CCO3}$ | $V_{CCO3}$ |
| 3 | 60P | I16 | I24 | K24 | I17 | 147 | E16 | G21 |
| — | — | GND | — | — | — | 148 | GND | GND |

## ispXPLD 5512MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 208 PQFP Pin Number | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | | |
| 3 | 79N | K8 | K5 | L8 | K9 | — | — | F13 |
| 3 | 79P | K6 | K4 | L6 | K7 | — | — | F15 |
| 3 | 80N | K5 | K3 | L5 | — | — | — | D16 |
| 3 | 80P | K4 | K2 | L4 | — | — | E10[1] | E16 |
| 3 | 81N | K2 | K1 | L2 | K3 | — | A12 | A16 |
| 3 | 81P | K0 | K0 | L0 | K1 | — | A11 | A15 |
| — | — | GND (Bank 3) | — | — | — | — | GND (Bank 3) | GND (Bank 3) |
| 3 | 82N | L30 | I15 | K15 | L31 | 162 | B11 | B15 |
| — | — | $V_{CCO3}$ | — | — | — | — | $V_{CCO3}$ | $V_{CCO3}$ |
| 3 | 82P | L28 | I14 | K14 | L29 | 163 | C11 | A14 |
| 3 | 83N | L26 | I13 | K13 | L27 | 164 | B10 | D15 |
| 3 | 83P | L24 | I12 | K12 | L25 | 165 | A10 | E15 |
| 3 | 84N | L22 | I11 | K11 | L23 | 166 | C10 | D14 |
| 3 | 84P | L21 | I10 | K10 | — | 167 | D10 | F14 |
| 3 | 85N | L20 | I9 | K9 | — | 168 | C9 | A13 |
| 3 | 85P | L18 | I8 | K8 | L19 | 169 | E9 | B13 |
| 3 | 86N | L16/VREF3 | I29 | K29 | L17 | 170 | D9 | C14 |
| 3 | 86P | L14 | I28 | K28 | L15 | 171 | F9 | E14 |
| 3 | 87N | L12 | I7 | K7 | L13 | 172 | A9 | E13 |
| 3 | 87P | L10 | I6 | K6 | L11 | 173 | F8 | F12 |
| — | — | GND (Bank 3) | — | — | — | 174 | GND (Bank 3) | GND (Bank 3) |
| 3 | 88N | L8 | I5 | K5 | L9 | 175 | E8 | D13 |
| — | — | $V_{CCO3}$ | — | — | — | 176 | $V_{CCO3}$ | $V_{CCO3}$ |
| 3 | 88P | L6 | I4 | K4 | L7 | 177 | A8 | C13 |
| 3 | 89N | L5 | I3 | K3 | — | 178 | B9 | E12 |
| 3 | 89P | L4 | I2 | K2 | — | 179 | D8 | C12 |
| — | — | VCC | — | — | — | 180 | VCC | VCC |
| 3 | 90N | L2 | I1 | K1 | L3 | 181 | B8 | B12 |
| 3 | 90P | L0 | I0 | K0 | L1 | 182 | C8 | A12 |
| 0 | 91N | M30 | M31 | O31 | M31 | 183 | B7 | E11 |
| 0 | 91P | M28 | M30 | O30 | M29 | 184 | A7 | C11 |
| — | — | GND | — | — | — | 185 | — | GND |
| — | — | GND | — | — | — | — | GND | GND |
| 0 | 92N | M26 | M29 | O29 | M27 | 186 | D7 | B11 |
| 0 | 92P | M24 | M28 | O28 | M25 | 187 | C7 | A11 |
| 0 | 93N | M22 | M27 | O27 | M23 | 188 | B6 | F11 |
| — | — | $V_{CCO0}$ | — | — | — | 189 | $V_{CCO0}$ | $V_{CCO0}$ |
| 0 | 93P | M21 | M26 | O26 | M22 | 190 | E7 | F10 |
| — | — | GND (Bank 0) | — | — | — | 191 | GND (Bank 0) | GND (Bank 0) |
| 0 | 94N | M20 | M25 | O25 | M21 | 192 | E6 | E10 |
| 0 | 94P | M18 | M24 | O24 | M19 | 193 | A6 | C10 |
| 0 | 95N | M16/$V_{REF0}$ | M3 | O3 | M17 | 194 | A5 | D10 |
| 0 | 95P | M14 | M2 | O2 | M15 | 195 | A4 | B10 |

## ispXPLD 5512MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 208 PQFP Pin Number | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | | |
| 0 | 96N | M12 | M23 | O23 | M13 | 196 | B5 | A10 |
| 0 | 96P | M10 | M22 | O22 | M11 | 197 | A3 | A9 |
| 0 | 97N | M8 | M21 | O21 | M9 | 198 | B4 | C9 |
| 0 | 97P | M6 | M20 | O20 | M7 | 199 | B3 | D9 |
| 0 | 98N | M5 | M19 | O19 | — | 200 | C5 | F9 |
| 0 | 98P | M4 | M18 | O18 | — | 201 | C6 | E9 |
| 0 | 99N | M2 | M1 | O1 | M3 | 202 | D5 | A8 |
| — | — | $V_{CCO0}$ | — | — | — | — | $V_{CCO0}$ | $V_{CCO0}$ |
| 0 | 99P | M0 | M0 | O0 | M1 | 203 | D6 | B8 |
| — | — | GND (Bank 0) | — | — | — | — | GND (Bank 0) | GND (Bank 0) |
| 0 | 100N | N30 | O29 | — | N31 | — | — | A7 |
| 0 | 100P | N28 | O28 | — | N29 | — | — | B7 |
| 0 | 101N | N26 | O27 | — | N27 | — | — | A5 |
| 0 | 101P | N24 | O26 | — | N25 | — | — | B5 |
| 0 | 102N | N22 | O25 | — | N23 | — | — | B6 |
| 0 | 102P | N21 | O24 | — | — | — | — | C7 |
| 0 | 103N | N20 | O23 | — | — | — | — | E8 |
| 0 | 103P | N18 | O22 | — | N19 | — | — | E7 |
| 0 | 104N | N16 | O21 | — | N17 | — | — | E6 |
| 0 | 104P | N14 | O20 | — | N15 | — | — | D6 |
| 0 | 105N | N12 | O19 | — | N13 | — | — | D8 |
| — | — | $V_{CCO0}$ | — | — | — | 204 | $V_{CCO0}$ | $V_{CCO0}$ |
| 0 | 105P | N10 | O18 | — | N11 | — | — | F8 |
| — | — | GND (Bank 0) | — | — | — | 205 | GND (Bank 0) | GND (Bank 0) |
| 0 | 106N | N8 | O17 | — | N9 | — | — | F7 |
| 0 | 106P | N6 | O16 | — | N7 | — | — | D7 |
| 0 | 107N | N5 | O15 | — | — | 206 | A2 | C6 |
| 0 | 107P | N4 | O14 | — | — | 207 | B2 | C5 |
| 0 | 108N | N2 | O13 | — | N3 | — | — | C4 |
| 0 | 108P | N0 | O12 | — | N1 | — | — | D5 |

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

## ispXPLD 5768MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Inputs | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| 3 | 76P | L30/PLL_FBK1 | L0 | J0 | L31 | F15 | E21 |
| 3 | 77N | M0/PLL_RST1 | P27 | N27 | M1 | H12 | G22 |
| 3 | 77P | M2 | P26 | N26 | M3 | G14 | F21 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 78N | M4 | P25 | N25 | M5 | F16 | H21 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 78P | M6 | P24 | N24 | - | E16 | G21 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 79N | M8 | P23 | N23 | M9 | G13 | D22 |
| 3 | 79P | M10 | P22 | N22 | M11 | G12 | D21 |
| 3 | 80N | M12 | P21 | N21 | M13 | F14 | J20 |
| 3 | 80P | M14/CLK_OUT1 | P20 | N20 | M15 | E15 | J19 |
| 3 | 81N | M16 | N31 | - | M17 | F12 | E20 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 81P | M18 | N30 | M30 | M19 | F13 | F20 |
| 3 | 82N | M20 | N29 | M28 | M21 | D16 | H17 |
| 3 | 82P | M22 | N28 | M26 | M23 | D15 | H18 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 83N | M24 | N27 | - | M25 | — | J18 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 83P | M26 | N26 | - | M27 | — | H19 |
| 3 | 84N | M28 | N25 | - | M29 | — | G20 |
| 3 | 84P | M30 | N24 | - | M31 | — | G19 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 85N | N0 | N23 | - | N1 | — | C22 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 85P | N2 | N22 | - | N3 | — | C21 |
| 3 | 86N | N4 | N21 | - | - | — | D20 |
| 3 | 86P | N6 | N20 | - | - | — | C19 |
| 3 | 87N | N8 | N19 | - | N9 | C16 | F19 |
| 3 | 87P | N10 | N18 | - | N11 | B16 | E19 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 88N | N12 | N17 | - | N13 | C15 | G18 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 88P | N14 | N16 | - | N15 | B15 | F18 |
| 3 | 89N | N16 | N15 | - | N17 | E14 | B20 |
| 3 | 89P | N18 | N14 | - | N19 | D14 | B19 |
| 3 | 90N | N20 | N13 | - | N21 | E13 | A20 |
| 3 | 90P | N22 | N12 | - | N23 | A15 | A19 |
| 3 | 91N | N24 | P19 | N19 | N25 | D12 | D18 |
| 3 | 91P | N26 | P18 | N18 | N27 | B14 | C18 |
| 3 | 92N | N28 | P17 | N17 | N29 | C13 | G17 |
| 3 | 92P | N30 | P16 | N16 | N31 | A14 | F16 |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| 1 | 15N | C0 | A31 | C31 | C1 | — | W5 |
| 1 | 16P | E30/DATA0 | G0 | E0 | E31 | W1 | W1 |
| 1 | 16N | E28/DATA1 | G1 | E1 | E29 | Y1 | Y1 |
| 1 | 17P | E26/DATA2 | G2 | E2 | E27 | P3 | V6 |
| 1 | 17N | E24/DATA3 | G3 | E3 | E25 | R3 | W6 |
| 1 | 18P | E22/DATA4 | G4 | E4 | E23 | T2 | Y2 |
| 1 | 18N | E20/DATA5 | G5 | E5 | E21 | U2 | Y3 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 19P | E18/DATA6 | G6 | E6 | E19 | V2 | Y4 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 19N | E16/DATA7 | G7 | E7 | E17 | W2 | Y5 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 20P | E14/INITB | G8 | E8 | E15 | R4 | V7 |
| 1 | 20N | E12/CSB | G9 | E9 | E13 | T4 | W7 |
| 1 | 21P | E10/READ | G10 | E10 | E11 | R6 | AA1 |
| 1 | 21N | E8/CCLK | G11 | E11 | E9 | R5 | AA2 |
| 1 | 22P | E6 | - | - | E7 | U3 | AA3 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 22N | E4 | - | - | E5 | V3 | AA4 |
| 1 | 23P | E2 | - | - | E3 | Y2 | Y6 |
| 1 | 23N | E0 | - | - | E1 | W3 | AA5 |
| 1 | 24P | F30 | H0 | - | F31 | U5 | AB2 |
| 1 | 24N | F28 | H2 | - | F29 | T5 | AB3 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 25P | F26 | H4 | | F27 | U4 | AB4 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 25N | F24 | H6 | - | F25 | V4 | AB5 |
| 1 | 26P | F22 | H8 | - | F23 | AA3 | AB1 |
| 1 | 26N | F20 | H10 | - | F21 | AB3 | AC2 |
| 1 | - | F18 | H12 | - | F19 | Y4 | AC3 |
| - | - | DONE | - | - | - | AA4 | AC4 |
| 1 | 27P | F14 | - | - | F15 | AB2 | AC1 |
| 1 | 27N | F12 | - | - | F13 | U6 | AD1 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 28P | F10 | | | F11 | V5 | AD2 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 28N | F8 | | | F9 | W6 | AD3 |
| 1 | 29P | F6 | G12 | E12 | F7 | AB4 | Y8 |
| 1 | 29N | F4 | G13 | E13 | F5 | AB5 | Y9 |
| 1 | 30P | F2 | G14 | E14 | F3 | T6 | AA8 |
| 1 | 30N | F0 | G15 | E15 | F1 | U7 | AA9 |
| - | - | PROGRAMB | - | - | - | W5 | AB8 |
| 1 | - | G28 | H14 | - | G29 | U8 | AB9 |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| - | GCLK3P | GCLK3 | - | - | - | N16 | N24 |
| 3 | 93N | R0 | T31 | R31 | R1 | J22 | N23 |
| 3 | 93P | R2 | T30 | R30 | R3 | H22 | N22 |
| 3 | 94N | R4 | T29 | R29 | R5 | N19 | M26 |
| 3 | 94P | R6 | T28 | R28 | R7 | P15 | M25 |
| 3 | 95N | R8 | T27 | R27 | R9 | P21 | M23 |
| 3 | 95P | R10 | T26 | R26 | R11 | N15 | M22 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 96N | R12 | T25 | R25 | R13 | M15 | N20 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 96P | R14 | T24 | R24 | R15 | N20 | M20 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 97N | R16 | T23 | R23 | R17 | P22 | N21 |
| 3 | 97P | R18 | T22 | R22 | R19 | N21 | M21 |
| 3 | 98N | R20 | T21 | R21 | R21 | N17 | M24 |
| 3 | 98P | R22 | T20 | R20 | R23 | M20 | L24 |
| 3 | 99N | R24 | T19 | R19 | R25 | P17 | L23 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 99P | R26 | T18 | R18 | R27 | P18 | L22 |
| 3 | 100N | R28 | T17 | R17 | R29 | M21 | L25 |
| 3 | 100P | R30 | T16 | R16 | R31 | M17 | K26 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 101N | T0 | T15 | R15 | T1 | L20 | K25 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 101P | T2 | T14 | R14 | T3 | N18 | K24 |
| 3 | 102N | T4 | T13 | R13 | T5 | L21 | K23 |
| 3 | 102P | T6 | T12 | R12 | T7 | M18 | K22 |
| 3 | 103N | T8 | T11 | R11 | T9 | L22 | J25 |
| 3 | 103P | T10 | T10 | R10 | T11 | L17 | J24 |
| 3 | 104N | T12 | T9 | R9 | T13 | K22 | L21 |
| 3 | 104P | T14 | T8 | R8 | T15 | L18 | K21 |
| 3 | 105N | T16 | T7 | R7 | T17 | K21 | L20 |
| 3 | 105P | T18 | T6 | R6 | T19 | K18 | K20 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 106N | T20 | T5 | R5 | T21 | K20 | J23 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 106P | T22 | T4 | R4 | T23 | K17 | J22 |
| 3 | 107N | T24 | T3 | R3 | T25 | K19 | J26 |
| 3 | 107P | T26 | T2 | R2 | T27 | J17 | H26 |
| 3 | 108N | T28 | T1 | R1 | T29 | E22 | H25 |
| 3 | 108P | T30/PLL_FBK1 | T0 | R0 | T31 | E21 | H24 |
| 3 | 109N | U0/PLL_RST1 | X27 | V27 | U1 | G22 | H23 |
| 3 | 109P | U2 | X26 | V26 | U3 | F21 | H22 |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 110N | U4 | X25 | V25 | U5 | H21 | J21 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 110P | U6 | X24 | V24 | U7 | G21 | H21 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 111N | U8 | X23 | V23 | U9 | D22 | G25 |
| 3 | 111P | U10 | X22 | V22 | U11 | D21 | G24 |
| 3 | 112N | U12 | X21 | V21 | U13 | J20 | G23 |
| 3 | 112P | U14/CLK_OUT1 | X20 | V20 | U15 | J19 | G22 |
| 3 | 113N | U16 | V31 | - | U17 | E20 | J20 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 113P | U18 | V30 | U30 | U19 | F20 | H20 |
| 3 | 114N | U20 | V29 | U28 | U21 | H17 | G26 |
| 3 | 114P | U22 | V28 | U26 | U23 | H18 | F25 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 115N | U24 | V27 | - | U25 | J18 | F24 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 115P | U26 | V26 | - | U27 | H19 | F23 |
| 3 | 116N | U28 | V25 | - | U29 | G20 | G21 |
| 3 | 116P | U30 | V24 | - | U31 | G19 | F22 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 117N | V0 | V23 | - | V1 | C22 | F26 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 117P | V2 | V22 | - | V3 | C21 | E26 |
| 3 | 118N | V4 | V21 | - | V5 | D20 | E25 |
| 3 | 118P | V6 | V20 | - | V7 | C19 | E24 |
| 3 | 119N | V8 | V19 | - | V9 | F19 | E23 |
| 3 | 119P | V10 | V18 | - | V11 | E19 | E22 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 120N | V12 | V17 | - | V13 | G18 | D26 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 120P | V14 | V16 | - | V15 | F18 | D25 |
| 3 | 121N | V16 | V15 | - | V17 | B20 | D24 |
| 3 | 121P | V18 | V14 | - | V19 | B19 | D23 |
| 3 | 122N | V20 | V13 | - | V21 | A20 | C26 |
| 3 | 122P | V22 | V12 | - | V23 | A19 | C25 |
| 3 | 123N | V24 | X19 | V19 | V25 | D18 | G19 |
| 3 | 123P | V26 | X18 | V18 | V27 | C18 | F19 |
| 3 | 124N | V28 | X17 | V17 | V29 | G17 | G18 |
| 3 | 124P | V30 | X16 | V16 | V31 | F16 | F18 |
| 3 | 125N | W0 | X31 | V31 | W1 | E17 | F20 |
| 3 | 125P | W2 | X30 | V30 | W3 | D17 | E20 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |

### ispXPLD 5000MB (2.5V) Lead-Free Commercial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MB | LC5256MB-4FN256C | 256 | 2.5 | 4.0 | Lead-free fpBGA | 256 | 141 | C |
| | LC5256MB-5FN256C | 256 | 2.5 | 5.0 | Lead-free fpBGA | 256 | 141 | C |
| | LC5256MB-75FN256C | 256 | 2.5 | 7.5 | Lead-free fpBGA | 256 | 141 | C |
| LC5512MB | LC5512MB-45QN208C | 512 | 2.5 | 4.5 | Lead-free PQFP | 208 | 149 | C |
| | LC5512MB-75QN208C | 512 | 2.5 | 7.5 | Lead-free PQFP | 208 | 149 | C |
| | LC5512MB-45FN256C | 512 | 2.5 | 4.5 | Lead-free fpBGA | 256 | 193 | C |
| | LC5512MB-75FN256C | 512 | 2.5 | 7.5 | Lead-free fpBGA | 256 | 193 | C |
| | LC5512MB-45FN484C | 512 | 2.5 | 4.5 | Lead-free fpBGA | 484 | 253 | C |
| | LC5512MB-75FN484C | 512 | 2.5 | 7.5 | Lead-free fpBGA | 484 | 253 | C |
| LC5768MB | LC5768MB-5FN256C | 768 | 2.5 | 5.0 | Lead-free fpBGA | 256 | 193 | C |
| | LC5768MB-75FN256C | 768 | 2.5 | 7.5 | Lead-free fpBGA | 256 | 193 | C |
| | LC5768MB-5FN484C | 768 | 2.5 | 5.0 | Lead-free fpBGA | 484 | 317 | C |
| | LC5768MB-75FN484C | 768 | 2.5 | 7.5 | Lead-free fpBGA | 484 | 317 | C |
| LC51024MB | LC51024MB-52FN484C | 1024 | 2.5 | 5.2 | Lead-free fpBGA | 484 | 317 | C |
| | LC51024MB-75FN484C | 1024 | 2.5 | 7.5 | Lead-free fpBGA | 484 | 317 | C |
| | LC51024MB-52FN672C | 1024 | 2.5 | 5.2 | Lead-free fpBGA | 672 | 381 | C |
| | LC51024MB-75FN672C | 1024 | 2.5 | 7.5 | Lead-free fpBGA | 672 | 381 | C |

### ispXPLD 5000MB (2.5V) Lead-Free Industrial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MB | LC5256MB-5FN256I | 256 | 2.5 | 5.0 | Lead-free fpBGA | 256 | 141 | I |
| | LC5256MB-75FN256I | 256 | 2.5 | 7.5 | Lead-free fpBGA | 256 | 141 | I |
| LC5512MB | LC5512MB-75QN208I | 512 | 2.5 | 7.5 | Lead-free PQFP | 208 | 149 | I |
| | LC5512MB-75FN256I | 512 | 2.5 | 7.5 | Lead-free fpBGA | 256 | 193 | I |
| | LC5512MB-75FN484I | 512 | 2.5 | 7.5 | Lead-free fpBGA | 484 | 253 | I |
| LC5768MB | LC5768MB-75FN256I | 768 | 2.5 | 7.5 | Lead-free fpBGA | 256 | 193 | I |
| | LC5768MB-75FN484I | 768 | 2.5 | 7.5 | Lead-free fpBGA | 484 | 317 | I |
| LC51024MB | LC51024MB-75FN484I | 1024 | 2.5 | 7.5 | Lead-free fpBGA | 484 | 317 | I |
| | LC51024MB-75FN672I | 1024 | 2.5 | 7.5 | Lead-free fpBGA | 672 | 381 | I |

### ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MV | LC5256MV-4FN256C | 256 | 3.3 | 4.0 | Lead-free fpBGA | 256 | 141 | C |
| | LC5256MV-5FN256C | 256 | 3.3 | 5.0 | Lead-free fpBGA | 256 | 141 | C |
| | LC5256MV-75FN256C | 256 | 3.3 | 7.5 | Lead-free fpBGA | 256 | 141 | C |

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| — | — | Previous Lattice releases. |
| December 2003 | 07 | Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers). |
| | | Updated ispXPLD 5000MX timing numbers (version v.1.7). |
| | | Added lead-free package designator. |
| | | Removed ispXPLD 5000MC industrial temperature grade ordering part numbers. |
| January 2004 | 08 | Lead-free package release for the ispXPLD 5000MC and 5000MV devices. |
| | | Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers). |
| March 2004 | 08.1 | Updated the MFB Cascade Chain table for the ispXPLD 5256MX device. |
| May 2004 | 09 | Updated the ispXPLD 5000MX timig numbers (version v.1.8)<br>ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release |
| | | Updated typical supply current data and condition. |
| | | ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14. |
| August 2004 | 10 | Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ. |
| | | Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free). |
| October 2004 | 10.1 | Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer) |
| November 2004 | 11 | Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers. |
| December 2004 | 11.1 | Pin name RESETB has been updated to RESET. |
| March 2005 | 12 | 208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices. |
| April 2005 | 12.1 | Page 23, clarification of footnote regarding IDK specification. |
| March 2006 | 12.2 | Signal description for RESET has been updated. |
| April 2009 | 12.3 | Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format. |
| February 2010 | 12.4 | References to "system gates" changed to "functional gates." |