Lattice Semiconductor Corporation - LC5512MB-75F256I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	193
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mb-75f256i

Product Line	Ordering Part Number	Product Status	Reference PCN
LC51024MV	LC51024MV-52F484C	Active / Orderable	
	LC51024MV-52FN484C		
	LC51024MV-75F484C		
	LC51024MV-75FN484C		
	LC51024MV-75F484I		
	LC51024MV-75FN484I		
	LC51024MV-52F672C		
	LC51024MV-52FN672C		
	LC51024MV-75F672C		
	LC51024MV-75FN672C		
	LC51024MV-75F672I		
	LC51024MV-75FN672I		
LC51024MB	LC51024MB-52F484C	**Discontinued**	PCN#09-10
	LC51024MB-52FN484C		
	LC51024MB-75F484C		
	LC51024MB-75FN484C		
	LC51024MB-75F484I		
	LC51024MB-75FN484I		
	LC51024MB-52F672C		
	LC51024MB-52FN672C		
	LC51024MB-75F672C		
	LC51024MB-75FN672C		
	LC51024MB-75F672I		
	LC51024MB-75FN672I		
LC51024MC	LC51024MC-52F484C	**Discontinued**	PCN#09-10
	LC51024MC-52FN484C		
	LC51024MC-75F484C		
	LC51024MC-75FN484C		
	LC51024MC-75F484I		
	LC51024MC-75FN484I		
	LC51024MC-52F672C		
	LC51024MC-52FN672C		
	LC51024MC-75F672C		
	LC51024MC-75FN672C		
	LC51024MC-75F672I		
	LC51024MC-75FN672I		

Figure 3. MFB in SuperWIDE Logic Mode†

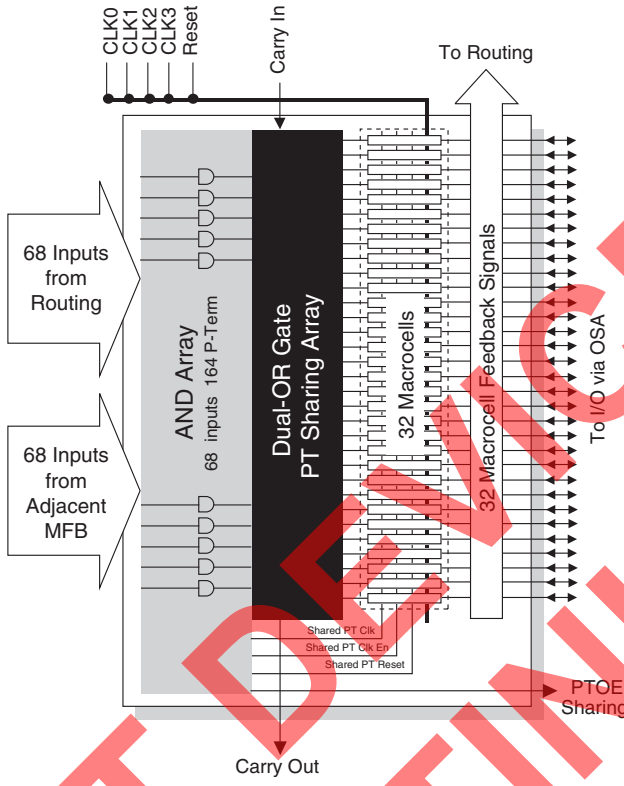
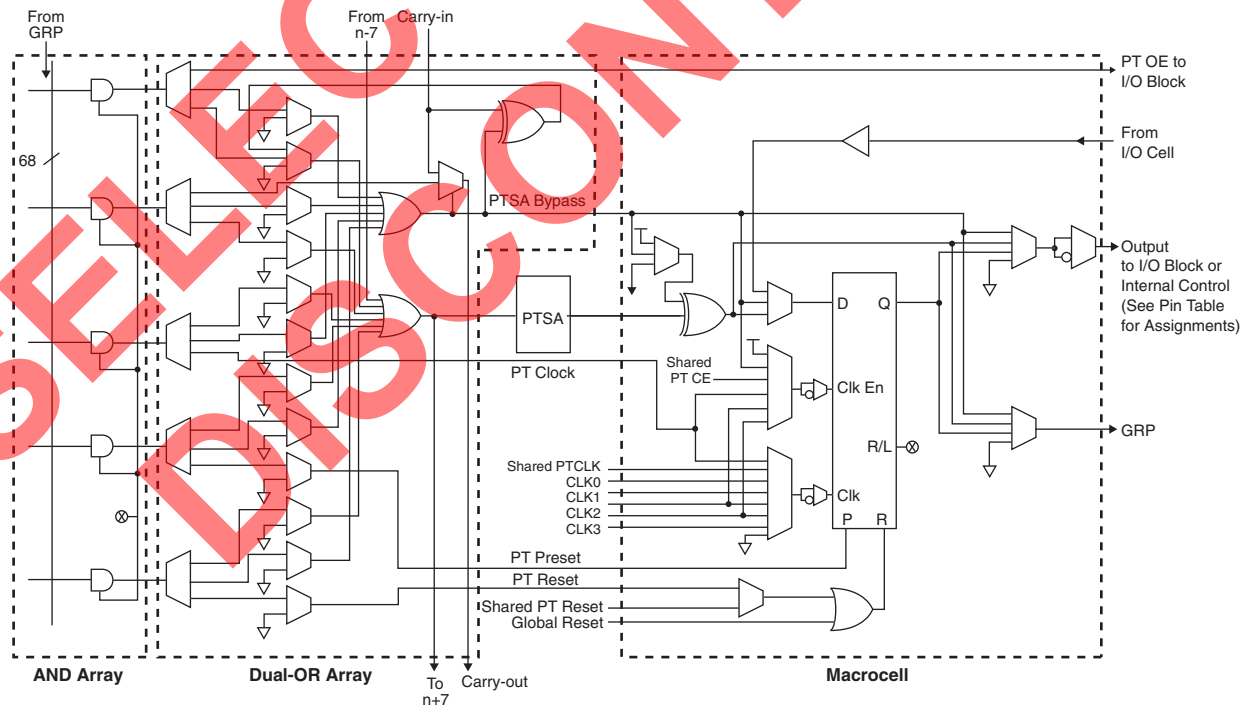


Figure 4. Macrocell Slice in Logic Mode AND-Array



Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

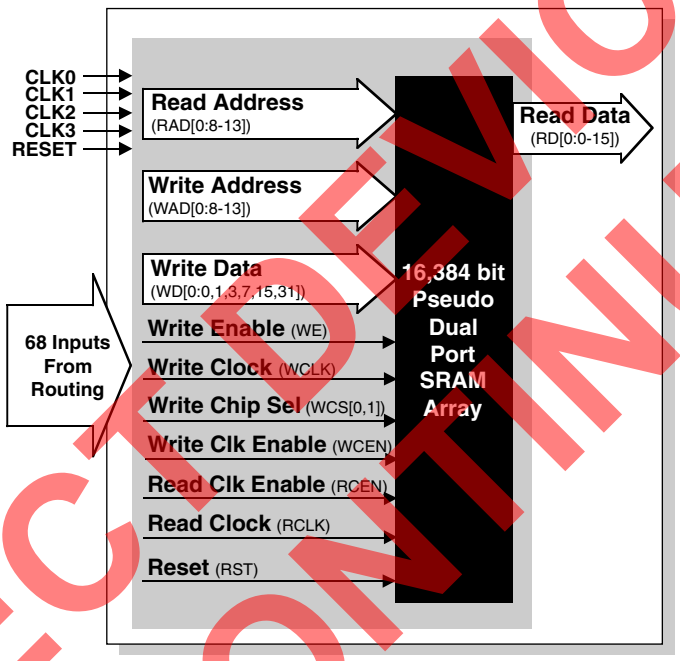


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

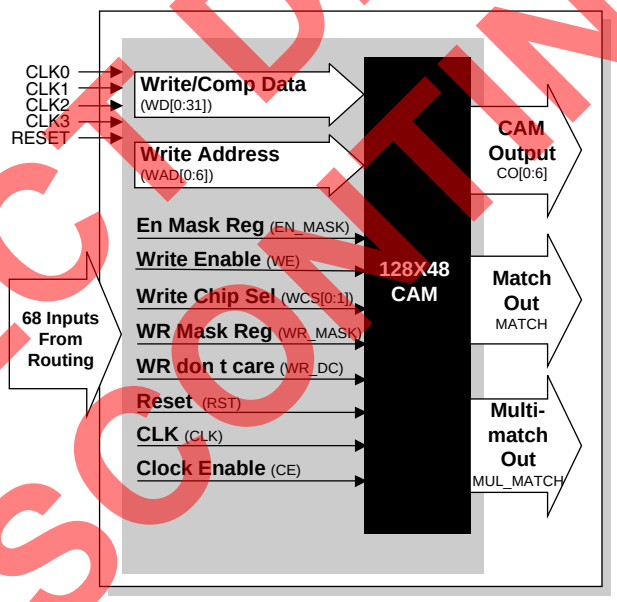


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

Output Sharing Array (OSA)

A number of I/O pads are available in each sysIO bank to route the selected number of macrocells from the MFB outputs directly to the I/O pads in logic mode. In the ispXPLD 5000MX, the large number of inputs and PTs to the MFB as well as the presence of the PTSA can cover most routing flexibility of signals to I/O cells. The Output Sharing Array gives additional routing capability and I/O access to an MFB when a wide output function takes up the whole MFB and cannot be easily divided across multiple MFBs. By using the OSA, the wide output function, such as 32-bit FIFO, can have all of its output signals from the one MFB routed to I/O cells. In a given I/O block, the wide output functions must share the I/O pads with other logic functions.

The OSA bypass option routes the MFB signal directly to the I/O cell, allowing a direct connection to the I/O cell. The logic functions use the option to provide faster speed to the outputs. The Logic Signal Connection tables list the OSA bypass as the primary macrocell and OSA options as alternate macrocells. Similarly, the Alternate Input listing in the table shows the alternate macrocell input connection for a given I/O pin. Figure 17 shows the alternate macrocell connections in an I/O cell.

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedback line to its associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The MFBs are grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PTOE signal is derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

Programmable Slew Rate

The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices support two slew rates. This allows system noise and performance to be balanced in a design.

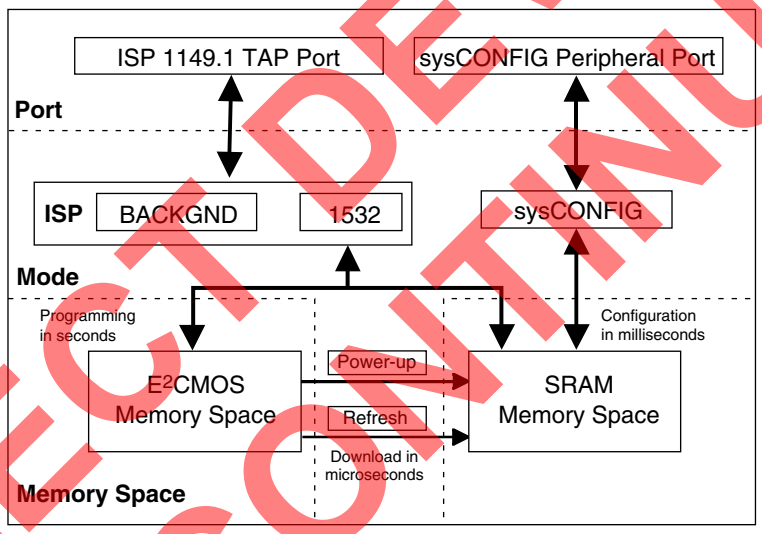
Programmable Bus-Maintenance

All general-purpose inputs have programmable bus maintenance circuitry. These are intended to maintain a valid logic level into a device when driving devices go into the tri-state mode. Four options are available for users: pull-up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device. Figure 18 shows the different ports and modes that are used in the configuration and programming of the ispXPLD 5000MX devices.

Figure 18. ispXP Block Diagram



IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfiguration of the SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during the testing of a circuit board.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) < V_{IN} ð 3.6V	—	—	40	µA
I_{IH}[4]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}[3]	I/O Active Pullup Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{CCO} * 0.35	—	V_{CCO} * 0.65	µA
C1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz
3. I_{PU} on JTAG pins has a maximum of -175µA for 5512MX devices.
4. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

sysIO Differential DC Electrical Characteristics

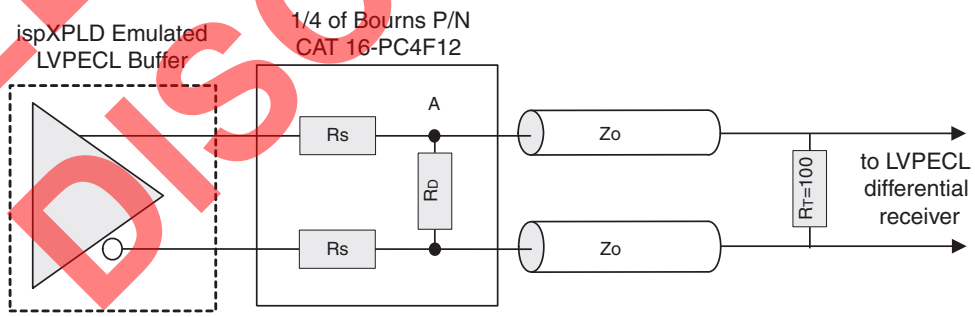
Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS					
V_{INP}	Input Voltage		0V	—	2.4V
V_{THD}	Differential Input Threshold	0.2 ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input Current	Power On	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50mV
V_{OS}	Output Voltage Offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125V	1.20V	1.375V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—	24mA

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input voltage	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 19). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V

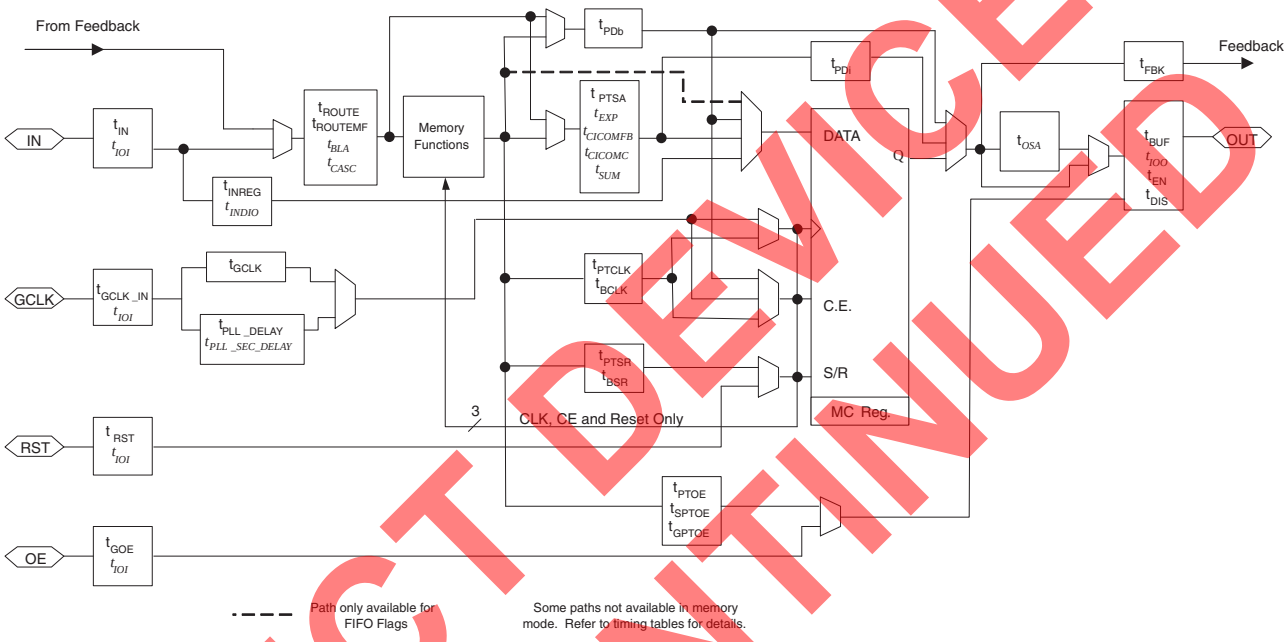
Figure 19. LVPECL Driver with Three Resistor Pack



Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	"Don't Care" Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	"Don't Care" Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—	8.54	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
Dual Port RAM													
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84	—	ns
t_{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDAS}$	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDAH}$	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATAAS}$	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATAAH}$	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns

Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

ispXPLD 5000MX Power Supply and NC Connections[1]

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
2	20P	C14	-	-	C15	P11
2	20N	C16/VREF2	-	-	C17	T14
2	21P	C18	C8	D8	C19	R12
2	21N	C20	C9	D9	-	R13
2	22P	C21	C10	D10	-	N11
2	22N	C22	C11	D11	C23	T15
2	23P	C24	C12	D12	C25	R14
2	23N	C26	C13	D13	C27	N12
2	24P	C28	C14	D14	C29	P12
2	24N	C30	C15	D15	C31	R15
-	-	VCCO2	-	-	-	VCCO2
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	25P	D0	-	-	D1	N15
2	25N	D2	-	-	D3	N14
2	26P	D4	C16	D16	-	N16
2	26N	D5	C17	D17	-	M16
2	27P	D6	C18	D18	D7	M14
2	27N	D8	C19	D19	D9	M15
-	-	VCC	-	-	-	VCC
2	28P	D10	C20	D20	D11	L13
2	28N	D12	C21	D21	D13	L12
2	29P	D14	C22	D22	D15	L15
2	29N	D16	C23	D23	D17	L16
-	-	GND	-	-	-	GND
2	30P	D18	C24	D24	D19	L14
-	-	VCCO2	-	-	-	VCCO2
2	30N	D20	C25	D25	-	K15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	31P	D21	C26	D26	-	K14
2	31N	D22	C27	D27	D23	K12
2	32P	D24	C28	D28	D25	K13
2	32N	D26	C29	D29	D27	J13
2	33P	D28	C30	D30	D29	J14
2	33N	D30	C31	D31	D31	J12
-	-	TOE	-	-	-	J15
-	-	RESET	-	-	-	J11
-	-	GOE0	-	-	-	H11
-	-	GOE1	-	-	-	H13
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3N	GCLK2	-	-	-	H15
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3P	GCLK3	-	-	-	H16

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	GCLK0N	GCLK1	—	—	—	28	J2	P7
—	—	GND	—	—	—	29	GND	GND
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	V_{CCO1}
1	3N	A14/DATA7	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	—	—	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	—	P1[1]	V3
1	7P	A28	—	—	A29	—	M3	Y2
1	7N	A30	—	—	A31	—	L4	W3
1	8P	B0	A0	—	B1	—	N2	U5
1	8N	B2	A2	—	B3	—	P2	T5
—	—	GND (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	—	R1	U4
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	9N	B5	A6	—	—	—	R2	V4
1	10P	B6	A8	—	B7	—	T2	AA3
1	10N	B8	A10	—	B9	—	T3	AB3
1	—	B10	A12	—	B11	—	—	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	—	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	V_{CCO2}
2	29N	E10	F5	H5	E11	86	M10	U12
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	GND (Bank 2)
2	30P	E12	F6	H6	E13	88	M11	AB13
2	30N	E16	F7	H7	E17	89	T13	Y13
2	31P	E18	—	—	E19	90	P11	V13
2	31N	E20/V_{REF2}	—	—	E21	91	T14	W13
2	32P	E22	F8	H8	E23	92	R12	V14
2	32N	E24	F9	H9	E25	93	R13	W14
2	33P	E26	F10	H10	E27	94	N11	Y14
2	33N	E28	F11	H11	E29	95	T15	AB14
2	34P	F0	F12	H12	F1	96	R14	AB15
2	34N	F2	F13	H13	F3	97	N12	AA15
2	35P	F4	F14	H14	F5	98	P12	U13
—	—	V_{CCO2}	—	—	—	—	V_{CCO2}	V_{CCO2}
2	35N	F6	F15	H15	F7	99	R15	U14
—	—	GND (Bank 2)	—	—	—	—	GND (Bank 2)	GND (Bank 2)
2	36P	F8	E0	—	F9	—	—	W15
2	36N	F10	E2	—	F11	—	—	W16
2	37P	F12	E4	—	F13	—	—	Y16
2	37N	F16	E6	—	F17	—	—	AA16
2	38P	F18	E8	—	F19	—	—	AB16
2	38N	F20	E10	—	F21	—	—	AA17
2	39P	F22	E12	—	F23	—	—	Y17
2	39N	F24	E16	—	F25	—	—	AA18
2	40P	F26	E20	—	F27	—	—	W17
2	40N	F28	E22	—	F29	—	—	W18
2	41P	G0	—	—	G1	—	—	V15
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	V_{CCO2}
2	41N	G2	—	—	G3	—	—	U15
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	GND (Bank 2)
2	42P	G4	—	—	G5	102	P13	Y18
2	42N	G6	—	—	G7	103	P15	V17
2	43P	G8	—	—	G9	—	M13	V16
2	43N	G10	—	—	G11	—	P14	U16
2	44P	G12	—	—	G13	—	—	AB18
2	44N	G14	—	—	G15	—	—	AB19
2	45P	G16	—	—	G17	—	—	U18
2	45N	G18	—	—	G19	—	—	T17
2	46P	G20	—	—	G21	104	R16	AB20
2	46N	G22	—	—	G23	105	P16	AA20
2	47P	G24	—	—	G25	106	N15	Y19
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	V_{CCO2}

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	B4
0	127P	S20	S10	T16	S21	E4	A4
0	128N	S18	Q17	S17	S19	B1	B3
0	128P	S16	Q16	S16	S17	C1	A3
0	129N	S14	Q15	S15	S15	D3	F5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	129P	S12	Q14	S14	S13	C2	G6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	130N	S10	Q13	S13	S11	E3	H6
0	130P	S8	Q12	S12	S9	D2	G5
0	131N	S6	S9	T14	S7	—	D3
0	131P	S4	S8	T12	S5	—	D2
0	132N	S2	S7	T10	S3	—	E4
-	-	VCC	-	-	-	VCC	VCC
0	132P	S0	S6	T8	S1	—	E3
-	-	GND	-	-	-	GND	GND
0	133N	T30	S5	T6	T31	—	F4
0	133P	T28	S4	T4	T29	—	G4
0	134N	T26	S3	T2	T27	—	C2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	134P	T24	S2	T0	T25	—	C1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	135N	T22	S1	-	T23	D1	F3
0	135P	T20	S0	-	T21	E1	G3
0	136N	T18	S31	-	T19	F4	H4
-	-	VCC	-	-	-	VCC	VCC
0	136P	T16	S30	-	T17	F5	J4
0	137N	T14	Q11	S11	T15	E2	H5
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	J5
0	138N	T10	Q9	S9	T11	F1	E2
0	138P	T8	Q8	S8	T9	G1	F2
-	-	GND	-	-	-	GND	GND
0	139N	T6	Q7	S7	T7	F3	D1
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	139P	T4	Q6	S6	T5	G5	E1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	140N	T2	Q5	S5	T3	H5	J3
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	H2
0	141N	U30	U31	W31	U31	G3	G2
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	G1
0	142N	U26	U29	W29	U27	—	J6
0	142P	U24	U28	W28	U25	—	K4

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	93N	O0	P31	N31	O1	A13	E17
3	93P	O2	P30	N30	O3	B13	D17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	94N	O4	N11	M21	O5	D11	B18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	94P	O6	N10	M20	O7	B12	A18
-	-	GND	-	-	-	GND	GND
3	95N	O8	N9	M18	O9	C12	C17
-	-	VCC	-	-	-	VCC	VCC
3	95P	O10	N8	M16	O11	E11	B17
3	96N	O12	N7	M12	O13	—	C16
3	96P	O14	N6	M10	O15	—	B16
3	97N	O16	N5	M8	O17	—	F13
3	97P	O18	N4	M6	O19	—	F15
3	98N	O20	N3	M5	O21	—	D16
3	98P	O22	N2	M4	O23	E10	E16
3	99N	O24	N1	M2	O25	A12	A16
3	99P	O26	N0	M0	O27	A11	A15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	100N	O28	P15	N15	O29	B11	B15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	100P	O30	P14	N14	O31	C11	A14
3	101N	P0	P13	N13	P1	B10	D15
3	101P	P2	P12	N12	P3	A10	E15
3	102N	P4	P11	N11	P5	C10	D14
3	102P	P6	P10	N10	P7	D10	F14
3	103N	P8	P9	N9	P9	C9	A13
3	103P	P10	P8	N8	P11	E9	B13
3	104N	P12/VREF3	P29	N29	P13	D9	C14
3	104P	P14	P28	N28	P15	F9	E14
3	105N	P16	P7	N7	P17	A9	E13
3	105P	P18	P6	N6	P19	F8	F12
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	P20	P5	N5	P21	E8	D13
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	P22	P4	N4	P23	A8	C13
3	107N	P24	P3	N3	P25	B9	E12
-	-	GND	-	-	-	GND	GND
3	107P	P26	P2	N2	P27	D8	C12
-	-	VCC	-	-	-	VCC	VCC
3	108N	P28	P1	N1	P29	B8	B12
3	108P	P30	P0	N0	P31	C8	A12
0	109N	Q30	Q31	S31	Q31	B7	E11

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	79N	N10	P5	N5	N11	—	V26
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	80P	N12	P6	N6	N13	—	V22
2	80N	N14	P7	N7	N15	—	V23
2	81P	N16	P8	N8	N17	—	V24
2	81N	N18	P9	N9	N19	—	V25
2	82P	N20	P10	N10	N21	—	U20
2	82N	N22	P11	N11	N23	—	T20
2	83P	N24	P12	N12	N25	—	U26
2	83N	N26	P13	N13	N27	—	U25
2	84P	N28	P14	N14	N29	—	U21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	84N	N30	P15	N15	N31	—	T21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	85P	P0	P16	N16	P1	—	U22
2	85N	P2	P17	N17	P3	—	U23
2	86P	P4	P18	N18	P5	—	U24
2	86N	P6	P19	N19	P7	—	T24
2	87P	P8	P20	N20	P9	—	T23
2	87N	P10	P21	N21	P11	—	T22
2	88P	P12	P22	N22	P13	—	T25
-	-	VCC	-	-	-	VCC	VCC
2	88N	P14	P23	N23	P15	—	R26
-	-	GND	-	-	-	GND	GND
2	89P	P16	P24	N24	P17	—	R25
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	89N	P18	P25	N25	P19	—	R24
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	90P	P20	P26	N26	P21	—	R21
2	90N	P22	P27	N27	P23	—	P21
2	91P	P24	P28	N28	P25	—	R22
2	91N	P26	P29	N29	P27	—	R23
2	92P	P28	P30	N30	P29	—	R20
2	92N	P30	P31	N31	P31	—	P20
-	-	TOE	-	-	-	W22	P25
-	-	RESET	-	-	-	V22	P24
-	-	GOE0	-	-	-	T22	P23
-	-	GOE1	-	-	-	R22	P22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3N	GCLK2	-	-	-	P16	N26
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	