# Lattice Semiconductor Corporation - LC5512MB-75FN256I Datasheet


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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 2.3V ~ 2.7V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 512 |
| Number of Gates | - |
| Number of I/O | 193 |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mb-75fn256i |

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

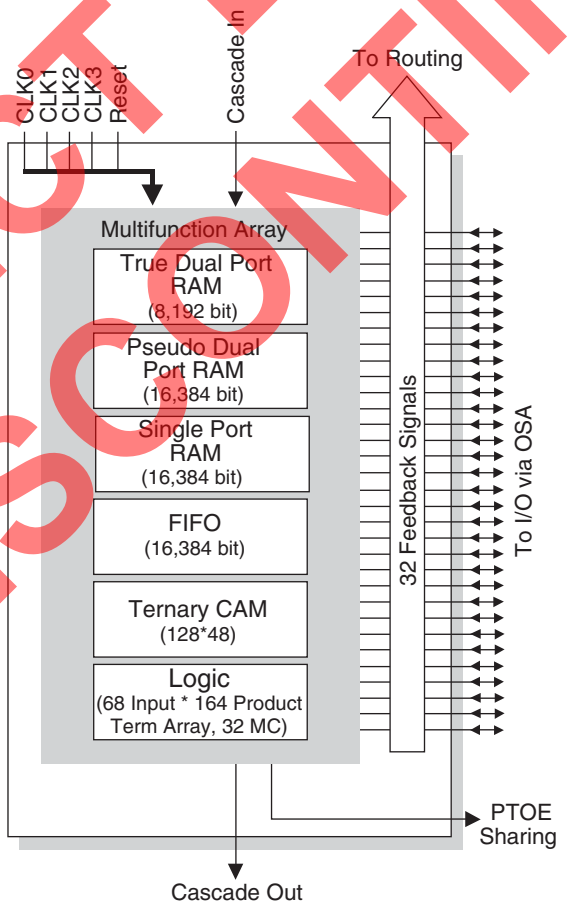
## Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

***Figure 2. MFB Block Diagram***



## True Dual-Port SRAM Mode

In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two independent read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are supported by the MFB. Figure 9 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Resets are asynchronous. All inputs on the same port share the same clock, clock enable, and reset selections. All outputs on the same port share the same clock, clock enable, and reset selections. Selections may be made independently between both inputs and outputs and ports. Table 5 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

***Figure 9. Dual-Port SRAM Block Diagram***

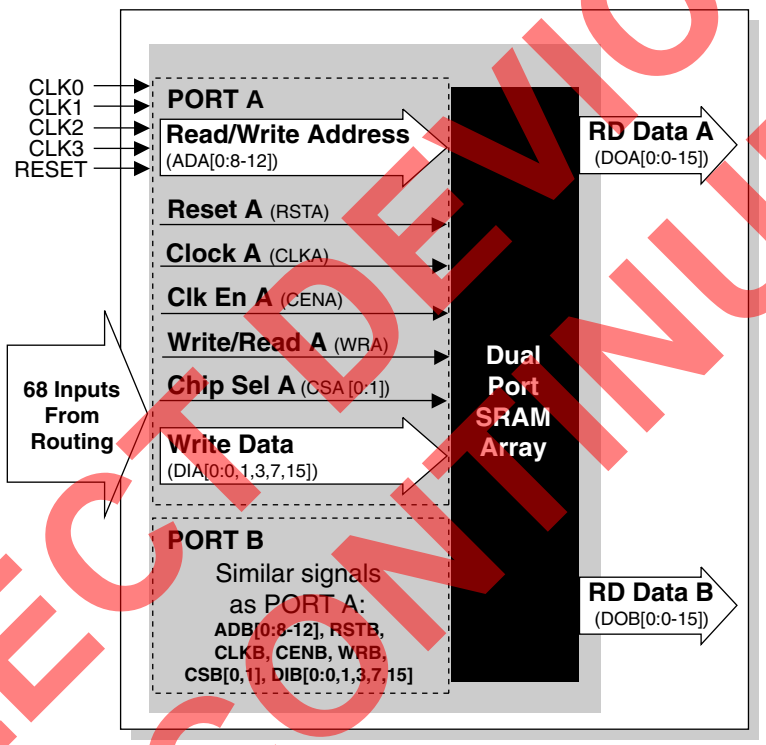


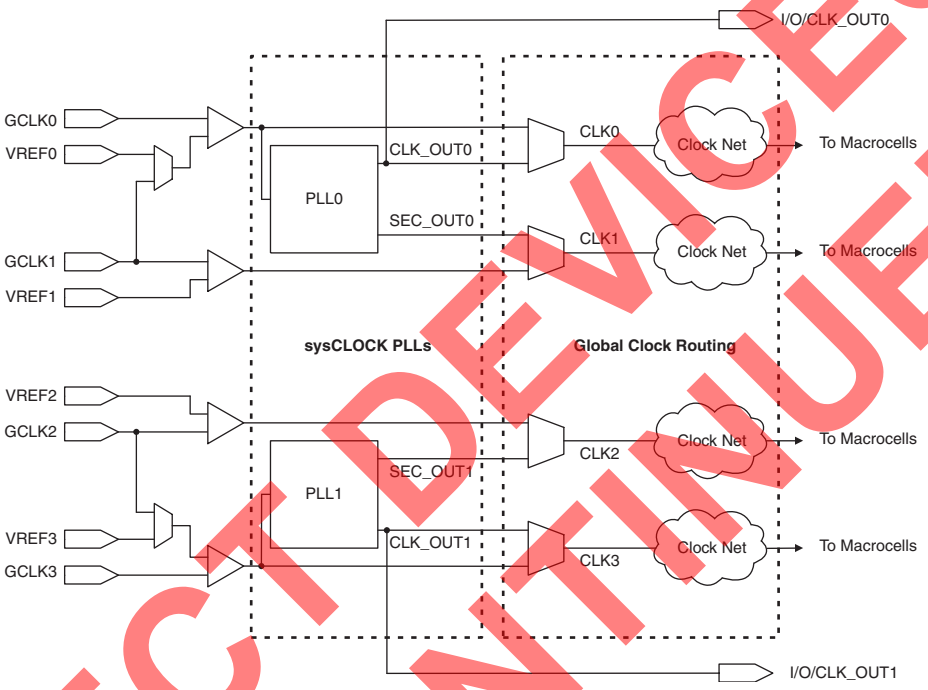

***Table 5. Register Clock, Clock Enable, and Reset in Dual-Port SRAM Mode***

| Register | Input | Source |
|---|---|---|
| Address, Write Data, Read Data, Read/ Write, and Chip Select | Clock | CLKA (CLKB) or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired. |
| | Clock Enable | CENA (CENB) or one of the global clocks (CLK1 - CLK 2). The selected signal can be inverted if required. |
| | Reset | Created by the logical OR of the global reset signal and RSTA (RSTB). RSTA (RSTB) can be inverted is desired. |

## Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

***Figure 14. Clock Distribution Network***




## sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

## Supply Current

| Symbol | Parameter | Condition | Min. | Typ.[3] | Max. | Units |
|---|---|---|---|---|---|---|
| **ispXPLD 5256** | | | | | | |
| $I_{CC}$[1,2] | Operating Power Supply Current | $V_{CC}$ = 3.3V, f = 1.0MHz | — | 26 | — | mA |
| | | $V_{CC}$ = 2.5V, f = 1.0MHz | — | 26 | — | mA |
| | | $V_{CC}$ = 1.8V, f = 1.0MHz | — | 16 | — | mA |
| $I_{CCO}$ | Standby Power Supply Current (per I/O Bank) | $V_{CCO}$ = 3.3V, f = 1.0MHz, unloaded | — | 4 | — | mA |
| | | $V_{CCO}$ = 2.5V, f = 1.0MHz, unloaded | — | 4 | — | mA |
| | | $V_{CCO}$ = 1.8V, f = 1.0MHz, unloaded | — | 3 | — | mA |
| $I_{CCP}$ | PLL Power Supply Current (per PLL Bank) | $V_{CCP}$ = 3.3V, f = 10MHz | — | 11 | — | mA |
| | | $V_{CCP}$ = 2.5V, f = 10MHz | — | 11 | — | mA |
| | | $V_{CCP}$ = 1.8V, f = 10MHz | — | 3 | — | mA |
| $I_{CCJ}$ | Standby IEEE 1149.1 TAP Power Supply Current | $V_{CCJ}$ = 3.3V | — | 1 | — | mA |
| | | $V_{CCJ}$ = 2.5V | — | 1 | — | mA |
| | | $V_{CCJ}$ = 1.8V | — | 1 | — | mA |
| **ispXPLD 5512** | | | | | | |
| $I_{CC}$[1,2] | Operating Power Supply Current | $V_{CC}$ = 3.3V, f = 1.0MHz | — | 33 | — | mA |
| | | $V_{CC}$ = 2.5V, f = 1.0MHz | — | 33 | — | mA |
| | | $V_{CC}$ = 1.8V, f = 1.0MHz | — | 22 | — | mA |
| $I_{CCO}$ | Standby Power Supply Current (per I/O Bank) | $V_{CCO}$ = 3.3V, f = 1.0MHz, unloaded | — | 4 | — | mA |
| | | $V_{CCO}$ = 2.5V, f = 1.0MHz, unloaded | — | 4 | — | mA |
| | | $V_{CCO}$ = 1.8V, f = 1.0MHz, unloaded | — | 3 | — | mA |
| $I_{CCP}$ | PLL Power Supply Current (per PLL Bank) | $V_{CCP}$ = 3.3V, f = 10MHz | — | 11 | — | mA |
| | | $V_{CCP}$ = 2.5V, f = 10MHz | — | 11 | — | mA |
| | | $V_{CCP}$ = 1.8V, f = 10MHz | — | 3 | — | mA |
| $I_{CCJ}$ | Standby IEEE 1149.1 TAP Power Supply Current | $V_{CCJ}$ = 3.3V | — | 1 | — | mA |
| | | $V_{CCJ}$ = 2.5V | — | 1 | — | mA |
| | | $V_{CCJ}$ = 1.8V | — | 1 | — | mA |
| **ispXPLD 5768** | | | | | | |
| $I_{CC}$[1,2] | Operating Power Supply Current | $V_{CC}$ = 3.3V, f = 1.0MHz | — | 40 | — | mA |
| | | $V_{CC}$ = 2.5V, f = 1.0MHz | — | 40 | — | mA |
| | | $V_{CC}$ = 1.8V, f = 1.0MHz | — | 30 | — | mA |
| $I_{CCO}$ | Standby Power Supply Current (per I/O Bank) | $V_{CCO}$ = 3.3V, f = 1.0MHz, unloaded | — | 4 | — | mA |
| | | $V_{CCO}$ = 2.5V, f = 1.0MHz, unloaded | — | 4 | — | mA |
| | | $V_{CCO}$ = 1.8V, f = 1.0MHz, unloaded | — | 3 | — | mA |
| $I_{CCP}$ | PLL Power Supply Current (per PLL Bank) | $V_{CCP}$ = 3.3V, f = 10MHz | — | 11 | — | mA |
| | | $V_{CCP}$ = 2.5V, f = 10MHz | — | 11 | — | mA |
| | | $V_{CCP}$ = 1.8V, f = 10MHz | — | 3 | — | mA |
| $I_{CCJ}$ | Standby IEEE 1149.1 TAP Power Supply Current | $V_{CCJ}$ = 3.3V | — | 1 | — | mA |
| | | $V_{CCJ}$ = 2.5V | — | 1 | — | mA |
| | | $V_{CCJ}$ = 1.8V | — | 1 | — | mA |

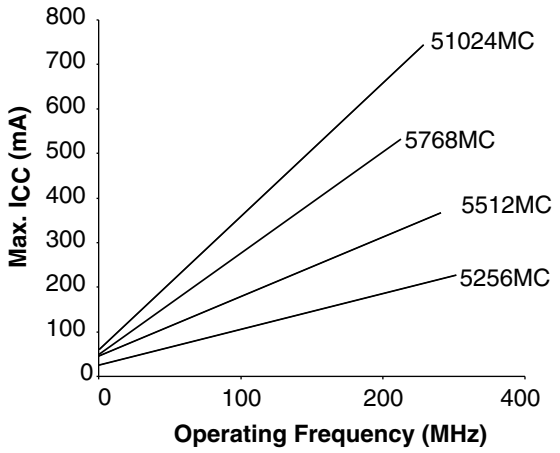
## ispXPLD 5000MX Family Timing Adders (Continued)

| Parameter | Description | Base Param. | -4 | | -45 | | -5 | | -52 | | -75 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| HSTL_I_out | Using HSTL 2.5V, Class I | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| HSTL_III_out | Using HSTL 2.5V, Class III | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| HSTL_IV_out | Using HSTL 2.5V, Class IV | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| LVDS_out | Using Low Voltage Differential Signaling (LVDS) | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | — | 0.8 | ns |
| LVPECL_out | Using Low Voltage PECL | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | ns |
| PCI_out | Using PCI Standard | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | ns |
| SSTL2_I_out | Using SSTL 2.5V, Class I | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | — | 0.3 | ns |
| SSTL2_II_out | Using SSTL 2.5V, Class II | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |
| SSTL3_I_out | Using SSTL 3.3V, Class I | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.2 | — | 0.2 | — | 0.2 | — | 0.2 | — | 0.2 | ns |
| SSTL3_II_out | Using SSTL 3.3V, Class II | $t_{IOBUF}$, $t_{IOEN}$, $t_{IODIS}$ | — | 0.4 | — | 0.4 | — | 0.4 | — | 0.4 | — | 0.4 | ns |

Timing v.1.8

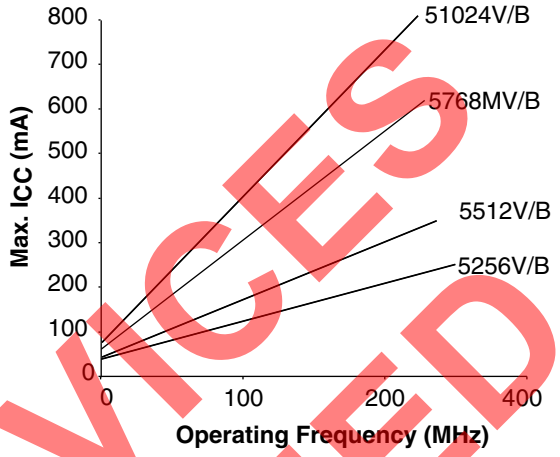
# Power Consumption

**ispXPLD 5000MC Typical $I_{CC}$ vs. Frequency**




Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

**ispXPLD 5000MV/B Typical $I_{CC}$ vs. Frequency**




Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

## Power Estimation Coefficients

| Device | K0 | K1 | K2 | K3 | K4 | K5 | K6 | K7 | DC | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | ispXPLD 5000MC | ispXPLD 5000MV/B |
| ispXPLD 5256 | 2.2 | 8.4 | 7 | 12 | 100 | 0.1379 | 0.0433 | 6.476 | 16 | 24 |
| ispXPLD 5512 | 2.2 | 8.4 | 9.4 | 18 | 151 | 0.1379 | 0.0433 | 6.476 | 17 | 25 |
| ispXPLD 5768 | 2.2 | 8.4 | 10.2 | 21 | 170 | 0.1379 | 0.0433 | 6.476 | 27 | 36 |
| ispXPLD 51024 | 2.2 | 8.4 | 13 | 27.6 | 200 | 0.1379 | 0.0433 | 6.476 | 35 | 43 |

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

## Memory Coefficients

| Device | K8 | K9 | K10 | K11 |
|---|---|---|---|---|
| ispXPLD 5256 | 0.004719 | 0.0924 | 4.4 | 2.9 |
| ispXPLD 5512 | 0.004719 | 0.0924 | 4.4 | 2.9 |
| ispXPLD 5768 | 0.004719 | 0.0924 | 4.4 | 2.9 |
| ispXPLD 51024 | 0.004719 | 0.0924 | 4.4 | 2.9 |

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

## Power Estimation Equations

**ICC = ICC_DC + IMFB_CPLD + IMFB_ SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL_D**

**ICC_DC**
Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) from the data sheet.

**IMFB_CPLD**
= ((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** * CPLD GRP from IFB) * AF+ **K4**) * FREQ / 1000µA/mA

**IMFB_CAM**
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

**IMFB_ SRAM/PDPRAM/FIFO**
= (WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (**K1** + 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * SRAM/PDPRAM/FIFO Memory MFBs * FREQ / 1000µA/mA

**IMFB_ DPRAM**
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs * FREQ / 1000µA/mA

**IPLL_D**
= **K5** * PLL_FREQ * number of PLLs used. IPPL_D is the PLL digital component of the VCC supply current.

Analog portion of PLL supply current consumption, from PLL power pin:

**IPLL_A** = (**K6** * PLL_FREQ + **K7**) * number of PLLs used

Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

## ispXPLD 5000MX Power Supply and NC Connections[1]

## ispXPLD 5512MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Input | 208 PQFP Pin Number | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | | |
| 0 | 96N | M12 | M23 | O23 | M13 | 196 | B5 | A10 |
| 0 | 96P | M10 | M22 | O22 | M11 | 197 | A3 | A9 |
| 0 | 97N | M8 | M21 | O21 | M9 | 198 | B4 | C9 |
| 0 | 97P | M6 | M20 | O20 | M7 | 199 | B3 | D9 |
| 0 | 98N | M5 | M19 | O19 | — | 200 | C5 | F9 |
| 0 | 98P | M4 | M18 | O18 | — | 201 | C6 | E9 |
| 0 | 99N | M2 | M1 | O1 | M3 | 202 | D5 | A8 |
| — | — | $V_{CCO0}$ | — | — | — | — | $V_{CCO0}$ | $V_{CCO0}$ |
| 0 | 99P | M0 | M0 | O0 | M1 | 203 | D6 | B8 |
| — | — | GND (Bank 0) | — | — | — | — | GND (Bank 0) | GND (Bank 0) |
| 0 | 100N | N30 | O29 | — | N31 | — | — | A7 |
| 0 | 100P | N28 | O28 | — | N29 | — | — | B7 |
| 0 | 101N | N26 | O27 | — | N27 | — | — | A5 |
| 0 | 101P | N24 | O26 | — | N25 | — | — | B5 |
| 0 | 102N | N22 | O25 | — | N23 | — | — | B6 |
| 0 | 102P | N21 | O24 | — | — | — | — | C7 |
| 0 | 103N | N20 | O23 | — | — | — | — | E8 |
| 0 | 103P | N18 | O22 | — | N19 | — | — | E7 |
| 0 | 104N | N16 | O21 | — | N17 | — | — | E6 |
| 0 | 104P | N14 | O20 | — | N15 | — | — | D6 |
| 0 | 105N | N12 | O19 | — | N13 | — | — | D8 |
| — | — | $V_{CCO0}$ | — | — | — | 204 | $V_{CCO0}$ | $V_{CCO0}$ |
| 0 | 105P | N10 | O18 | — | N11 | — | — | F8 |
| — | — | GND (Bank 0) | — | — | — | 205 | GND (Bank 0) | GND (Bank 0) |
| 0 | 106N | N8 | O17 | — | N9 | — | — | F7 |
| 0 | 106P | N6 | O16 | — | N7 | — | — | D7 |
| 0 | 107N | N5 | O15 | — | — | 206 | A2 | C6 |
| 0 | 107P | N4 | O14 | — | — | 207 | B2 | C5 |
| 0 | 108N | N2 | O13 | — | N3 | — | — | C4 |
| 0 | 108P | N0 | O12 | — | N1 | — | — | D5 |

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

## ispXPLD 5768MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Inputs | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| - | - | TCK | - | - | - | J6 | T1 |
| - | - | TDO | - | - | - | K2 | V1 |
| 1 | 0P | A30/DATA0 | C0 | A0 | A31 | K3 | W1 |
| 1 | 0N | A28/DATA1 | C1 | A1 | A29 | J3 | Y1 |
| 1 | 1P | A26/DATA2 | C2 | A2 | A27 | J5 | P3 |
| 1 | 1N | A24/DATA3 | C3 | A3 | A25 | J4 | R3 |
| 1 | 2P | A22/DATA4 | C4 | A4 | A23 | L2 | T2 |
| 1 | 2N | A20/DATA5 | C5 | A5 | A21 | M1 | U2 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 3P | A18/DATA6 | C6 | A6 | A19 | K4 | V2 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 3N | A16/DATA7 | C7 | A7 | A17 | L3 | W2 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 4P | A14/INITB | C8 | A8 | A15 | K5 | R4 |
| 1 | 4N | A12/CSB | C9 | A9 | A13 | L5 | T4 |
| 1 | 5P | A10/READ | C10 | A10 | A11 | N1 | R6 |
| 1 | 5N | A8/CCLK | C11 | A11 | A9 | M2 | R5 |
| 1 | 6P | A6 | - | - | A7 | — | U3 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 6N | A4 | - | - | A5 | P1 | V3 |
| 1 | 7P | A2 | - | - | A3 | M3 | Y2 |
| 1 | 7N | A0 | - | - | A1 | L4 | W3 |
| 1 | 8P | B30 | D0 | - | B31 | N2 | U5 |
| 1 | 8N | B28 | D2 | - | B29 | P2 | T5 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 9P | B26 | D4 | - | B27 | R1 | U4 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 9N | B24 | D6 | - | B25 | R2 | V4 |
| 1 | 10P | B22 | D8 | - | B23 | T2 | AA3 |
| 1 | 10N | B20 | D10 | - | B21 | T3 | AB3 |
| 1 | - | B18 | D12 | - | B19 | — | Y4 |
| - | - | DONE | - | - | - | M4 | AA4 |
| 1 | 11P | B14 | - | - | B15 | — | AB2 |
| 1 | 11N | B12 | - | - | B13 | — | U6 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 12P | B10 | - | - | B11 | — | V5 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 12N | B8 | - | - | B9 | — | W6 |
| 1 | 13P | B6 | C12 | A12 | B7 | N3 | AB4 |
| 1 | 13N | B4 | C13 | A13 | B5 | P4 | AB5 |
| 1 | 14P | B2 | C14 | A14 | B3 | N5 | T6 |
| 1 | 14N | B0 | C15 | A15 | B1 | M6 | U7 |
| - | - | PROGRAMB | - | - | - | R3 | W5 |

## ispXPLD 5768MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Inputs | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| 1 | - | C28 | D14 | - | C29 | P5 | U8 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 15P | C26 | D16 | - | C27 | T4 | V6 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 15N | C24 | D18 | - | C25 | T5 | V7 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 16P | C22 | D20 | - | C23 | R4 | Y5 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 16N | C20 | D22 | - | C21 | N6 | AA5 |
| 1 | 17P | C18 | - | - | C19 | R5 | Y6 |
| 1 | 17N | C16 | - | - | C17 | P6 | Y7 |
| 1 | 18P | C14 | - | - | C15 | — | AA6 |
| 1 | 18N | C12 | - | - | C13 | — | AA7 |
| 1 | 19P | C10 | - | - | C11 | — | W7 |
| 1 | 19N | C8 | - | - | C9 | M7 | V8 |
| 1 | 20P | C6 | - | - | C7 | T6 | W8 |
| 1 | 20N | C4 | - | - | C5 | R6 | U9 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| - | - | CFG0 | - | - | - | L8 | U10 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 21P | C0 | C16 | A16 | C1 | T7 | AB7 |
| 1 | 21N | D30 | C17 | A17 | D31 | R7 | AA8 |
| 1 | 22P | D28 | C18 | A18 | D29 | N7 | AB8 |
| 1 | 22N | D26 | C19 | A19 | D27 | P7 | AB9 |
| 1 | 23P | D24 | C20 | A20 | D25 | T8 | W9 |
| 1 | 23N | D22 | C21 | A21 | D23 | R8 | Y9 |
| 1 | 24P | D20 | C22 | A22 | D21 | M8 | AB10 |
| 1 | 24N | D18 | C23 | A23 | D19 | P8 | AA10 |
| 1 | - | D16/VREF1 | - | - | D17 | L9 | W10 |
| 1 | 25P | D14 | C24 | A24 | D15 | N8 | Y10 |
| 1 | 25N | D12 | C25 | A25 | D13 | M9 | Y11 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 26P | D10 | C26 | A26 | D11 | N10 | V9 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 26N | D8 | C27 | A27 | D9 | T9 | V10 |
| 1 | 27P | D6 | C28 | A28 | D7 | T10 | AA11 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 27N | D4 | C29 | A29 | D5 | R9 | AB11 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 28P | D2 | C30 | A30 | D3 | P9 | U11 |
| 1 | 28N | D0 | C31 | A31 | D1 | N9 | V11 |
| 2 | 29P | E0 | F0 | H0 | E1 | T11 | AB12 |
| - | - | VCC | - | - | - | VCC | VCC |

## ispXPLD 5768MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/ Function | Alternate Outputs | | Alternate Inputs | 256 fpBGA Ball Number | 484 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| 2 | 46N | G6 | H19 | - | G7 | — | AB19 |
| 2 | 47P | G8 | H20 | - | G9 | — | AA19 |
| - | - | VCCO2 | - | - | - | VCCO2 | VCCO2 |
| 2 | 47N | G10 | H21 | - | G11 | — | U17 |
| - | - | GND (Bank 2) | - | - | - | GND (Bank 2) | GND (Bank 2) |
| 2 | 48P | G12 | H22 | - | G13 | — | V18 |
| 2 | 48N | G14 | H23 | - | G15 | — | AB21 |
| 2 | 49P | G16 | H24 | - | G17 | — | U18 |
| 2 | 49N | G18 | H25 | - | G19 | — | T17 |
| 2 | 50P | G20 | H26 | - | G21 | R16 | AB20 |
| 2 | 50N | G22 | H27 | - | G23 | P16 | AA20 |
| 2 | 51P | G24 | H28 | - | G25 | N15 | Y19 |
| - | - | VCCO2 | - | - | - | VCCO2 | VCCO2 |
| 2 | 51N | G26 | H29 | - | G27 | N14 | V19 |
| - | - | GND (Bank 2) | - | - | - | GND (Bank 2) | GND (Bank 2) |
| 2 | 52P | G28 | F16 | H16 | G29 | N16 | T18 |
| 2 | 52N | G30 | F17 | H17 | G31 | M16 | R17 |
| 2 | 53P | H0 | F18 | H18 | H1 | M14 | U19 |
| 2 | 53N | H2 | F19 | H19 | H3 | M15 | T19 |
| 2 | 54P | H4 | H30 | E24 | H5 | — | V20 |
| - | - | VCC | - | - | - | VCC | VCC |
| 2 | 54N | H6 | H31 | E26 | H7 | — | U20 |
| 2 | 55P | H8 | F20 | H20 | H9 | L13 | W20 |
| 2 | 55N | H10 | F21 | H21 | H11 | L12 | Y21 |
| 2 | 56P | H12 | F22 | H22 | H13 | L15 | R18 |
| 2 | 56N | H14 | F23 | H23 | H15 | L16 | R19 |
| - | - | GND | - | - | - | GND | GND |
| 2 | 57P | H16 | F24 | H24 | H17 | L14 | W21 |
| - | - | VCCO2 | - | - | - | VCCO2 | VCCO2 |
| 2 | 57N | H18 | F25 | H25 | H19 | K15 | Y22 |
| - | - | GND (Bank 2) | - | - | - | GND (Bank 2) | GND (Bank 2) |
| 2 | 58P | H20 | F26 | H26 | H21 | K14 | R20 |
| 2 | 58N | H22 | F27 | H27 | H23 | K12 | P20 |
| 2 | 59P | H24 | F28 | H28 | H25 | K13 | T21 |
| 2 | 59N | H26 | F29 | H29 | H27 | J13 | R21 |
| 2 | 60P | H28 | F30 | H30 | H29 | J14 | U21 |
| 2 | 60N | H30 | F31 | H31 | H31 | J12 | V21 |
| - | - | TOE | - | - | - | J15 | W22 |
| - | - | RESET | - | - | - | J11 | V22 |
| - | - | GOE0 | - | - | - | H11 | T22 |
| - | - | GOE1 | - | - | - | H13 | R22 |
| - | - | GNDP | - | - | - | See Power Supply and NC Connections Table | |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| 1 | 15N | C0 | A31 | C31 | C1 | — | W5 |
| 1 | 16P | E30/DATA0 | G0 | E0 | E31 | W1 | W1 |
| 1 | 16N | E28/DATA1 | G1 | E1 | E29 | Y1 | Y1 |
| 1 | 17P | E26/DATA2 | G2 | E2 | E27 | P3 | V6 |
| 1 | 17N | E24/DATA3 | G3 | E3 | E25 | R3 | W6 |
| 1 | 18P | E22/DATA4 | G4 | E4 | E23 | T2 | Y2 |
| 1 | 18N | E20/DATA5 | G5 | E5 | E21 | U2 | Y3 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 19P | E18/DATA6 | G6 | E6 | E19 | V2 | Y4 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 19N | E16/DATA7 | G7 | E7 | E17 | W2 | Y5 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 20P | E14/INITB | G8 | E8 | E15 | R4 | V7 |
| 1 | 20N | E12/CSB | G9 | E9 | E13 | T4 | W7 |
| 1 | 21P | E10/READ | G10 | E10 | E11 | R6 | AA1 |
| 1 | 21N | E8/CCLK | G11 | E11 | E9 | R5 | AA2 |
| 1 | 22P | E6 | - | - | E7 | U3 | AA3 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 22N | E4 | - | - | E5 | V3 | AA4 |
| 1 | 23P | E2 | - | - | E3 | Y2 | Y6 |
| 1 | 23N | E0 | - | - | E1 | W3 | AA5 |
| 1 | 24P | F30 | H0 | - | F31 | U5 | AB2 |
| 1 | 24N | F28 | H2 | - | F29 | T5 | AB3 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 25P | F26 | H4 | | F27 | U4 | AB4 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 25N | F24 | H6 | - | F25 | V4 | AB5 |
| 1 | 26P | F22 | H8 | - | F23 | AA3 | AB1 |
| 1 | 26N | F20 | H10 | - | F21 | AB3 | AC2 |
| 1 | - | F18 | H12 | - | F19 | Y4 | AC3 |
| - | - | DONE | - | - | - | AA4 | AC4 |
| 1 | 27P | F14 | - | - | F15 | AB2 | AC1 |
| 1 | 27N | F12 | - | - | F13 | U6 | AD1 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 28P | F10 | | | F11 | V5 | AD2 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 28N | F8 | | | F9 | W6 | AD3 |
| 1 | 29P | F6 | G12 | E12 | F7 | AB4 | Y8 |
| 1 | 29N | F4 | G13 | E13 | F5 | AB5 | Y9 |
| 1 | 30P | F2 | G14 | E14 | F3 | T6 | AA8 |
| 1 | 30N | F0 | G15 | E15 | F1 | U7 | AA9 |
| - | - | PROGRAMB | - | - | - | W5 | AB8 |
| 1 | - | G28 | H14 | - | G29 | U8 | AB9 |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 31P | G26 | H16 | - | G27 | V6 | AB7 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 31N | G24 | H18 | - | G25 | V7 | AC7 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 32P | G22 | H20 | - | G23 | Y5 | AB6 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 32N | G20 | H22 | - | G21 | AA5 | AC6 |
| 1 | 33P | G18 | - | - | G19 | Y6 | AC8 |
| 1 | 33N | G16 | - | - | G17 | Y7 | AC9 |
| 1 | 34P | G14 | - | - | G15 | AA6 | AC5 |
| 1 | 34N | G12 | - | - | G13 | AA7 | AD4 |
| 1 | 35P | G10 | - | - | G11 | W7 | AD5 |
| 1 | 35N | G8 | - | - | G9 | V8 | AD6 |
| 1 | 36P | G6 | - | - | G7 | W8 | AD7 |
| 1 | 36N | G4 | - | - | G5 | U9 | AD8 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| - | - | CFG0 | - | - | - | U10 | AE3 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 37P | G0 | G16 | E16 | G1 | AB7 | AD9 |
| 1 | 37N | H30 | G17 | E17 | H31 | AA8 | AD10 |
| 1 | 38P | H28 | G18 | E18 | H29 | AB8 | AE4 |
| 1 | 38N | H26 | G19 | E19 | H27 | AB9 | AE5 |
| 1 | 39P | H24 | G20 | E20 | H25 | W9 | AE6 |
| 1 | 39N | H22 | G21 | E21 | H23 | Y9 | AE7 |
| 1 | 40P | H20 | G22 | E22 | H21 | AB10 | AE8 |
| 1 | 40N | H18 | G23 | E23 | H19 | AA10 | AE9 |
| 1 | - | H16/VREF1 | - | - | H17 | W10 | AE10 |
| 1 | 41P | H14 | G24 | E24 | H15 | Y10 | AF3 |
| 1 | 41N | H12 | G25 | E25 | H13 | Y11 | AF4 |
| - | - | GND (Bank 1) | - | - | - | GND (Bank 1) | GND (Bank 1) |
| 1 | 42P | H10 | G26 | E26 | H11 | V9 | AF5 |
| - | - | VCCO1 | - | - | - | VCCO1 | VCCO1 |
| 1 | 42N | H8 | G27 | E27 | H9 | V10 | AF6 |
| 1 | 43P | H6 | G28 | E28 | H7 | AA11 | AF7 |
| - | - | GND | - | - | - | GND | GND |
| 1 | 43N | H4 | G29 | E29 | H5 | AB11 | AF8 |
| - | - | VCC | - | - | - | VCC | VCC |
| 1 | 44P | H2 | G30 | E30 | H3 | U11 | AF9 |
| 1 | 44N | H0 | G31 | E31 | H1 | V11 | AF10 |
| 2 | 45P | I0 | J0 | L0 | I1 | AB12 | AF17 |
| - | - | VCC | - | - | - | VCC | VCC |
| 2 | 45N | I2 | J1 | L1 | I3 | AA12 | AF18 |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| - | GCLK3P | GCLK3 | - | - | - | N16 | N24 |
| 3 | 93N | R0 | T31 | R31 | R1 | J22 | N23 |
| 3 | 93P | R2 | T30 | R30 | R3 | H22 | N22 |
| 3 | 94N | R4 | T29 | R29 | R5 | N19 | M26 |
| 3 | 94P | R6 | T28 | R28 | R7 | P15 | M25 |
| 3 | 95N | R8 | T27 | R27 | R9 | P21 | M23 |
| 3 | 95P | R10 | T26 | R26 | R11 | N15 | M22 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 96N | R12 | T25 | R25 | R13 | M15 | N20 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 96P | R14 | T24 | R24 | R15 | N20 | M20 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 97N | R16 | T23 | R23 | R17 | P22 | N21 |
| 3 | 97P | R18 | T22 | R22 | R19 | N21 | M21 |
| 3 | 98N | R20 | T21 | R21 | R21 | N17 | M24 |
| 3 | 98P | R22 | T20 | R20 | R23 | M20 | L24 |
| 3 | 99N | R24 | T19 | R19 | R25 | P17 | L23 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 99P | R26 | T18 | R18 | R27 | P18 | L22 |
| 3 | 100N | R28 | T17 | R17 | R29 | M21 | L25 |
| 3 | 100P | R30 | T16 | R16 | R31 | M17 | K26 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 101N | T0 | T15 | R15 | T1 | L20 | K25 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 101P | T2 | T14 | R14 | T3 | N18 | K24 |
| 3 | 102N | T4 | T13 | R13 | T5 | L21 | K23 |
| 3 | 102P | T6 | T12 | R12 | T7 | M18 | K22 |
| 3 | 103N | T8 | T11 | R11 | T9 | L22 | J25 |
| 3 | 103P | T10 | T10 | R10 | T11 | L17 | J24 |
| 3 | 104N | T12 | T9 | R9 | T13 | K22 | L21 |
| 3 | 104P | T14 | T8 | R8 | T15 | L18 | K21 |
| 3 | 105N | T16 | T7 | R7 | T17 | K21 | L20 |
| 3 | 105P | T18 | T6 | R6 | T19 | K18 | K20 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 106N | T20 | T5 | R5 | T21 | K20 | J23 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 106P | T22 | T4 | R4 | T23 | K17 | J22 |
| 3 | 107N | T24 | T3 | R3 | T25 | K19 | J26 |
| 3 | 107P | T26 | T2 | R2 | T27 | J17 | H26 |
| 3 | 108N | T28 | T1 | R1 | T29 | E22 | H25 |
| 3 | 108P | T30/PLL_FBK1 | T0 | R0 | T31 | E21 | H24 |
| 3 | 109N | U0/PLL_RST1 | X27 | V27 | U1 | G22 | H23 |
| 3 | 109P | U2 | X26 | V26 | U3 | F21 | H22 |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 110N | U4 | X25 | V25 | U5 | H21 | J21 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 110P | U6 | X24 | V24 | U7 | G21 | H21 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 111N | U8 | X23 | V23 | U9 | D22 | G25 |
| 3 | 111P | U10 | X22 | V22 | U11 | D21 | G24 |
| 3 | 112N | U12 | X21 | V21 | U13 | J20 | G23 |
| 3 | 112P | U14/CLK_OUT1 | X20 | V20 | U15 | J19 | G22 |
| 3 | 113N | U16 | V31 | - | U17 | E20 | J20 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 113P | U18 | V30 | U30 | U19 | F20 | H20 |
| 3 | 114N | U20 | V29 | U28 | U21 | H17 | G26 |
| 3 | 114P | U22 | V28 | U26 | U23 | H18 | F25 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 115N | U24 | V27 | - | U25 | J18 | F24 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 115P | U26 | V26 | - | U27 | H19 | F23 |
| 3 | 116N | U28 | V25 | - | U29 | G20 | G21 |
| 3 | 116P | U30 | V24 | - | U31 | G19 | F22 |
| - | - | GND | - | - | - | GND | GND |
| 3 | 117N | V0 | V23 | - | V1 | C22 | F26 |
| - | - | VCC | - | - | - | VCC | VCC |
| 3 | 117P | V2 | V22 | - | V3 | C21 | E26 |
| 3 | 118N | V4 | V21 | - | V5 | D20 | E25 |
| 3 | 118P | V6 | V20 | - | V7 | C19 | E24 |
| 3 | 119N | V8 | V19 | - | V9 | F19 | E23 |
| 3 | 119P | V10 | V18 | - | V11 | E19 | E22 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |
| 3 | 120N | V12 | V17 | - | V13 | G18 | D26 |
| - | - | VCCO3 | - | - | - | VCCO3 | VCCO3 |
| 3 | 120P | V14 | V16 | - | V15 | F18 | D25 |
| 3 | 121N | V16 | V15 | - | V17 | B20 | D24 |
| 3 | 121P | V18 | V14 | - | V19 | B19 | D23 |
| 3 | 122N | V20 | V13 | - | V21 | A20 | C26 |
| 3 | 122P | V22 | V12 | - | V23 | A19 | C25 |
| 3 | 123N | V24 | X19 | V19 | V25 | D18 | G19 |
| 3 | 123P | V26 | X18 | V18 | V27 | C18 | F19 |
| 3 | 124N | V28 | X17 | V17 | V29 | G17 | G18 |
| 3 | 124P | V30 | X16 | V16 | V31 | F16 | F18 |
| 3 | 125N | W0 | X31 | V31 | W1 | E17 | F20 |
| 3 | 125P | W2 | X30 | V30 | W3 | D17 | E20 |
| - | - | GND (Bank 3) | - | - | - | GND (Bank 3) | GND (Bank 3) |

## ispXPLD 51024MX Logic Signal Connections (Continued)

| sysIO Bank | LVDS Pair | Primary Macrocell/Function | Alternate Outputs | | Alternate Input | 484 fpBGA Ball Number | 672 fpBGA Ball Number |
|---|---|---|---|---|---|---|---|
| | | | Macrocell 1 | Macrocell 2 | | | |
| 0 | 142N | Y26 | Y29 | AA29 | Y27 | B11 | A10 |
| 0 | 142P | Y24 | Y28 | AA28 | Y25 | A11 | A9 |
| 0 | 143N | Y22 | Y27 | AA27 | Y23 | F11 | A8 |
| - | - | VCCO0 | - | - | - | VCCO0 | VCCO0 |
| 0 | 143P | Y20 | Y26 | AA26 | Y21 | F10 | A7 |
| - | - | GND (Bank 0) | - | - | - | GND (Bank 0) | GND (Bank 0) |
| 0 | 144N | Y18 | Y25 | AA25 | Y19 | E10 | A6 |
| 0 | 144P | Y16 | Y24 | AA24 | Y17 | C10 | A5 |
| 0 | 145N | Y14/VREF0 | Y3 | AA3 | Y15 | D10 | A4 |
| 0 | 145P | Y12 | Y2 | AA2 | Y13 | B10 | A3 |
| 0 | 146N | Y10 | Y23 | AA23 | Y11 | A10 | B10 |
| 0 | 146P | Y8 | Y22 | AA22 | Y9 | A9 | B9 |
| 0 | 147N | Y6 | Y21 | AA21 | Y7 | C9 | B8 |
| 0 | 147P | Y4 | Y20 | AA20 | Y5 | D9 | B7 |
| 0 | 148N | Y2 | Y19 | AA19 | Y3 | F9 | B6 |
| 0 | 148P | Y0 | Y18 | AA18 | Y1 | E9 | B5 |
| 0 | 149N | Z30 | Y1 | AA1 | Z31 | A8 | B4 |
| - | - | VCCO0 | - | - | - | VCCO0 | VCCO0 |
| 0 | 149P | Z28 | Y0 | AA0 | Z29 | B8 | B3 |
| - | - | GND (Bank 0) | - | - | - | GND (Bank 0) | GND (Bank 0) |
| 0 | 150N | Z26 | AA29 | - | Z27 | A7 | C10 |
| 0 | 150P | Z24 | AA28 | - | Z25 | B7 | C9 |
| 0 | 151N | Z22 | AA27 | - | Z23 | A5 | C8 |
| 0 | 151P | Z20 | AA26 | - | Z21 | B5 | C7 |
| 0 | 152N | Z18 | AA25 | - | Z19 | B6 | C6 |
| 0 | 152P | Z16 | AA24 | - | Z17 | C7 | C5 |
| 0 | 153N | Z14 | AA23 | - | Z15 | E8 | C4 |
| 0 | 153P | Z12 | AA22 | - | Z13 | E7 | D5 |
| 0 | 154N | Z10 | AA21 | - | Z11 | E6 | D9 |
| - | - | VCC | - | - | - | VCC | VCC |
| 0 | 154P | Z8 | AA20 | - | Z9 | D6 | D8 |
| - | - | GND | - | - | - | GND | GND |
| 0 | 155N | Z6 | AA19 | - | Z7 | D8 | D7 |
| - | - | VCCO0 | - | - | - | VCCO0 | VCCO0 |
| 0 | 155P | Z4 | AA18 | - | Z5 | F8 | D6 |
| - | - | GND (Bank 0) | - | - | - | GND (Bank 0) | GND (Bank 0) |
| 0 | 156N | Z2 | AA17 | - | Z3 | F7 | F9 |
| 0 | 156P | Z0 | AA16 | - | Z1 | D7 | E9 |
| 0 | 157N | AA30 | AA15 | - | AA31 | C6 | F7 |
| 0 | 157P | AA28 | AA14 | - | AA29 | C5 | F8 |
| 0 | 158N | AA26 | AA13 | - | AA27 | C4 | G8 |
| 0 | 158P | AA24 | AA12 | - | AA25 | D5 | G9 |

### ispXPLD 5000MB (2.5V) Industrial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MB | LC5256MB-5F256I | 256 | 2.5 | 5.0 | fpBGA | 256 | 141 | I |
| | LC5256MB-75F256I | 256 | 2.5 | 7.5 | fpBGA | 256 | 141 | I |
| LC5512MB | LC5512MB-75Q208I | 512 | 2.5 | 7.5 | PQFP | 208 | 149 | I |
| | LC5512MB-75F256I | 512 | 2.5 | 7.5 | fpBGA | 256 | 193 | I |
| | LC5512MB-75F484I | 512 | 2.5 | 7.5 | fpBGA | 484 | 253 | I |
| LC5768MB | LC5768MB-75F256I | 768 | 2.5 | 7.5 | fpBGA | 256 | 193 | I |
| | LC5768MB-75F484I | 768 | 2.5 | 7.5 | fpBGA | 484 | 317 | I |
| LC51024MB | LC51024MB-75F484I | 1024 | 2.5 | 7.5 | fpBGA | 484 | 317 | I |
| | LC51024MB-75F672I | 1024 | 2.5 | 7.5 | fpBGA | 672 | 381 | I |

### ispXPLD 5000MV (3.3V) Commercial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MV | LC5256MV-4F256C | 256 | 3.3 | 4.0 | fpBGA | 256 | 141 | C |
| | LC5256MV-5F256C | 256 | 3.3 | 5.0 | fpBGA | 256 | 141 | C |
| | LC5256MV-75F256C | 256 | 3.3 | 7.5 | fpBGA | 256 | 141 | C |
| LC5512MV | LC5512MV-45Q208C | 512 | 3.3 | 4.5 | PQFP | 208 | 149 | C |
| | LC5512MV-75Q208C | 512 | 3.3 | 7.5 | PQFP | 208 | 149 | C |
| | LC5512MV-45F256C | 512 | 3.3 | 4.5 | fpBGA | 256 | 193 | C |
| | LC5512MV-75F256C | 512 | 3.3 | 7.5 | fpBGA | 256 | 193 | C |
| | LC5512MV-45F484C | 512 | 3.3 | 4.5 | fpBGA | 484 | 253 | C |
| | LC5512MV-75F484C | 512 | 3.3 | 7.5 | fpBGA | 484 | 253 | C |
| LC5768MV | LC5768MV-5F256C | 768 | 3.3 | 5.0 | fpBGA | 256 | 193 | C |
| | LC5768MV-75F256C | 768 | 3.3 | 7.5 | fpBGA | 256 | 193 | C |
| | LC5768MV-5F484C | 768 | 3.3 | 5.0 | fpBGA | 484 | 317 | C |
| | LC5768MV-75F484C | 768 | 3.3 | 7.5 | fpBGA | 484 | 317 | C |
| LC51024MV | LC51024MV-52F484C | 1024 | 3.3 | 5.2 | fpBGA | 484 | 317 | C |
| | LC51024MV-75F484C | 1024 | 3.3 | 7.5 | fpBGA | 484 | 317 | C |
| | LC51024MV-52F672C | 1024 | 3.3 | 5.2 | fpBGA | 672 | 381 | C |
| | LC51024MV-75F672C | 1024 | 3.3 | 7.5 | fpBGA | 672 | 381 | C |

### ispXPLD 5000MV (3.3V) Industrial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MV | LC5256MV-5F256I | 256 | 3.3 | 5.0 | fpBGA | 256 | 141 | I |
| | LC5256MV-75F256I | 256 | 3.3 | 7.5 | fpBGA | 256 | 141 | I |
| LC5512MV | LC5512MV-75Q208I | 512 | 3.3 | 7.5 | PQFP | 208 | 149 | I |
| | LC5512MV-75F256I | 512 | 3.3 | 7.5 | fpBGA | 256 | 193 | I |
| | LC5512MV-75F484I | 512 | 3.3 | 7.5 | fpBGA | 484 | 253 | I |
| LC5768MV | LC5768MV-75F256I | 768 | 3.3 | 7.5 | fpBGA | 256 | 193 | I |
| | LC5768MV-75F484I | 768 | 3.3 | 7.5 | fpBGA | 484 | 317 | I |
| LC51024MV | LC51024MV-75F484I | 1024 | 3.3 | 7.5 | fpBGA | 484 | 317 | I |
| | LC51024MV-75F672I | 1024 | 3.3 | 7.5 | fpBGA | 672 | 381 | I |

## Lead-Free Packaging

### ispXPLD 5000MC (1.8V) Lead-Free Commercial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MC | LC5256MC-4FN256C | 256 | 1.8 | 4.0 | Lead-free fpBGA | 256 | 141 | C |
| | LC5256MC-5FN256C | 256 | 1.8 | 5.0 | Lead-free fpBGA | 256 | 141 | C |
| | LC5256MC-75FN256C | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 141 | C |
| LC5512MC | LC5512MC-45QN208C | 512 | 1.8 | 4.5 | Lead-free PQFP | 208 | 149 | C |
| | LC5512MC-75QN208C | 512 | 1.8 | 7.5 | Lead-free PQFP | 208 | 149 | C |
| | LC5512MC-45FN256C | 512 | 1.8 | 4.5 | Lead-free fpBGA | 256 | 193 | C |
| | LC5512MC-75FN256C | 512 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 193 | C |
| | LC5512MC-45FN484C | 512 | 1.8 | 4.5 | Lead-free fpBGA | 484 | 253 | C |
| | LC5512MC-75FN484C | 512 | 1.8 | 7.5 | Lead-free fpBGA | 484 | 253 | C |
| LC5768MC | LC5768MC-5FN256C | 768 | 1.8 | 5.0 | Lead-free fpBGA | 256 | 193 | C |
| | LC5768MC-75FN256C | 768 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 193 | C |
| | LC5768MC-5FN484C | 768 | 1.8 | 5.0 | Lead-free fpBGA | 484 | 317 | C |
| | LC5768MC-75FN484C | 768 | 1.8 | 7.5 | Lead-free fpBGA | 484 | 317 | C |
| LC51024MC | LC51024MC-52FN484C | 1024 | 1.8 | 5.2 | Lead-free fpBGA | 484 | 317 | C |
| | LC51024MC-75FN484C | 1024 | 1.8 | 7.5 | Lead-free fpBGA | 484 | 317 | C |
| | LC51024MC-52FN672C | 1024 | 1.8 | 5.2 | Lead-free fpBGA | 672 | 381 | C |
| | LC51024MC-75FN672C | 1024 | 1.8 | 7.5 | Lead-free fpBGA | 672 | 381 | C |

### ispXPLD 5000MC (1.8V) Lead-Free Industrial Devices

| Device | Part Number | Macrocells | Voltage (V) | $t_{PD}$ (ns) | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC5256MC | LC5256MC-5FN256I | 256 | 1.8 | 5.0 | Lead-free fpBGA | 256 | 141 | I |
| | LC5256MC-75FN256I | 256 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 141 | I |
| LC5512MC | LC5512MC-75QN208I | 512 | 1.8 | 7.5 | Lead-free PQFP | 208 | 149 | I |
| | LC5512MC-75FN256I | 512 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 193 | I |
| | LC5512MC-75FN484I | 512 | 1.8 | 7.5 | Lead-free fpBGA | 484 | 253 | I |
| LC5768MC | LC5768MC-75FN256I | 768 | 1.8 | 7.5 | Lead-free fpBGA | 256 | 193 | I |
| | LC5768MC-75FN484I | 768 | 1.8 | 7.5 | Lead-free fpBGA | 484 | 317 | I |
| LC51024MC | LC51024MC-75FN484I | 1024 | 1.8 | 7.5 | Lead-free fpBGA | 484 | 317 | I |
| | LC51024MC-75FN672I | 1024 | 1.8 | 7.5 | Lead-free fpBGA | 672 | 381 | I |

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| — | — | Previous Lattice releases. |
| December 2003 | 07 | Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers). |
| | | Updated ispXPLD 5000MX timing numbers (version v.1.7). |
| | | Added lead-free package designator. |
| | | Removed ispXPLD 5000MC industrial temperature grade ordering part numbers. |
| January 2004 | 08 | Lead-free package release for the ispXPLD 5000MC and 5000MV devices. |
| | | Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers). |
| March 2004 | 08.1 | Updated the MFB Cascade Chain table for the ispXPLD 5256MX device. |
| May 2004 | 09 | Updated the ispXPLD 5000MX timig numbers (version v.1.8)<br>ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release |
| | | Updated typical supply current data and condition. |
| | | ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14. |
| August 2004 | 10 | Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ. |
| | | Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free). |
| October 2004 | 10.1 | Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer) |
| November 2004 | 11 | Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers. |
| December 2004 | 11.1 | Pin name RESETB has been updated to RESET. |
| March 2005 | 12 | 208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices. |
| April 2005 | 12.1 | Page 23, clarification of footnote regarding IDK specification. |
| March 2006 | 12.2 | Signal description for RESET has been updated. |
| April 2009 | 12.3 | Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format. |
| February 2010 | 12.4 | References to "system gates" changed to "functional gates." |