Lattice Semiconductor Corporation - LC5512MC-75FN484C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	253
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mc-75fn484c

Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width support.

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	H -> G -> F -> E
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

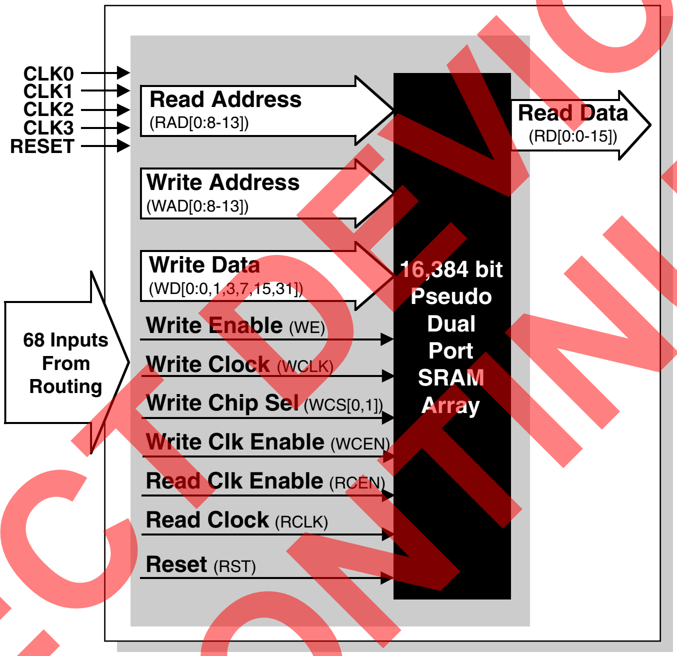


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

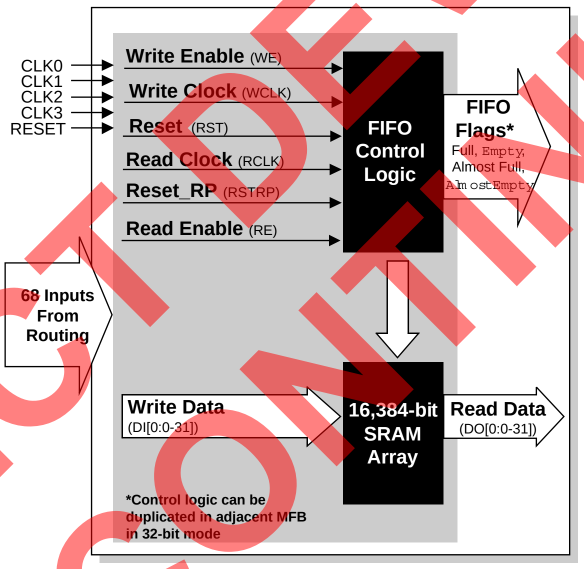


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Figure 17. I/O Cell

Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 12 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}. For more information on the sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to TN1000 – sysIO Usage Guidelines for Lattice Devices.

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. The JTAG TAP pins support only LVCMOS 3.3, 2.5 and 1.8V standards. The voltage is controlled by V_{CCJ}. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

Absolute Maximum Ratings[1, 2, 3]

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IHMAX} +2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95	V
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7	V
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6	V
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95	V
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7	V
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6	V
T_J	Junction Temperature (Commercial Operation)	0	90	C
	Junction Temperature (Industrial Operation)	-40	105	C

E^2CMOS Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	0 ð V_{IN} ð 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO}þð 1.0V. For V_{CCO} > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO})þð 3.6V.
2. 0 ð V_{CC} ð V_{CC} (MAX), 0 ð V_{CCO} ð V_{CCO} (MAX)
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.
4. LVTTL, LVCMOS only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCO} - 0.2V)$	—	—	10	µA
		$(V_{CCO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40	µA
I_{IH}[4]	Input High Leakage Current	$3.6V < V_{IN} \le 5.5V$ and $3.0V \le V_{CCO} \le 3.6V$	—	—	3	mA
I_{PU}[3]	I/O Active Pullup Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	-30	—	-150	µA
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{CCO} * 0.35	—	V_{CCO} * 0.65	µA
C1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz
3. I_{PU} on JTAG pins has a maximum of -175µA for 5512MX devices.
4. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \le V_{CCO} \le 3.6V$. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	"Don't Care" Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	"Don't Care" Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

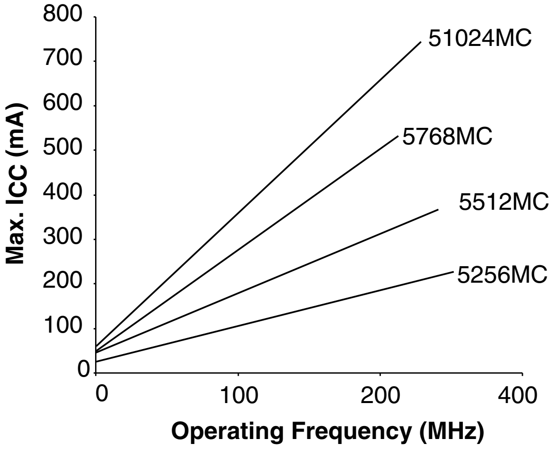
ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{SPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{SPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	9.86	ns
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns
Pseudo Dual Port RAM													
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCES}$	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{PDPRCEH}$	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPWCES}$	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43	—	ns
$t_{PDPWCEH}$	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPRADDS}$	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPRADDH}$	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPWADDS}$	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPWADDH}$	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{PDPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns

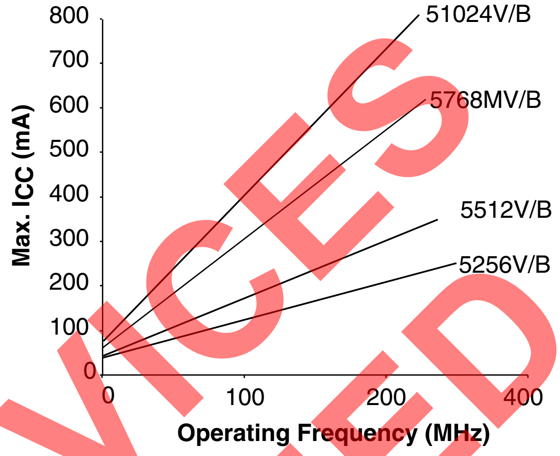
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the IEEE 1149.1 state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data out.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the registers in the device. The global polarity for this pin is selectable on a global basis.þ The default is active low. An external pull-down is required when polarity is set to active high.
yzz	Input/Output – These are the general purpose I/O used by the logic array. *y* is the MFB reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs (see Figure 14 for differential pairing).
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GNDP	GND – Ground for PLLs.
V_{CCP}	V_{CC} – The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG interface.
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2CMOS or IEEE 1149.1 TAP.
PROGRAMB	Input – Controls the programming of SRAM. Hold high for normal operation. Toggle low to reload SRAM from E^2 memory.
CCLK[1]	Input – Clock for sysCONFIG interface. Reads and writes occur on the rising edge of the clock.
READ[1]	Input – Drive high to perform reads from the sysCONFIG interface.
INITB	I/O – Indicates status of configuration. Can be driven low to inhibit configuration.
DONE	Output (open drain) – Indicates status of configuration.

[1] These inputs should not toggle during power up for proper power-up configuration.

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	51N	F2	E1	F1	F3	B8
3	51P	F0	E0	F0	F1	C8
0	52N	G30	G31	H31	G31	B7
0	52P	G28	G30	H30	G29	A7
-	-	GND	-	-	-	NC
0	53N	G26	G29	H29	G27	D7
0	53P	G24	G28	H28	G25	C7
0	54N	G22	G27	H27	G23	B6
-	-	VCCO0	-	-	-	VCCO0
0	54P	G21	G26	H26	-	E7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	55N	G20	G25	H25	-	E6
0	55P	G18	G24	H24	G19	A6
0	56N	G16/VREF0	G3	H3	G17	A5
0	56P	G14	G2	H2	G15	A4
0	57N	G12	G23	H23	G13	B5
0	57P	G10	G22	H22	G11	A3
0	58N	G8	G21	H21	G9	B4
0	58P	G6	G20	H20	G7	B3
0	59N	G5	G19	H19	-	C5
0	59P	G4	G18	H18	-	C6
0	60N	G2	G1	H1	G3	D5
0	60P	G0	G0	H0	G1	D6
-	-	VCCO0	-	-	-	VCCO0
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	V19
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	—	—	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	—	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

ispXPLD 51024MX Logic Signal Connections

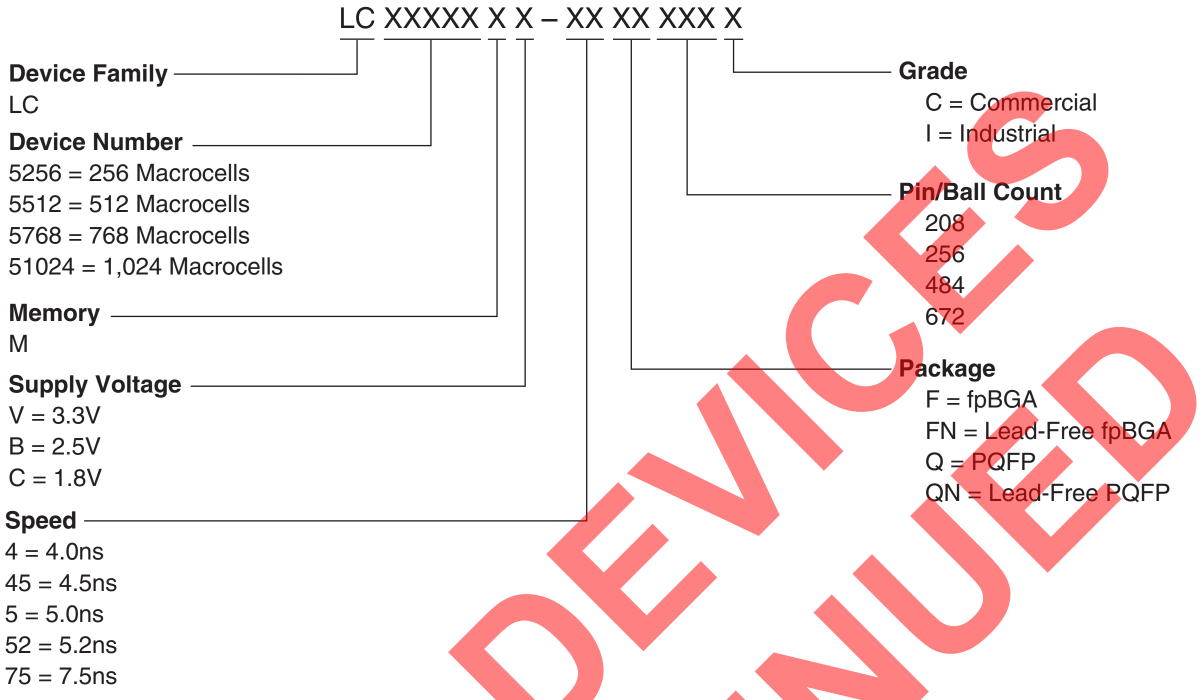
sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	159N	AA22	AA11	AB18	AA23	B4	C2
0	159P	AA20	AA10	AB16	AA21	A4	C1
0	160N	AA18	Y17	AA17	AA19	B3	D4
0	160P	AA16	Y16	AA16	AA17	A3	D3
0	161N	AA14	Y15	AA15	AA15	F5	D2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	161P	AA12	Y14	AA14	AA13	G6	D1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	162N	AA10	Y13	AA13	AA11	H6	E5
0	162P	AA8	Y12	AA12	AA9	G5	E4
0	163N	AA6	AA9	AB14	AA7	D3	E3
0	163P	AA4	AA8	AB12	AA5	D2	E2
0	164N	AA2	AA7	AB10	AA3	E4	E1
-	-	VCC	-	-	-	VCC	VCC
0	164P	AA0	AA6	AB8	AA1	E3	F2
-	-	GND	-	-	-	GND	GND
0	165N	AB30	AA5	AB6	AB31	F4	F5
0	165P	AB28	AA4	AB4	AB29	G4	G6
0	166N	AB26	AA3	AB2	AB27	C2	F4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	166P	AB24	AA2	AB0	AB25	C1	F3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	167N	AB22	AA1	-	AB23	F3	F1
0	167P	AB20	AA0	-	AB21	G3	G1
0	168N	AB18	AA31	-	AB19	H4	G5
-	-	VCC	-	-		VCC	VCC
0	168P	AB16	AA30	-	AB17	J4	G4
0	169N	AB14	Y11	AA11	AB15	H5	H7
0	169P	AB12/CLK_OUT0	Y10	AA10	AB13	J5	J7
0	170N	AB10	Y9	AA9	AB11	E2	G3
0	170P	AB8	Y8	AA8	AB9	F2	G2
-	-	GND	-	-	-	GND	GND
0	171N	AB6	Y7	AA7	AB7	D1	H6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	171P	AB4	Y6	AA6	AB5	E1	J6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	172N	AB2	Y5	AA5	AB3	J3	H5
0	172P	AB0/PLL_RST0	Y4	AA4	AB1	H2	H4
0	173N	AC30	AC31	AE31	AC31	G2	H3
0	173P	AC28/PLL_FBK0	AC30	AE30	AC29	G1	H2
0	174N	AC26	AC29	AE29	AC27	J6	H1
0	174P	AC24	AC28	AE28	AC25	K4	J1

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	15N	C0	A31	C31	C1	—	W5
1	16P	E30/DATA0	G0	E0	E31	W1	W1
1	16N	E28/DATA1	G1	E1	E29	Y1	Y1
1	17P	E26/DATA2	G2	E2	E27	P3	V6
1	17N	E24/DATA3	G3	E3	E25	R3	W6
1	18P	E22/DATA4	G4	E4	E23	T2	Y2
1	18N	E20/DATA5	G5	E5	E21	U2	Y3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	19P	E18/DATA6	G6	E6	E19	V2	Y4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	19N	E16/DATA7	G7	E7	E17	W2	Y5
-	-	GND	-	-	-	GND	GND
1	20P	E14/INITB	G8	E8	E15	R4	V7
1	20N	E12/CSB	G9	E9	E13	T4	W7
1	21P	E10/READ	G10	E10	E11	R6	AA1
1	21N	E8/CCLK	G11	E11	E9	R5	AA2
1	22P	E6	-	-	E7	U3	AA3
-	-	VCC	-	-	-	VCC	VCC
1	22N	E4	-	-	E5	V3	AA4
1	23P	E2	-	-	E3	Y2	Y6
1	23N	E0	-	-	E1	W3	AA5
1	24P	F30	H0	-	F31	U5	AB2
1	24N	F28	H2	-	F29	T5	AB3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	25P	F26	H4		F27	U4	AB4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	25N	F24	H6	-	F25	V4	AB5
1	26P	F22	H8	-	F23	AA3	AB1
1	26N	F20	H10	-	F21	AB3	AC2
1	-	F18	H12	-	F19	Y4	AC3
-	-	DONE	-	-	-	AA4	AC4
1	27P	F14	-	-	F15	AB2	AC1
1	27N	F12	-	-	F13	U6	AD1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	28P	F10			F11	V5	AD2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	28N	F8			F9	W6	AD3
1	29P	F6	G12	E12	F7	AB4	Y8
1	29N	F4	G13	E13	F5	AB5	Y9
1	30P	F2	G14	E14	F3	T6	AA8
1	30N	F0	G15	E15	F1	U7	AA9
-	-	PROGRAMB	-	-	-	W5	AB8
1	-	G28	H14	-	G29	U8	AB9

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

Part Number Description


LC XXXXX X X – XX XX XXX X

Device Family
LC

Device Number
5256 = 256 Macrocells
5512 = 512 Macrocells
5768 = 768 Macrocells
51024 = 1,024 Macrocells

Memory
M

Supply Voltage
V = 3.3V
B = 2.5V
C = 1.8V

Speed
4 = 4.0ns
45 = 4.5ns
5 = 5.0ns
52 = 5.2ns
75 = 7.5ns

Grade
C = Commercial
I = Industrial

Pin/Ball Count
208
256
484
672

Package
F = fpBGA
FN = Lead-Free fpBGA
Q = PQFP
QN = Lead-Free PQFP

Ordering Information

Note: For voltage families offered in industrial temperature grades and for all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -45XXXXC is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only. In addition, the fastest commercial speed grade (-5) for the LC5768MB/MV devices, at Lattice's discretion, will utilize either a commercial grade only single-mark or a dual-mark format in conjunction with the slower industrial speed grade (-75).

Conventional Packaging

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	141	C
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	141	C
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	141	C
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	149	C
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	149	C
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	193	C
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	193	C
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	253	C
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	253	C

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193	I
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193	C
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193	C
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317	C
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193	I
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
December 2003	07	Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers).
		Updated ispXPLD 5000MX timing numbers (version v.1.7).
		Added lead-free package designator.
		Removed ispXPLD 5000MC industrial temperature grade ordering part numbers.
January 2004	08	Lead-free package release for the ispXPLD 5000MC and 5000MV devices.
		Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers).
March 2004	08.1	Updated the MFB Cascade Chain table for the ispXPLD 5256MX device.
May 2004	09	Updated the ispXPLD 5000MX timig numbers (version v.1.8) ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release
		Updated typical supply current data and condition.
		ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14.
August 2004	10	Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ.
		Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free).
October 2004	10.1	Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer)
November 2004	11	Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers.
December 2004	11.1	Pin name RESETB has been updated to RESET.
March 2005	12	208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices.
April 2005	12.1	Page 23, clarification of footnote regarding IDK specification.
March 2006	12.2	Signal description for RESET has been updated.
April 2009	12.3	Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format.
February 2010	12.4	References to "system gates" changed to "functional gates."