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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.65V ~ 1.95V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	149
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mc-75qn208i

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor style interface (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more information on the sysCONFIG capability, refer to TN1026, ispXP Configuration Usage Guidelines.

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For information on estimating power consumption, refer to TN1031 Power Estimation in ispXPLD 5000MX Devices.

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family External Switching Characteristics [1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Output Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX} [4]	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
f_{MAX} (Ext.)	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
f_{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
f_{MAX} (CAMC) [5]	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
f_{MAX} (CAM) [5]	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family External Switching Characteristics (Continued)[1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (RAM)[5]	Clock Frequency to RAM in:											
	Single Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Dual Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—	106	MHz
f_{MAX} (FIFO)[5]	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—	132	MHz
t_{PWR_ON}	Power-on Time	—	200	—	200	—	200	—	200	—	200	µs

Timing v.1.8

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—	1.33	ns
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—	0.66	ns
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—	0.19	ns
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—	4.91	ns
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	2.89	—	3.21	—	3.34	—	4.82	ns
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—	1.50	ns
Optional Adjusters													
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—	0.07	ns
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—	0.99	ns
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—	0.94	ns
$t_{PLL_SEC_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—	0.91	ns
t_{INEXP}	MFB Input Extender	t_{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—	1.16	ns
Input and Output Buffer Delays													
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables										ns
t_{IOO}	Output Buffer Selection Adder	t_{BUF}											ns
FIFO													
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—	4.00	ns
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	“Don’t Care” Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	“Don’t Care” Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CAMWMSKS}$	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t_{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t_{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

SELECT DEVICES DISCONTINUED

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Power Supply and NC Connections[1]

SELECT DEVICES DISCONTINUED

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
1	4N	A16/CSB	A9	B9	A17	L5
1	5P	A18/READ	A10	B10	A19	N1
1	5N	A20/CCLK	A11	B11	A21	M2
-	-	VCC	-	-	-	VCC
-	-	DONE	-	-	-	M4
1	6P	A22	A12	B12	A23	N3
1	6N	A24	A13	B13	A25	P4
1	7P	A26	A14	B14	A27	N5
1	7N	A28	A15	B15	A29	M6
-	-	PROGRAMB	-	-	-	R3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
-	-	VCCO1	-	-	-	VCC01
-	-	CFG0	-	-	-	L8
1	8P	B2	A16	B16	B3	T7
1	8N	B4	A17	B17	-	R7
1	9P	B5	A18	B18	-	N7
1	9N	B6	A19	B19	B7	P7
1	10P	B8	A20	B20	B9	T8
1	10N	B10	A21	B21	B11	R8
1	11P	B12	A22	B22	B13	M8
1	11N	B14	A23	B23	B15	P8
1	-	B16/VREF1	-	-	B17	L9
1	12P	B18	A24	B24	B19	N8
1	12N	B20	A25	B25	-	M9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	13P	B21	A26	B26	-	N10
-	-	VCCO1	-	-	-	VCCO1
1	13N	B22	A27	B27	B23	T9
1	14P	B24	A28	B28	B25	T10
1	14N	B26	A29	B29	B27	R9
-	-	VCC	-	-	-	VCC
1	15P	B28	A30	B30	B29	P9
1	15N	B30	A31	B31	B31	N9
2	16P	C0	C0	D0	C1	T11
2	16N	C2	C1	D1	C3	T12
2	17P	C4	C2	D2	-	P10
2	17N	C5	C3	D3	-	R10
2	18P	C6	C4	D4	C7	R11
-	-	VCCO2	-	-	-	VCCO2
2	18N	C8	C5	D5	C9	M10
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	19P	C10	C6	D6	C11	M11
2	19N	C12	C7	D7	C13	T13

SELECT DEVICES DISCONTINUED

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	V19
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	—	—	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	—	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND

SELECT DEVICES DISCONTINUED

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	29N	E2	F1	H1	E3	T12	AA12
-	-	GND	-	-	-	GND	GND
2	30P	E4	F2	H2	E5	P10	Y12
2	30N	E6	F3	H3	E7	R10	AA13
2	31P	E8	F4	H4	E9	R11	V12
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	31N	E10	F5	H5	E11	M10	U12
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	32P	E12	F6	H6	E13	M11	AB13
2	32N	E14	F7	H7	E15	T13	Y13
2	33P	E16	H0	-	E17	P11	V13
2	33N	E18/VREF2	H1	-	E19	T14	W13
2	34P	E20	F8	H8	E21	R12	V14
2	34N	E22	F9	H9	E23	R13	W14
2	35P	E24	F10	H10	E25	N11	Y14
2	35N	E26	F11	H11	E27	T15	AB14
2	36P	E28	F12	H12	E29	R14	AB15
2	36N	E30	F13	H13	E31	N12	AA15
2	37P	F0	F14	H14	F1	P12	U13
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	37N	F2	F15	H15	F3	R15	U14
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	38P	F4	H2	E0	F5	—	W15
2	38N	F6	H3	E2	F7	—	W16
2	39P	F8	H4	E4	F9	—	Y16
2	39N	F10	H5	E6	F11	—	AA16
2	40P	F12	H6	E8	F13	—	AB16
2	40N	F14	H7	E10	F15	—	AA17
2	41P	F16	H8	E12	F17	—	Y17
2	41N	F18	H9	E16	F19	—	AA18
2	42P	F20	H10	E20	F21	—	W17
-	-	VCC	-	-	-	VCC	VCC
2	42N	F22	H11	E22	F23	—	W18
-	-	GND	-	-	-	GND	GND
2	43P	F24	H12	-	F25	—	V15
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	43N	F26	H13	-	F27	—	U15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	44P	F28	H14	-	F29	P13	Y18
2	44N	F30	H15	-	F31	P15	V17
2	45P	G0	H16	-	G1	M13	V16
2	45N	G2	H17	-	G3	P14	U16
2	46P	G4	H18	-	G5	—	AB18

SELECT DEVICES DISCONTINUED

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

SELECT DEVICES DISCONTINUED

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor style interface (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more information on the sysCONFIG capability, refer to TN1026, ispXP Configuration Usage Guidelines.

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For information on estimating power consumption, refer to TN1031 Power Estimation in ispXPLD 5000MX Devices.

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice s ispVM System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings [1, 2, 3]

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IHMAX} +2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95	V
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7	V
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6	V
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95	V
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7	V
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6	V
T_J	Junction Temperature (Commercial Operation)	0	90	C
	Junction Temperature (Industrial Operation)	-40	105	C

E^2CMOS Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle[1]	1,000		Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics [1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	0 ðV $_{IN}$ ð3.0V		+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO} ð1.0V. For V $_{CCO}$ > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and $V_{CCO,}$ provided (V_{IN} - V_{CCO}) ð3.6V.
2. 0 ðV $_{CC}$ ðV $_{CC}$ (MAX), 0 ðV $_{CCO}$ ðV $_{CCO}$ (MAX)
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.
4. LVTTL, LVCMOS only.