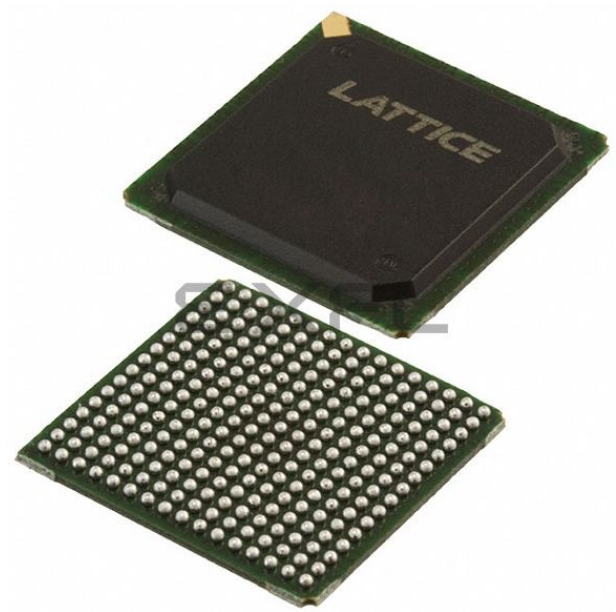
Lattice Semiconductor Corporation - LC5512MV-45FN256C Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	193
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-45fn256c

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram

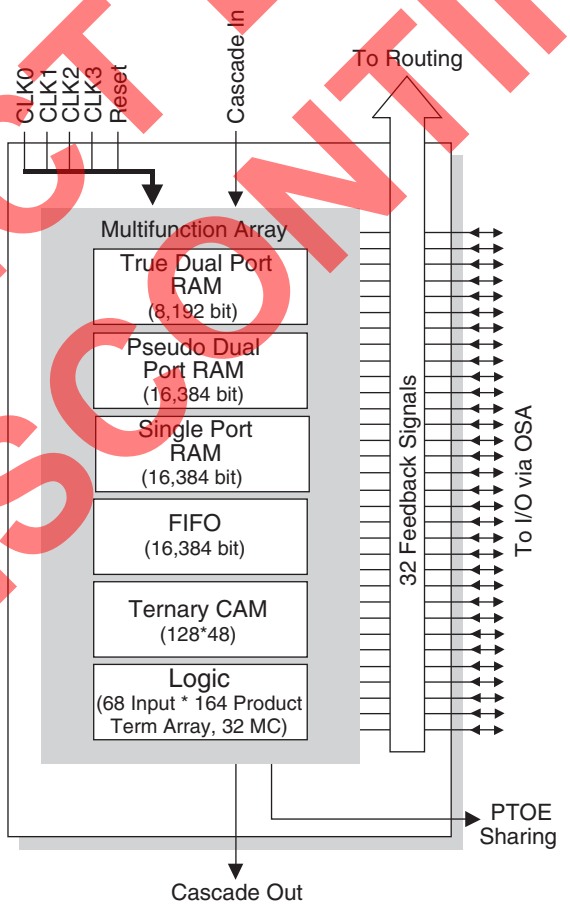
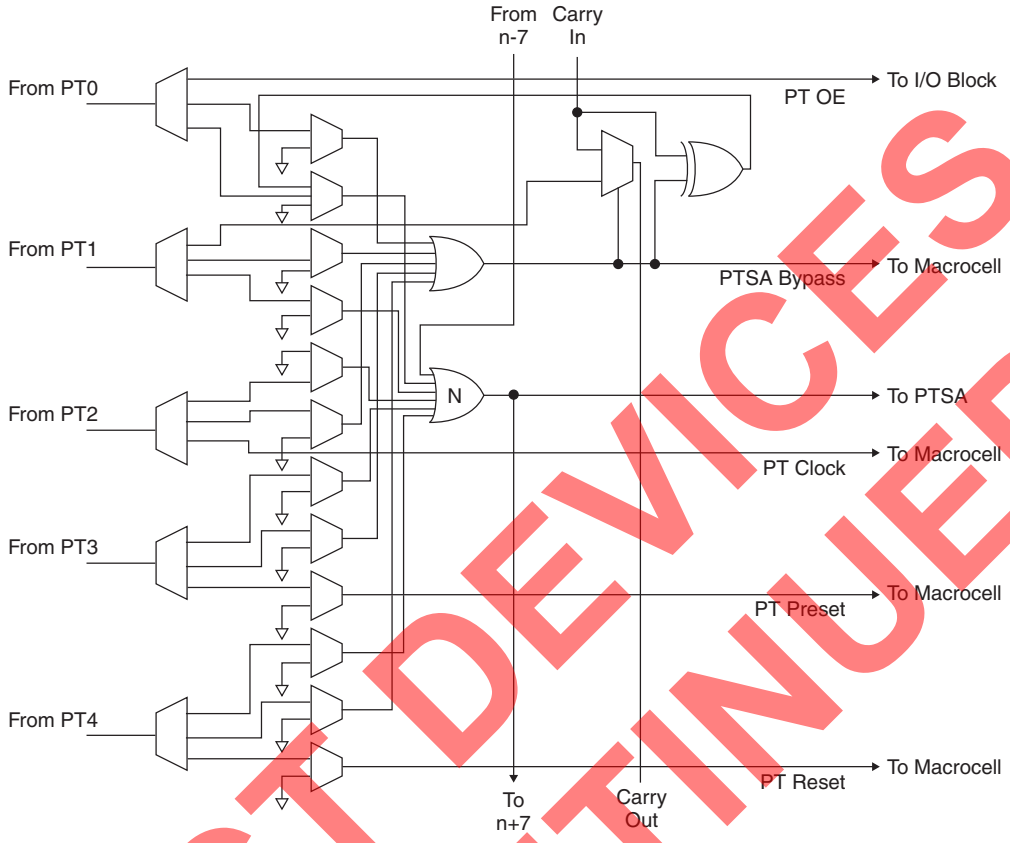


Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

Figure 7. Product Term Sharing Array (PTSA)

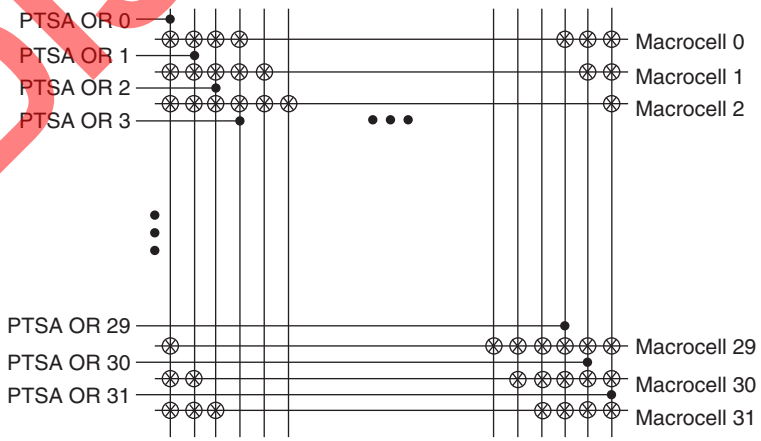


Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size[1]
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output
The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation
In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width
Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching
All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

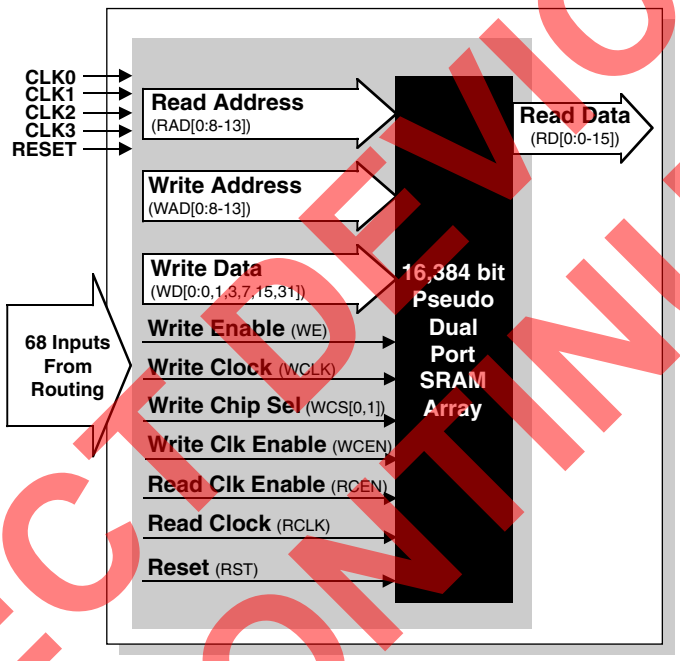


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

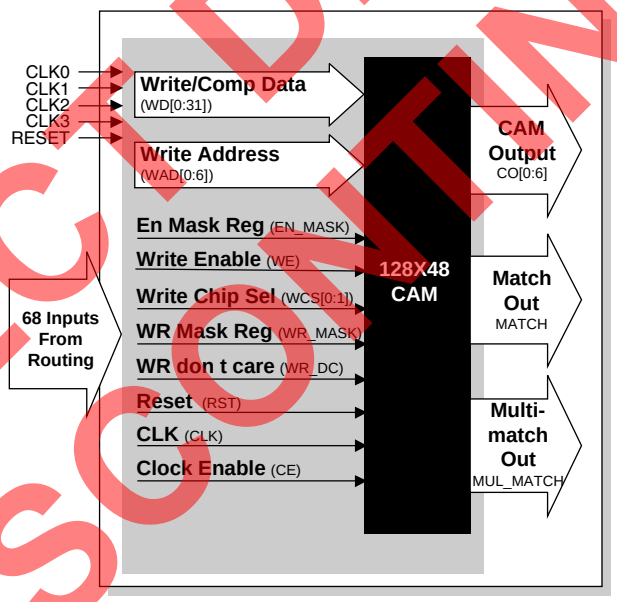


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to TN1000 – sysIO Usage Guidelines for Lattice Devices.

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. The JTAG TAP pins support only LVCMOS 3.3, 2.5 and 1.8V standards. The voltage is controlled by V_{CCJ}. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} and V_{IH} = 0.65 * V_{CC}.
4. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CAMWMSKS}$	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t_{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t_{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{SPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{SPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	9.86	ns
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns
Pseudo Dual Port RAM													
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCES}$	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{PDPRCEH}$	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPWCES}$	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43	—	ns
$t_{PDPWCEH}$	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPRADDS}$	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPRADDH}$	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPWADDS}$	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPWADDH}$	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{PDPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DPCEBS}	Clock Enable B Setup before Clock B Time	—	2.33	—	2.33	—	2.33	—	2.33	—	3.03	—	ns
t_{DPCEBH}	Clock Enable Hold B after Clock B Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDBS}$	Address B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDBH}$	Address B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWBS}	R/W B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWBH}	R/W B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATABS}$	Write Data B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATABH}$	Write Data B Hold after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	5.97	—	5.92	—	5.86	—	5.65	—	9.86	ns
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	5.16	—	5.16	—	5.16	—	5.16	—	6.71	ns
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.40	—	1.40	—	1.83	—	ns
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns

Timing v.1.8

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

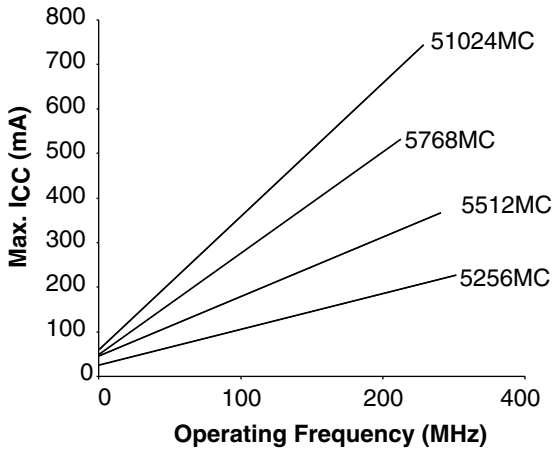
Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

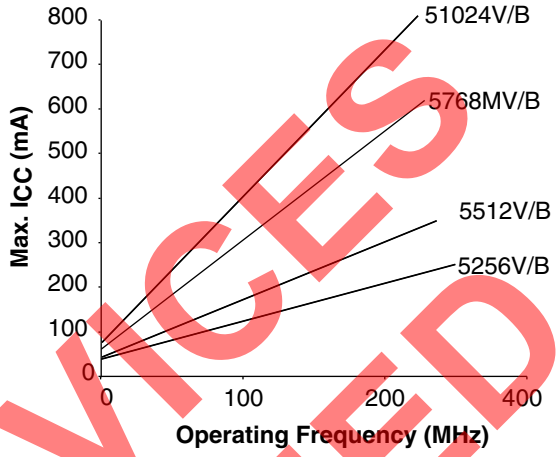
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

ispXPLD 5256MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
0	61N	H30	G17	H17	H31	B1
0	61P	H28	G16	H16	H29	C1
0	62N	H26	G15	H15	H27	D3
0	62P	H24	G14	H14	H25	C2
0	63N	H22	G13	H13	H23	E3
0	63P	H21	G12	H12	-	D2
-	-	VCC	-	-	-	VCC
0	64N	H20	G11	H11	-	E2
0	64P	H18/CLK_OUT0	G10	H10	H19	F2
0	65N	H16	G9	H9	H17	F1
0	65P	H14	G8	H8	H15	G1
-	-	GND	-	-	-	GND
0	66N	H12	G7	H7	H13	F3
-	-	VCCO0	-	-	-	VCCO0
0	66P	H10	G6	H6	H11	G5
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	67N	H8	G5	H5	H9	H5
0	67P	H6/PLL_RST0	G4	H4	H7	G4
0	68N	H5	-	-	-	G3
0	68P	H4/PLL_FBK0	-	-	-	H3
0	69N	H2	-	-	H3	G2
0	69P	H0	-	-	H1	H1
-	GCLK0P	GCLK0	-	-	-	H2
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table
-	GCLK0N	GCLK1	-	-	-	J2
-	-	GND	-	-	-	GND
-	-	TDI	-	-	-	H6
-	-	TMS	-	-	-	H4
-	-	TCK	-	-	-	J6
-	-	TDO	-	-	-	K2
1	0P	A0/DATA0	A0	B0	A1	K3
1	0N	A2/DATA1	A1	B1	A3	J3
1	1P	A4/DATA2	A2	B2	-	J5
1	1N	A5/DATA3	A3	B3	-	J4
1	2P	A6/DATA4	A4	B4	A7	L2
1	2N	A8/DATA5	A5	B5	A9	M1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	3P	A10/DATA6	A6	B6	A11	K4
-	-	VCCO1	-	-	-	VCCO1
1	3N	A12/DATA7	A7	B7	A13	L3
-	-	GND	-	-	-	GND
1	4P	A14/INITB	A8	B8	A15	K5

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	34N	E30	-	-	E31	H14
3	34P	E28	-	-	E29	G16
3	35N	E26	-	-	E27	G15
3	35P	E24/PLL_FBK1	-	-	E25	F15
3	36N	E22/PLL_RST1	E27	F27	E23	H12
3	36P	E21	E26	F26	-	G14
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	37N	E20	E25	F25	-	F16
-	-	VCCO3	-	-	-	VCCO3
3	37P	E18	E24	F24	E19	E16
-	-	GND	-	-	-	GND
3	38N	E16	E23	F23	E17	G13
3	38P	E14	E22	F22	E15	G12
3	39N	E12	E21	F21	E13	F14
3	39P	E10/CLK_OUT1	E20	F20	E11	E15
-	-	VCC	-	-	-	VCC
3	40N	E8	E19	F19	E9	D12
3	40P	E6	E18	F18	E7	B14
3	41N	E5	E17	F17	-	C13
3	41P	E4	E16	F16	-	A14
3	42N	E2	E31	F31	E3	A13
3	42P	E0	E30	F30	E1	B13
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
-	-	VCCO3	-	-	-	VCCO3
3	43N	F30	E15	F15	F31	B11
3	43P	F28	E14	F14	F29	C11
3	44N	F26	E13	F13	F27	B10
3	44P	F24	E12	F12	F25	A10
3	45N	F22	E11	F11	F23	C10
3	45P	F21	E10	F10	-	D10
3	46N	F20	E9	F9	-	C9
3	46P	F18	E8	F8	F19	E9
3	47N	F16/VREF3	E29	F29	F17	D9
3	47P	F14	E28	F28	F15	F9
3	48N	F12	E7	F7	F13	A9
3	48P	F10	E6	F6	F11	F8
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	49N	F8	E5	F5	F9	E8
-	-	VCCO3	-	-	-	VCCO3
3	49P	F6	E4	F4	F7	A8
3	50N	F5	E3	F3	-	B9
3	50P	F4	E2	F2	-	D8
-	-	VCC	-	-	-	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	29N	E2	F1	H1	E3	T12	AA12
-	-	GND	-	-	-	GND	GND
2	30P	E4	F2	H2	E5	P10	Y12
2	30N	E6	F3	H3	E7	R10	AA13
2	31P	E8	F4	H4	E9	R11	V12
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	31N	E10	F5	H5	E11	M10	U12
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	32P	E12	F6	H6	E13	M11	AB13
2	32N	E14	F7	H7	E15	T13	Y13
2	33P	E16	H0	-	E17	P11	V13
2	33N	E18/VREF2	H1	-	E19	T14	W13
2	34P	E20	F8	H8	E21	R12	V14
2	34N	E22	F9	H9	E23	R13	W14
2	35P	E24	F10	H10	E25	N11	Y14
2	35N	E26	F11	H11	E27	T15	AB14
2	36P	E28	F12	H12	E29	R14	AB15
2	36N	E30	F13	H13	E31	N12	AA15
2	37P	F0	F14	H14	F1	P12	U13
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	37N	F2	F15	H15	F3	R15	U14
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	38P	F4	H2	E0	F5	—	W15
2	38N	F6	H3	E2	F7	—	W16
2	39P	F8	H4	E4	F9	—	Y16
2	39N	F10	H5	E6	F11	—	AA16
2	40P	F12	H6	E8	F13	—	AB16
2	40N	F14	H7	E10	F15	—	AA17
2	41P	F16	H8	E12	F17	—	Y17
2	41N	F18	H9	E16	F19	—	AA18
2	42P	F20	H10	E20	F21	—	W17
-	-	VCC	-	-	-	VCC	VCC
2	42N	F22	H11	E22	F23	—	W18
-	-	GND	-	-	-	GND	GND
2	43P	F24	H12	-	F25	—	V15
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	43N	F26	H13	-	F27	—	U15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	44P	F28	H14	-	F29	P13	Y18
2	44N	F30	H15	-	F31	P15	V17
2	45P	G0	H16	-	G1	M13	V16
2	45N	G2	H17	-	G3	P14	U16
2	46P	G4	H18	-	G5	—	AB18

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	15N	C0	A31	C31	C1	—	W5
1	16P	E30/DATA0	G0	E0	E31	W1	W1
1	16N	E28/DATA1	G1	E1	E29	Y1	Y1
1	17P	E26/DATA2	G2	E2	E27	P3	V6
1	17N	E24/DATA3	G3	E3	E25	R3	W6
1	18P	E22/DATA4	G4	E4	E23	T2	Y2
1	18N	E20/DATA5	G5	E5	E21	U2	Y3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	19P	E18/DATA6	G6	E6	E19	V2	Y4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	19N	E16/DATA7	G7	E7	E17	W2	Y5
-	-	GND	-	-	-	GND	GND
1	20P	E14/INITB	G8	E8	E15	R4	V7
1	20N	E12/CSB	G9	E9	E13	T4	W7
1	21P	E10/READ	G10	E10	E11	R6	AA1
1	21N	E8/CCLK	G11	E11	E9	R5	AA2
1	22P	E6	-	-	E7	U3	AA3
-	-	VCC	-	-	-	VCC	VCC
1	22N	E4	-	-	E5	V3	AA4
1	23P	E2	-	-	E3	Y2	Y6
1	23N	E0	-	-	E1	W3	AA5
1	24P	F30	H0	-	F31	U5	AB2
1	24N	F28	H2	-	F29	T5	AB3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	25P	F26	H4		F27	U4	AB4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	25N	F24	H6	-	F25	V4	AB5
1	26P	F22	H8	-	F23	AA3	AB1
1	26N	F20	H10	-	F21	AB3	AC2
1	-	F18	H12	-	F19	Y4	AC3
-	-	DONE	-	-	-	AA4	AC4
1	27P	F14	-	-	F15	AB2	AC1
1	27N	F12	-	-	F13	U6	AD1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	28P	F10			F11	V5	AD2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	28N	F8			F9	W6	AD3
1	29P	F6	G12	E12	F7	AB4	Y8
1	29N	F4	G13	E13	F5	AB5	Y9
1	30P	F2	G14	E14	F3	T6	AA8
1	30N	F0	G15	E15	F1	U7	AA9
-	-	PROGRAMB	-	-	-	W5	AB8
1	-	G28	H14	-	G29	U8	AB9

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	63P	K8	L20	-	K9	AA19	AA18
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	63N	K10	L21	-	K11	U17	Y18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	64P	K12	L22	-	K13	V18	AD25
2	64N	K14	L23	-	K15	AB21	AD26
2	65P	K16	L24	-	K17	U18	AC23
2	65N	K18	L25	-	K19	T17	AC24
2	66P	K20	L26	-	K21	AB20	AC25
2	66N	K22	L27	-	K23	AA20	AC26
2	67P	K24	L28	-	K25	Y19	AB22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	67N	K26	L29	-	K27	V19	AB23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	68P	K28	J16	L16	K29	T18	AB24
2	68N	K30	J17	L17	K31	R17	AB25
2	69P	L0	J18	L18	L1	U19	AB26
2	69N	L2	J19	L19	L3	T19	AA26
2	70P	L4	L30	I24	L5	V20	AA22
-	-	VCC	-	-	-	VCC	VCC
2	70N	L6	L31	I26	L7	U20	Y21
2	71P	L8	J20	L20	L9	W20	AA23
2	71N	L10	J21	L21	L11	Y21	AA24
2	72P	L12	J22	L22	L13	R18	AA25
2	72N	L14	J23	L23	L15	R19	Y26
-	-	GND	-	-	-	GND	GND
2	73P	L16	J24	L24	L17	W21	Y22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	73N	L18	J25	L25	L19	Y22	Y23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	74P	L20	J26	L26	L21	R20	W20
2	74N	L22	J27	L27	L23	P20	V20
2	75P	L24	J28	L28	L25	T21	W21
2	75N	L26	J29	L29	L27	R21	V21
2	76P	L28	J30	L30	L29	U21	Y24
2	76N	L30	J31	L31	L31	V21	Y25
2	77P	N0	P0	N0	N1	—	W22
2	77N	N2	P1	N1	N3	—	W23
2	78P	N4	P2	N2	N5	—	W24
-	-	VCC	-	-	-	VCC	VCC
2	78N	N6	P3	N3	N7	—	W25
-	-	GND	-	-	-	GND	GND
2	79P	N8	P4	N4	N9	—	W26

Lead-Free Packaging

ispXPLD 5000MC (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4FN256C	256	1.8	4.0	Lead-free fpBGA	256	141	C
	LC5256MC-5FN256C	256	1.8	5.0	Lead-free fpBGA	256	141	C
	LC5256MC-75FN256C	256	1.8	7.5	Lead-free fpBGA	256	141	C
LC5512MC	LC5512MC-45QN208C	512	1.8	4.5	Lead-free PQFP	208	149	C
	LC5512MC-75QN208C	512	1.8	7.5	Lead-free PQFP	208	149	C
	LC5512MC-45FN256C	512	1.8	4.5	Lead-free fpBGA	256	193	C
	LC5512MC-75FN256C	512	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5512MC-45FN484C	512	1.8	4.5	Lead-free fpBGA	484	253	C
	LC5512MC-75FN484C	512	1.8	7.5	Lead-free fpBGA	484	253	C
LC5768MC	LC5768MC-5FN256C	768	1.8	5.0	Lead-free fpBGA	256	193	C
	LC5768MC-75FN256C	768	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5768MC-5FN484C	768	1.8	5.0	Lead-free fpBGA	484	317	C
	LC5768MC-75FN484C	768	1.8	7.5	Lead-free fpBGA	484	317	C
LC51024MC	LC51024MC-52FN484C	1024	1.8	5.2	Lead-free fpBGA	484	317	C
	LC51024MC-75FN484C	1024	1.8	7.5	Lead-free fpBGA	484	317	C
	LC51024MC-52FN672C	1024	1.8	5.2	Lead-free fpBGA	672	381	C
	LC51024MC-75FN672C	1024	1.8	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5FN256I	256	1.8	5.0	Lead-free fpBGA	256	141	I
	LC5256MC-75FN256I	256	1.8	7.5	Lead-free fpBGA	256	141	I
LC5512MC	LC5512MC-75QN208I	512	1.8	7.5	Lead-free PQFP	208	149	I
	LC5512MC-75FN256I	512	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5512MC-75FN484I	512	1.8	7.5	Lead-free fpBGA	484	253	I
LC5768MC	LC5768MC-75FN256I	768	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5768MC-75FN484I	768	1.8	7.5	Lead-free fpBGA	484	317	I
LC51024MC	LC51024MC-75FN484I	1024	1.8	7.5	Lead-free fpBGA	484	317	I
	LC51024MC-75FN672I	1024	1.8	7.5	Lead-free fpBGA	672	381	I