Lattice Semiconductor Corporation - LC5512MV-45QN208C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

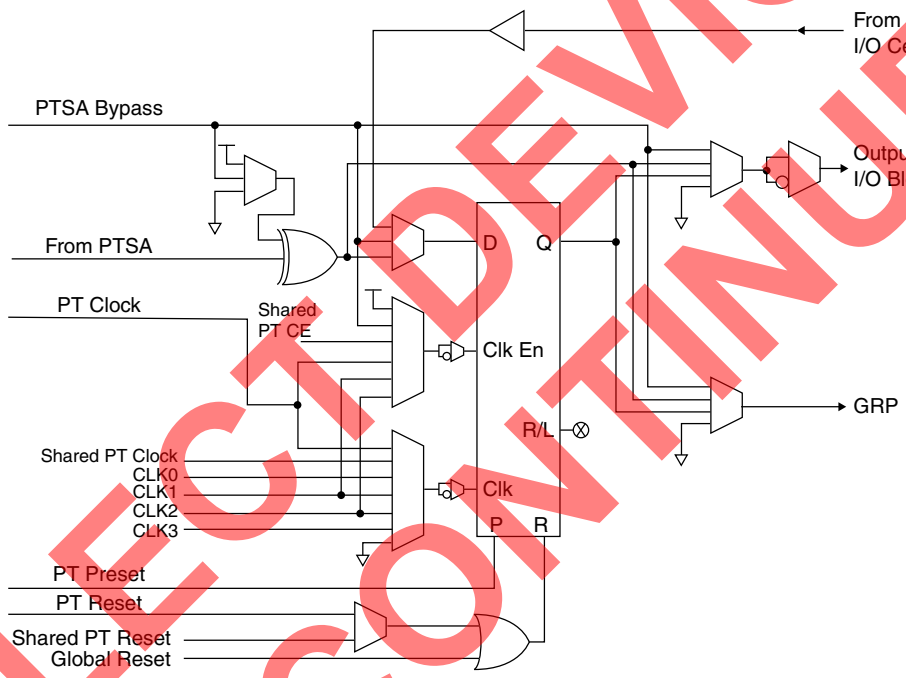
Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	149
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-45qn208c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in TN1030, Using Memory in ispXPLD 5000MX Devices.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

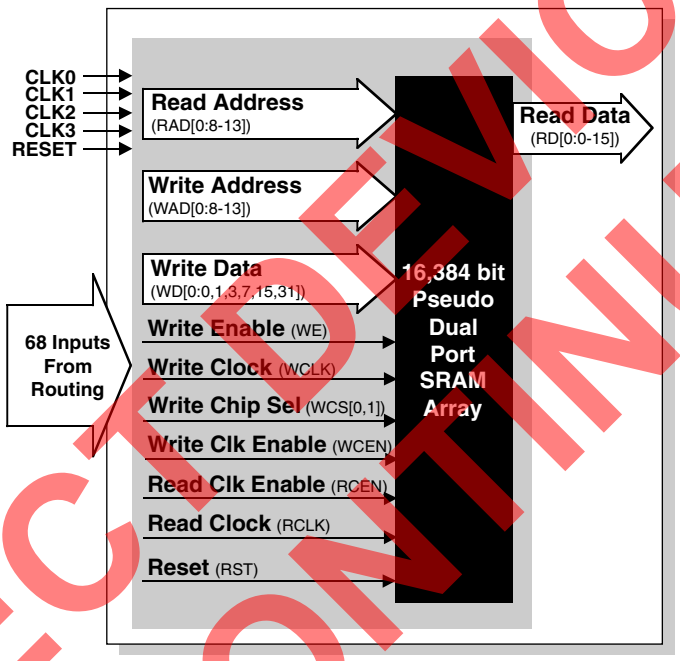


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

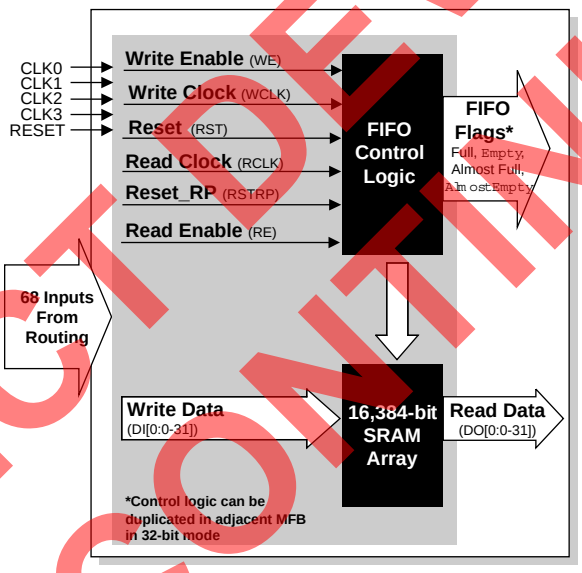


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

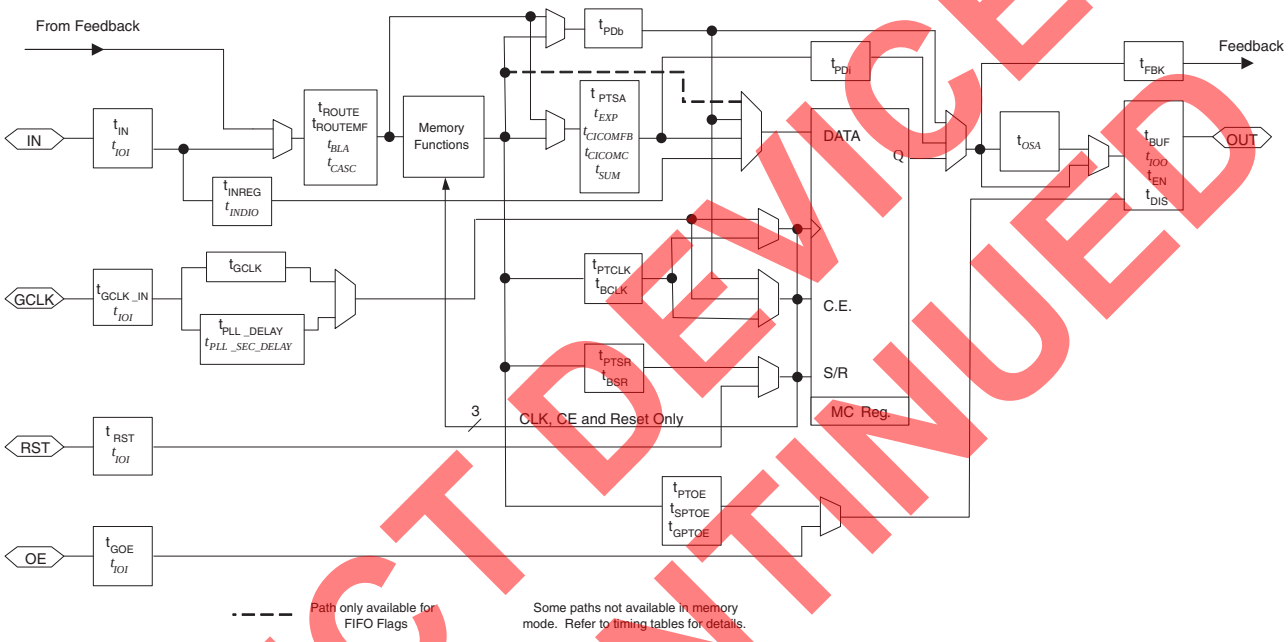
Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} and V_{IH} = 0.65 * V_{CC}.
4. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8.

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—	1.33	ns
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—	0.66	ns
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—	0.19	ns
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—	4.91	ns
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	2.89	—	3.21	—	3.34	—	4.82	ns
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—	1.50	ns
Optional Adjusters													
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—	0.07	ns
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—	0.99	ns
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—	0.94	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—	0.91	ns
t_{INEXP}	MFB Input Extender	t_{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—	1.16	ns
Input and Output Buffer Delays													
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables										ns
t_{IOO}	Output Buffer Selection Adder	t_{BUF}											ns
FIFO													
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—	4.00	ns
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

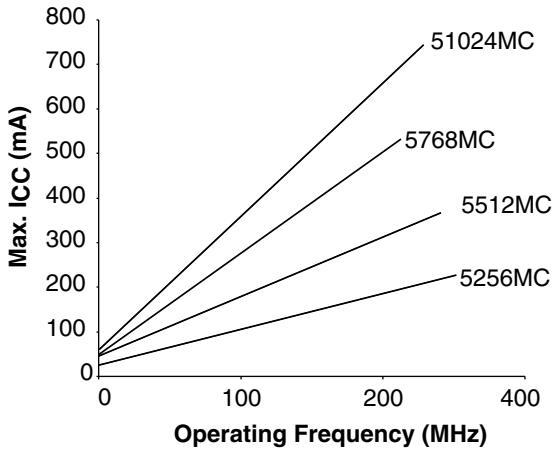
Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CAMWMSKS}$	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t_{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t_{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

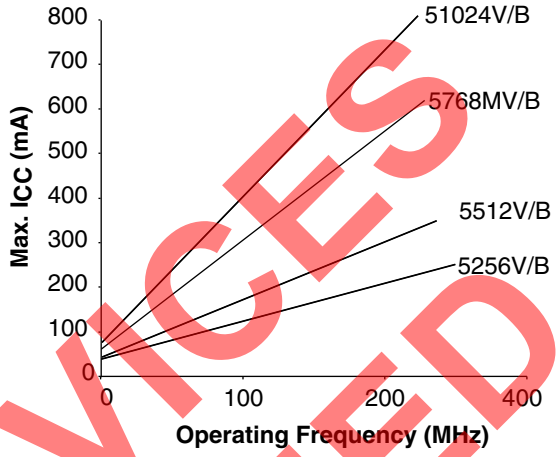
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	GCLK0N	GCLK1	—	—	—	28	J2	P7
—	—	GND	—	—	—	29	GND	GND
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	V_{CCO1}
1	3N	A14/DATA7	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	—	—	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	—	P1[1]	V3
1	7P	A28	—	—	A29	—	M3	Y2
1	7N	A30	—	—	A31	—	L4	W3
1	8P	B0	A0	—	B1	—	N2	U5
1	8N	B2	A2	—	B3	—	P2	T5
—	—	GND (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	—	R1	U4
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	9N	B5	A6	—	—	—	R2	V4
1	10P	B6	A8	—	B7	—	T2	AA3
1	10N	B8	A10	—	B9	—	T3	AB3
1	—	B10	A12	—	B11	—	—	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	—	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	V19
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	—	—	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	—	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	—	AA6
1	18N	C12	-	-	C13	—	AA7
1	19P	C10	-	-	C11	—	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	76P	L30/PLL_FBK1	L0	J0	L31	F15	E21
3	77N	M0/PLL_RST1	P27	N27	M1	H12	G22
3	77P	M2	P26	N26	M3	G14	F21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	78N	M4	P25	N25	M5	F16	H21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	78P	M6	P24	N24	-	E16	G21
-	-	GND	-	-	-	GND	GND
3	79N	M8	P23	N23	M9	G13	D22
3	79P	M10	P22	N22	M11	G12	D21
3	80N	M12	P21	N21	M13	F14	J20
3	80P	M14/CLK_OUT1	P20	N20	M15	E15	J19
3	81N	M16	N31	-	M17	F12	E20
-	-	VCC	-	-	-	VCC	VCC
3	81P	M18	N30	M30	M19	F13	F20
3	82N	M20	N29	M28	M21	D16	H17
3	82P	M22	N28	M26	M23	D15	H18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	83N	M24	N27	-	M25	—	J18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	83P	M26	N26	-	M27	—	H19
3	84N	M28	N25	-	M29	—	G20
3	84P	M30	N24	-	M31	—	G19
-	-	GND	-	-	-	GND	GND
3	85N	N0	N23	-	N1	—	C22
-	-	VCC	-	-	-	VCC	VCC
3	85P	N2	N22	-	N3	—	C21
3	86N	N4	N21	-	-	—	D20
3	86P	N6	N20	-	-	—	C19
3	87N	N8	N19	-	N9	C16	F19
3	87P	N10	N18	-	N11	B16	E19
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	88N	N12	N17	-	N13	C15	G18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	88P	N14	N16	-	N15	B15	F18
3	89N	N16	N15	-	N17	E14	B20
3	89P	N18	N14	-	N19	D14	B19
3	90N	N20	N13	-	N21	E13	A20
3	90P	N22	N12	-	N23	A15	A19
3	91N	N24	P19	N19	N25	D12	D18
3	91P	N26	P18	N18	N27	B14	C18
3	92N	N28	P17	N17	N29	C13	G17
3	92P	N30	P16	N16	N31	A14	F16

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND	-	-	-	GND	GND
2	46P	I4	J2	L2	I5	Y12	AF19
2	46N	I6	J3	L3	I7	AA13	AF20
2	47P	I8	J4	L4	I9	V12	AF21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	47N	I10	J5	L5	I11	U12	AF22
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	48P	I12	J6	L6	I13	AB13	AF23
2	48N	I14	J7	L7	I15	Y13	AF24
2	49P	I16	L0	-	I17	V13	AE17
2	49N	I18/VREF2	L1	-	I19	W13	AE18
2	50P	I20	J8	L8	I21	V14	AE19
2	50N	I22	J9	L9	I23	W14	AE20
2	51P	I24	J10	L10	I25	Y14	AE21
2	51N	I26	J11	L11	I27	AB14	AE22
2	52P	I28	J12	L12	I29	AB15	AE23
2	52N	I30	J13	L13	I31	AA15	AE24
2	53P	J0	J14	L14	J1	U13	AD17
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	53N	J2	J15	L15	J3	U14	AD18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	54P	J4	L2	I0	J5	W15	AD19
2	54N	J6	L3	I2	J7	W16	AD20
2	55P	J8	L4	I4	J9	Y16	AD21
2	55N	J10	L5	I6	J11	AA16	AD22
2	56P	J12	L6	I8	J13	AB16	AD23
2	56N	J14	L7	I10	J15	AA17	AD24
2	57P	J16	L8	I12	J17	Y17	AC22
2	57N	J18	L9	I16	J19	AA18	AC21
2	58P	J20	L10	I20	J21	W17	AC18
-	-	VCC	-	-	-	VCC	VCC
2	58N	J22	L11	I22	J23	W18	AC19
-	-	GND	-	-	-	GND	GND
2	59P	J24	L12	-	J25	V15	AC20
-	-	VCCO2		-	-	VCCO2	VCCO2
2	59N	J26	L13	-	J27	U15	AB21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	60P	J28	L14	-	J29	Y18	AB18
2	60N	J30	L15	-	J31	V17	AB19
2	61P	K0	L16	-	K1	V16	AB20
2	61N	K2	L17	-	K3	U16	AA20
2	62P	K4	L18	-	K5	AB18	AA19
2	62N	K6	L19	-	K7	AB19	Y19

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	142N	Y26	Y29	AA29	Y27	B11	A10
0	142P	Y24	Y28	AA28	Y25	A11	A9
0	143N	Y22	Y27	AA27	Y23	F11	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	Y20	Y26	AA26	Y21	F10	A7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	Y18	Y25	AA25	Y19	E10	A6
0	144P	Y16	Y24	AA24	Y17	C10	A5
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	A4
0	145P	Y12	Y2	AA2	Y13	B10	A3
0	146N	Y10	Y23	AA23	Y11	A10	B10
0	146P	Y8	Y22	AA22	Y9	A9	B9
0	147N	Y6	Y21	AA21	Y7	C9	B8
0	147P	Y4	Y20	AA20	Y5	D9	B7
0	148N	Y2	Y19	AA19	Y3	F9	B6
0	148P	Y0	Y18	AA18	Y1	E9	B5
0	149N	Z30	Y1	AA1	Z31	A8	B4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	149P	Z28	Y0	AA0	Z29	B8	B3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	150N	Z26	AA29	-	Z27	A7	C10
0	150P	Z24	AA28	-	Z25	B7	C9
0	151N	Z22	AA27	-	Z23	A5	C8
0	151P	Z20	AA26	-	Z21	B5	C7
0	152N	Z18	AA25	-	Z19	B6	C6
0	152P	Z16	AA24	-	Z17	C7	C5
0	153N	Z14	AA23	-	Z15	E8	C4
0	153P	Z12	AA22	-	Z13	E7	D5
0	154N	Z10	AA21	-	Z11	E6	D9
-	-	VCC	-	-	-	VCC	VCC
0	154P	Z8	AA20	-	Z9	D6	D8
-	-	GND	-	-	-	GND	GND
0	155N	Z6	AA19	-	Z7	D8	D7
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	155P	Z4	AA18	-	Z5	F8	D6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	156N	Z2	AA17	-	Z3	F7	F9
0	156P	Z0	AA16	-	Z1	D7	E9
0	157N	AA30	AA15	-	AA31	C6	F7
0	157P	AA28	AA14	-	AA29	C5	F8
0	158N	AA26	AA13	-	AA27	C4	G8
0	158P	AA24	AA12	-	AA25	D5	G9

Lead-Free Packaging

ispXPLD 5000MC (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4FN256C	256	1.8	4.0	Lead-free fpBGA	256	141	C
	LC5256MC-5FN256C	256	1.8	5.0	Lead-free fpBGA	256	141	C
	LC5256MC-75FN256C	256	1.8	7.5	Lead-free fpBGA	256	141	C
LC5512MC	LC5512MC-45QN208C	512	1.8	4.5	Lead-free PQFP	208	149	C
	LC5512MC-75QN208C	512	1.8	7.5	Lead-free PQFP	208	149	C
	LC5512MC-45FN256C	512	1.8	4.5	Lead-free fpBGA	256	193	C
	LC5512MC-75FN256C	512	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5512MC-45FN484C	512	1.8	4.5	Lead-free fpBGA	484	253	C
	LC5512MC-75FN484C	512	1.8	7.5	Lead-free fpBGA	484	253	C
LC5768MC	LC5768MC-5FN256C	768	1.8	5.0	Lead-free fpBGA	256	193	C
	LC5768MC-75FN256C	768	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5768MC-5FN484C	768	1.8	5.0	Lead-free fpBGA	484	317	C
	LC5768MC-75FN484C	768	1.8	7.5	Lead-free fpBGA	484	317	C
LC51024MC	LC51024MC-52FN484C	1024	1.8	5.2	Lead-free fpBGA	484	317	C
	LC51024MC-75FN484C	1024	1.8	7.5	Lead-free fpBGA	484	317	C
	LC51024MC-52FN672C	1024	1.8	5.2	Lead-free fpBGA	672	381	C
	LC51024MC-75FN672C	1024	1.8	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5FN256I	256	1.8	5.0	Lead-free fpBGA	256	141	I
	LC5256MC-75FN256I	256	1.8	7.5	Lead-free fpBGA	256	141	I
LC5512MC	LC5512MC-75QN208I	512	1.8	7.5	Lead-free PQFP	208	149	I
	LC5512MC-75FN256I	512	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5512MC-75FN484I	512	1.8	7.5	Lead-free fpBGA	484	253	I
LC5768MC	LC5768MC-75FN256I	768	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5768MC-75FN484I	768	1.8	7.5	Lead-free fpBGA	484	317	I
LC51024MC	LC51024MC-75FN484I	1024	1.8	7.5	Lead-free fpBGA	484	317	I
	LC51024MC-75FN672I	1024	1.8	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5512MV	LC5512MV-45QN208C	512	3.3	4.5	Lead-free PQFP	208	149	C
	LC5512MV-75QN208C	512	3.3	7.5	Lead-free PQFP	208	149	C
	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	193	C
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	253	C
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	253	C
LC5768MV	LC5768MV-5FN256C	768	3.3	5.0	Lead-free fpBGA	256	193	C
	LC5768MV-75FN256C	768	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5768MV-5FN484C	768	3.3	5.0	Lead-free fpBGA	484	317	C
	LC5768MV-75FN484C	768	3.3	7.5	Lead-free fpBGA	484	317	C
LC51024MV	LC51024MV-52FN484C	1024	3.3	5.2	Lead-free fpBGA	484	317	C
	LC51024MV-75FN484C	1024	3.3	7.5	Lead-free fpBGA	484	317	C
	LC51024MV-52FN672C	1024	3.3	5.2	Lead-free fpBGA	672	381	C
	LC51024MV-75FN672C	1024	3.3	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5FN256I	256	3.3	5.0	Lead-free fpBGA	256	141	I
	LC5256MV-75FN256I	256	3.3	7.5	Lead-free fpBGA	256	141	I
LC5512MV	LC5512MV-75QN208I	512	3.3	7.5	Lead-free PQFP	208	149	I
	LC5512MV-75FN256I	512	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5512MV-75FN484I	512	3.3	7.5	Lead-free fpBGA	484	253	I
LC5768MV	LC5768MV-75FN256I	768	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5768MV-75FN484I	768	3.3	7.5	Lead-free fpBGA	484	317	I
LC51024MV	LC51024MV-75FN484I	1024	3.3	7.5	Lead-free fpBGA	484	317	I
	LC51024MV-75FN672I	1024	3.3	7.5	Lead-free fpBGA	672	381	I

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- TN1000 – sysIO Usage Guidelines for Lattice Devices
- TN1003 – sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices
- TN1031 – Power Estimation in ispXPLD 5000MX Devices
- TN1030 – Using Memory in ispXPLD 5000MX Devices
- TN1026 – ispXP Configuration Usage Guidelines