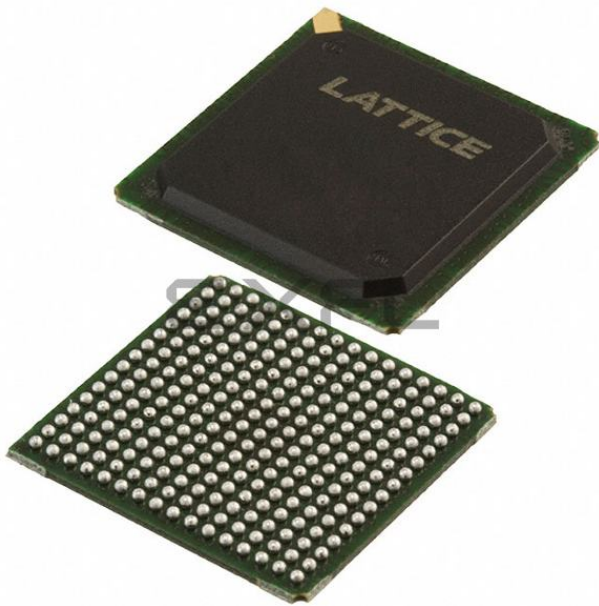




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	193
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75f256i



Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	Discontinued	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	Discontinued	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	Discontinued	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

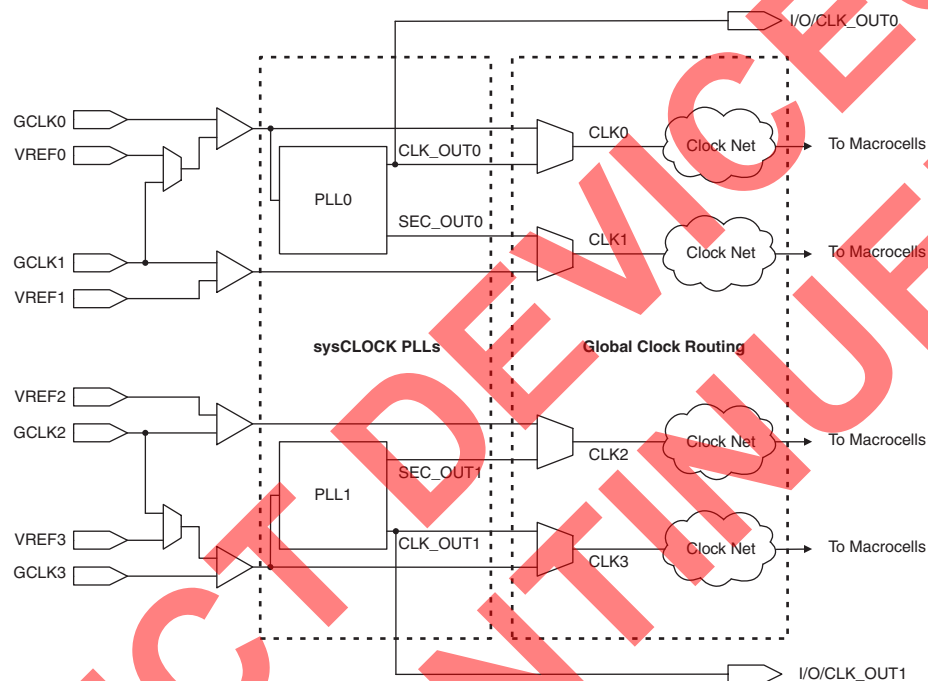


Product Line	Ordering Part Number	Product Status	Reference PCN
LC51024MV	LC51024MV-52F484C	Active / Orderable	
	LC51024MV-52FN484C		
	LC51024MV-75F484C		
	LC51024MV-75FN484C		
	LC51024MV-75F484I		
	LC51024MV-75FN484I		
	LC51024MV-52F672C		
	LC51024MV-52FN672C		
	LC51024MV-75F672C		
	LC51024MV-75FN672C		
	LC51024MV-75F672I		
	LC51024MV-75FN672I		
LC51024MB	LC51024MB-52F484C	Discontinued	PCN#09-10
	LC51024MB-52FN484C		
	LC51024MB-75F484C		
	LC51024MB-75FN484C		
	LC51024MB-75F484I		
	LC51024MB-75FN484I		
	LC51024MB-52F672C		
	LC51024MB-52FN672C		
	LC51024MB-75F672C		
	LC51024MB-75FN672C		
	LC51024MB-75F672I		
	LC51024MB-75FN672I		
LC51024MC	LC51024MC-52F484C	Discontinued	PCN#09-10
	LC51024MC-52FN484C		
	LC51024MC-75F484C		
	LC51024MC-75FN484C		
	LC51024MC-75F484I		
	LC51024MC-75FN484I		
	LC51024MC-52F672C		
	LC51024MC-52FN672C		
	LC51024MC-75F672C		
	LC51024MC-75FN672C		
	LC51024MC-75F672I		
	LC51024MC-75FN672I		

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GCLK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

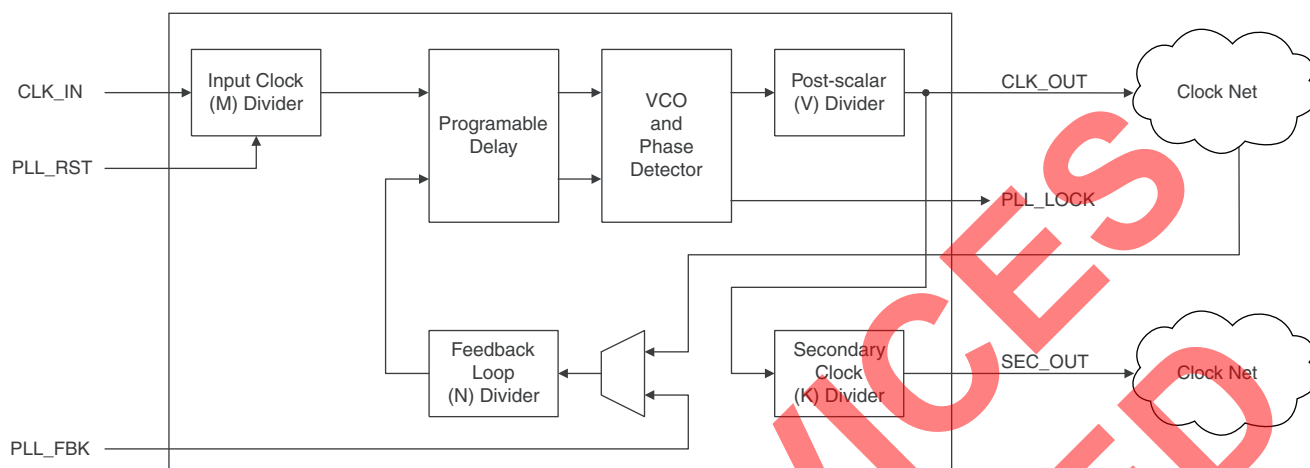
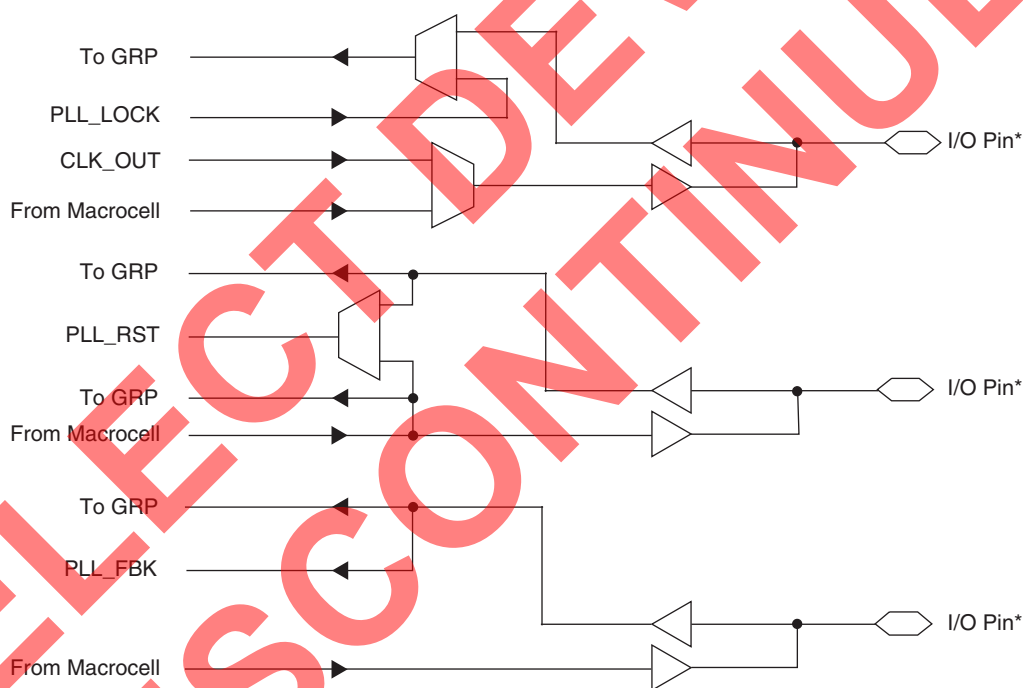
Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are de-skewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Figure 15. PLL Block Diagram**Figure 16. Connection of Optional PLL Inputs and Outputs**

*See pinout table for details

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, [sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices](#).

Supply Current

Symbol	Parameter	Condition	Min.	Typ. ³	Max.	Units
ispXPLD 5256						
$I_{CC}^{1,2}$	Operating Power Supply Current	$V_{CC} = 3.3V, f = 1.0MHz$	—	26	—	mA
		$V_{CC} = 2.5V, f = 1.0MHz$	—	26	—	mA
		$V_{CC} = 1.8V, f = 1.0MHz$	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	$V_{CCO} = 3.3V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 2.5V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 1.8V, f = 1.0MHz, \text{ unloaded}$	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	$V_{CCP} = 3.3V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 2.5V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 1.8V, f = 10MHz$	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	$V_{CCJ} = 3.3V$	—	1	—	mA
		$V_{CCJ} = 2.5V$	—	1	—	mA
		$V_{CCJ} = 1.8V$	—	1	—	mA
ispXPLD 5512						
$I_{CC}^{1,2}$	Operating Power Supply Current	$V_{CC} = 3.3V, f = 1.0MHz$	—	33	—	mA
		$V_{CC} = 2.5V, f = 1.0MHz$	—	33	—	mA
		$V_{CC} = 1.8V, f = 1.0MHz$	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	$V_{CCO} = 3.3V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 2.5V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 1.8V, f = 1.0MHz, \text{ unloaded}$	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	$V_{CCP} = 3.3V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 2.5V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 1.8V, f = 10MHz$	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	$V_{CCJ} = 3.3V$	—	1	—	mA
		$V_{CCJ} = 2.5V$	—	1	—	mA
		$V_{CCJ} = 1.8V$	—	1	—	mA
ispXPLD 5768						
$I_{CC}^{1,2}$	Operating Power Supply Current	$V_{CC} = 3.3V, f = 1.0MHz$	—	40	—	mA
		$V_{CC} = 2.5V, f = 1.0MHz$	—	40	—	mA
		$V_{CC} = 1.8V, f = 1.0MHz$	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	$V_{CCO} = 3.3V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 2.5V, f = 1.0MHz, \text{ unloaded}$	—	4	—	mA
		$V_{CCO} = 1.8V, f = 1.0MHz, \text{ unloaded}$	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	$V_{CCP} = 3.3V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 2.5V, f = 10MHz$	—	11	—	mA
		$V_{CCP} = 1.8V, f = 10MHz$	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	$V_{CCJ} = 3.3V$	—	1	—	mA
		$V_{CCJ} = 2.5V$	—	1	—	mA
		$V_{CCJ} = 1.8V$	—	1	—	mA

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}^2 (mA)	I_{OH}^2 (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCO} - 0.4$	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 1.8 ^{1,3}	-0.3	0.68	1.07	3.6	0.4	$V_{CCO} - 0.4$	8	-8
LVCMOS 1.8 ³	-0.3	0.68	1.07	3.6	0.4	$V_{CCO} - 0.4$	12, 5.33, 4	-12, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
PCI 3.3 ⁴	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X ⁴	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCO} - 0.43$	15.2	-15.2
CTT 3.3	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
CTT 2.5	-0.3	$V_{REF} - 0.3$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
HSTL class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL class III	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL class IV	-0.3	$V_{REF} - 0.3$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
GTL+	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	n/a	36	n/a

1. Software default setting.

2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n \cdot 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.3. For 1.8V devices (ispXPLD 5000MC) these specifications are $V_{IL} = 0.35 \cdot V_{CC}$ and $V_{IH} = 0.65 \cdot V_{CC}$.4. For 1.8V devices (ispXPLD 5000MC) these specifications are $V_{IL} = 0.3 \cdot V_{CC} \cdot 3.3/1.8$, $V_{IH} = 0.5 \cdot V_{CC} \cdot 3.3/1.8$.

ispXPLD 5000MX Family External Switching Characteristics^{1, 2, 3}

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Out-put Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX}^4	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
$f_{MAX} (Ext.)$	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
$f_{MAX} (Tog.)$	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
$f_{MAX} (CAMC)^5$	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
$f_{MAX} (CAM)^5$	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

ispXPLD 5000MX Family Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays													
t _{IN}	Input Buffer Delay	—	—	0.70	—	0.91	—	0.96	—	1.11	—	1.30	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.40	—	0.35	—	0.35	—	0.35	—	0.55	ns
t _{RST}	Global RESET Pin Delay	—	—	3.77	—	4.24	—	4.71	—	4.71	—	7.07	ns
t _{GOE}	Global OE Pin Delay	—	—	1.98	—	2.66	—	2.34	—	2.87	—	3.27	ns
t _{BUF}	Delay through Output Buffer	—	—	1.16	—	1.30	—	1.45	—	1.60	—	2.17	ns
t _{EN}	Output Enable Time	—	—	2.52	—	2.84	—	3.16	—	3.63	—	4.23	ns
t _{DIS}	Output Disable Time	—	—	1.92	—	2.40	—	2.40	—	2.40	—	3.60	ns
Routing Delays													
t _{ROUTE}	Delay through SRP	—	—	1.95	—	2.06	—	2.34	—	2.24	—	3.66	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.60	—	0.60	—	0.60	—	0.47	—	1.63	ns
t _{PTSA}	Product Term Sharing Array Delay	—	—	0.50	—	0.50	—	0.53	—	0.83	—	1.34	ns
t _{FBK}	Internal Feedback Delay	—	—	0.19	—	0.02	—	0.39	—	0.03	—	0.60	ns
t _{GCLK}	Global Clock Tree Delay	—	—	0.52	—	0.32	—	0.72	—	0.82	—	0.78	ns
t _{BCLK}	Block PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t _{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.30	—	0.30	—	0.30	—	0.30	ns
t _{BSR}	Block PT Reset Delay	—	—	0.72	—	0.81	—	0.90	—	0.94	—	1.35	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	—	0.60	—	0.75	—	0.75	—	0.75	—	1.13	ns
t _{LP_{TOE}}	Macrocell PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t _{SPTOE}	Segment PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t _{OSA}	Output Sharing Array Delay	—	—	0.80	—	0.90	—	1.00	—	1.00	—	1.50	ns
t _{PTOE}	Global PT OE Delay	—	—	0.83	—	1.04	—	1.04	—	1.04	—	1.56	ns
t _{PDB}	5-PT Bypass Propagation Delay	—	—	0.20	—	0.23	—	0.25	—	0.25	—	0.38	ns
t _{PDI}	Macrocell Propagation Delay	—	—	0.50	—	0.93	—	0.72	—	0.72	—	1.04	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{FIFOWES}	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
t _{FIFOWEH}	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{FIFORES}	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
t _{FIFOREH}	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
t _{FIFORSTO}	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
t _{FIFORSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
t _{FIFORSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
t _{FIFORCLKO}	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t _{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t _{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMENMSKS}	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMENMSKH}	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMADDS}	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMADDH}	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMDATAS}	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
t _{CAMDATAH}	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMDACS}	“Don’t Care” Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMDCH}	“Don’t Care” Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t _{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	GCLK0N	GCLK1	—	—	—	28	J2	P7
—	—	GND	—	—	—	29	GND	GND
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V _{CCO1}	—	—	—	42	V _{CCO1}	V _{CCO1}
1	3N	A14/DATA7	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	—	—	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	—	P1 ¹	V3
1	7P	A28	—	—	A29	—	M3	Y2
1	7N	A30	—	—	A31	—	L4	W3
1	8P	B0	A0	—	B1	—	N2	U5
1	8N	B2	A2	—	B3	—	P2	T5
—	—	GND (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	—	R1	U4
—	—	V _{CCO1}	—	—	—	—	V _{CCO1}	V _{CCO1}
1	9N	B5	A6	—	—	—	R2	V4
1	10P	B6	A8	—	B7	—	T2	AA3
1	10N	B8	A10	—	B9	—	T3	AB3
1	—	B10	A12	—	B11	—	—	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	—	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	61N	I14	I23	K23	I15	149	G13	D22
3	61P	I12	I22	K22	I13	150	G12	D21
3	62N	I10	I21	K21	I11	151	F14	J20
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	J19
3	63N	I6	K31	—	I7	—	F12	E20
—	—	V _{CC}	—	—	—	153	V _{CC}	V _{CC}
3	63P	I4	K30	L30	I5	—	F13	F20
3	64N	I2	K29	L28	I3	—	D16	H17
3	64P	I0	K28	L26	I1	—	D15	H18
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	65N	J30	K27	—	J31	—	—	J18
—	—	V _{CCO3}	—	—	—	—	V _{CCO3}	V _{CCO3}
3	65P	J28	K26	—	J29	—	—	H19
3	66N	J26	K25	—	J27	—	—	G20
3	66P	J24	K24	—	J25	—	—	G19
3	67N	J22	K23	—	J23	—	—	C22
3	67P	J20	K22	—	J21	—	—	C21
3	68N	J18	K21	—	J19	—	—	D20
3	68P	J16	K20	—	J17	—	—	C19
3	69N	J14	K19	—	J15	—	C16	F19
3	69P	J12	K18	—	J13	—	B16	E19
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	70N	J10	K17	—	J11	—	C15	G18
—	—	V _{CCO3}	—	—	—	—	V _{CCO3}	V _{CCO3}
3	70P	J8	K16	—	J9	—	B15	F18
3	71N	J6	K15	—	J7	—	E14	B20
3	71P	J4	K14	—	J5	—	D14	B19
3	72N	J2	K13	—	J3	—	E13	A20
3	72P	J0	K12	—	J1	—	A15	A19
3	73N	K30	I19	K19	K31	154	D12	D18
3	73P	K28	I18	K18	K29	155	B14	C18
3	74N	K26	I17	K17	K27	156	C13	G17
3	74P	K24	I16	K16	K25	157	A14	F16
3	75N	K22	I31	K31	K23	158	A13	E17
3	75P	K21	I30	K30	—	159	B13	D17
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	GND (Bank 3)
3	76N	K20	K11	L21	—	—	D11	B18
—	—	V _{CCO3}	—	—	—	161	V _{CCO3}	V _{CCO3}
3	76P	K18	K10	L20	K19	—	B12	A18
3	77N	K16	K9	L18	K17	—	C12	C17
3	77P	K14	K8	L16	K15	—	E11	B17
3	78N	K12	K7	L12	K13	—	—	C16
3	78P	K10	K6	L10	K11	—	—	B16

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10 ¹	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V _{CCO3}	—	—	—	—	V _{CCO3}	V _{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V _{CCO3}	—	—	—	176	V _{CCO3}	V _{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V _{CCO0}	—	—	—	189	V _{CCO0}	V _{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V _{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	143N	U22	U27	W27	U23	—	K6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	U20	U26	W26	U21	—	K3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	U18	U25	W25	U19	—	K5
0	144P	U16	U24	W24	U17	—	K2
0	145N	U14	U23	W23	U15	—	L5
0	145P	U12	U22	W22	U13	—	K1
0	146N	U10	U21	W21	U11	—	L6
0	146P	U8	U20	W20	U9	—	L1
0	147N	U6	U19	W19	U7	—	M5
0	147P	U4	U18	W18	U5	—	L2
0	148N	U2	U17	W17	U3	—	N5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	148P	U0	U16	W16	U1	—	L3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	149N	W30	U15	W15	W31	—	M6
0	149P	W28	U14	W14	W29	—	M2
0	150N	W26	U13	W13	W27	—	P5
-	-	VCC	-	-	-	VCC	VCC
0	150P	W24	U12	W12	W25	—	P6
0	151N	W22	U11	W11	W23	—	M3
0	151P	W20	U10	W10	W21	—	N6
0	152N	W18	U9	W9	W19	—	N2
0	152P	W16	U8	W8	W17	—	P1
-	-	GND	-	-	-	GND	GND
0	153N	W14	U7	W7	W15	—	N3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	153P	W12	U6	W6	W13	—	M8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	154N	W10	U5	W5	W11	—	N8
0	154P	W8	U4	W4	-	—	P2
0	155N	W6	U3	W3	W7	—	P8
0	155P	W4	U2	W2	W5	—	N4
0	156N	W2	U1	W1	W3	G2	H1
0	156P	W0	U0	W0	W1	H1	J1
-	GCLK0P	GCLK0	-	-	-	H2	N7
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	J2	P7
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	H6	R1
-	-	TMS	-	-	-	H4	R2

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	-	AA6
1	18N	C12	-	-	C13	-	AA7
1	19P	C10	-	-	C11	-	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	110N	U4	X25	V25	U5	H21	J21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	110P	U6	X24	V24	U7	G21	H21
-	-	GND	-	-	-	GND	GND
3	111N	U8	X23	V23	U9	D22	G25
3	111P	U10	X22	V22	U11	D21	G24
3	112N	U12	X21	V21	U13	J20	G23
3	112P	U14/CLK_OUT1	X20	V20	U15	J19	G22
3	113N	U16	V31	-	U17	E20	J20
-	-	VCC	-	-	-	VCC	VCC
3	113P	U18	V30	U30	U19	F20	H20
3	114N	U20	V29	U28	U21	H17	G26
3	114P	U22	V28	U26	U23	H18	F25
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	115N	U24	V27	-	U25	J18	F24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	115P	U26	V26	-	U27	H19	F23
3	116N	U28	V25	-	U29	G20	G21
3	116P	U30	V24	-	U31	G19	F22
-	-	GND	-	-	-	GND	GND
3	117N	V0	V23	-	V1	C22	F26
-	-	VCC	-	-	-	VCC	VCC
3	117P	V2	V22	-	V3	C21	E26
3	118N	V4	V21	-	V5	D20	E25
3	118P	V6	V20	-	V7	C19	E24
3	119N	V8	V19	-	V9	F19	E23
3	119P	V10	V18	-	V11	E19	E22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	120N	V12	V17	-	V13	G18	D26
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	120P	V14	V16	-	V15	F18	D25
3	121N	V16	V15	-	V17	B20	D24
3	121P	V18	V14	-	V19	B19	D23
3	122N	V20	V13	-	V21	A20	C26
3	122P	V22	V12	-	V23	A19	C25
3	123N	V24	X19	V19	V25	D18	G19
3	123P	V26	X18	V18	V27	C18	F19
3	124N	V28	X17	V17	V29	G17	G18
3	124P	V30	X16	V16	V31	F16	F18
3	125N	W0	X31	V31	W1	E17	F20
3	125P	W2	X30	V30	W3	D17	E20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)

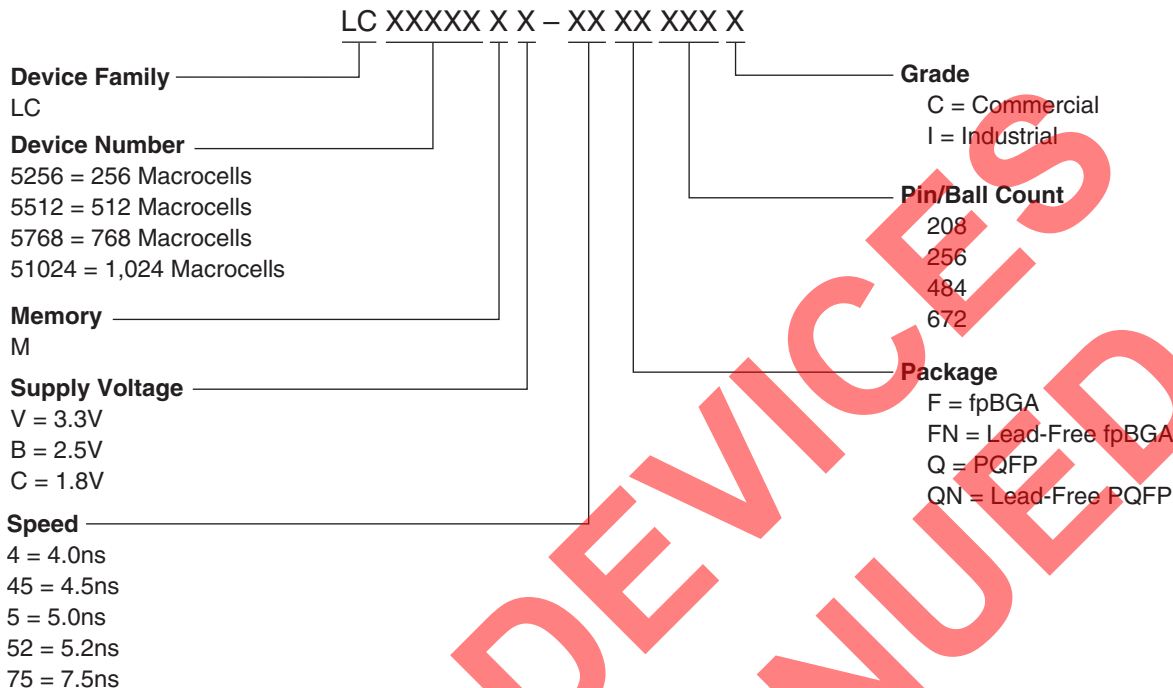
ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	126N	W4	V11	U21	W5	B18	E19
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	126P	W6	V10	U20	W7	A18	E18
-	-	GND	-	-	-	GND	GND
3	127N	W8	V9	U18	W9	C17	C24
-	-	VCC	-	-	-	VCC	VCC
3	127P	W10	V8	U16	W11	B17	C23
3	128N	W12	V7	U12	W13	C16	D22
3	128P	W14	V6	U10	W15	B16	D21
3	129N	W16	V5	U8	W17	F13	E21
3	129P	W18	V4	U6	W19	F15	D20
3	130N	W20	V3	U5	W21	D16	D19
3	130P	W22	V2	U4	W23	E16	D18
3	131N	W24	V1	U2	W25	A16	C22
3	131P	W26	V0	U0	W27	A15	C21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	132N	W28	X15	V15	W29	B15	C20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	132P	W30	X14	V14	W31	A14	C19
3	133N	X0	X13	V13	X1	D15	C18
3	133P	X2	X12	V12	X3	E15	C17
3	134N	X4	X11	V11	X5	D14	B24
3	134P	X6	X10	V10	X7	F14	B23
3	135N	X8	X9	V9	X9	A13	B22
3	135P	X10	X8	V8	X11	B13	B21
3	136N	X12/VREF3	X29	V29	X13	C14	B20
3	136P	X14	X28	V28	X15	E14	B19
3	137N	X16	X7	V7	X17	E13	B18
3	137P	X18	X6	V6	X19	F12	B17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	138N	X20	X5	V5	X21	D13	A24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	138P	X22	X4	V4	X23	C13	A23
3	139N	X24	X3	V3	X25	E12	A22
-	-	GND	-	-	-	GND	GND
3	139P	X26	X2	V2	X27	C12	A21
-	-	VCC	-	-	-	VCC	VCC
3	140N	X28	X1	V1	X29	B12	A20
3	140P	X30	X0	V0	X31	A12	A19
0	141N	Y30	Y31	AA31	Y31	E11	A18
-	-	VCC	-	-	-	VCC	VCC
0	141P	Y28	Y30	AA30	Y29	C11	A17
-	-	GND	-	-	-	GND	GND

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

SELECT DEVICES
DISCONTINUED

Part Number Description



Ordering Information

Note: For voltage families offered in industrial temperature grades and for all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -45XXXXC is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only. In addition, the fastest commercial speed grade (-5) for the LC5768MB/MV devices, at Lattice's discretion, will utilize either a commercial grade only single-mark or a dual-mark format in conjunction with the slower industrial speed grade (-75).

Conventional Packaging

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	141	C
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	141	C
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	141	C
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	149	C
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	149	C
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	193	C
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	193	C
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	253	C
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	253	C

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5512MV	LC5512MV-45QN208C	512	3.3	4.5	Lead-free PQFP	208	149	C
	LC5512MV-75QN208C	512	3.3	7.5	Lead-free PQFP	208	149	C
	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	193	C
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	253	C
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	253	C
LC5768MV	LC5768MV-5FN256C	768	3.3	5.0	Lead-free fpBGA	256	193	C
	LC5768MV-75FN256C	768	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5768MV-5FN484C	768	3.3	5.0	Lead-free fpBGA	484	317	C
	LC5768MV-75FN484C	768	3.3	7.5	Lead-free fpBGA	484	317	C
LC51024MV	LC51024MV-52FN484C	1024	3.3	5.2	Lead-free fpBGA	484	317	C
	LC51024MV-75FN484C	1024	3.3	7.5	Lead-free fpBGA	484	317	C
	LC51024MV-52FN672C	1024	3.3	5.2	Lead-free fpBGA	672	381	C
	LC51024MV-75FN672C	1024	3.3	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t _{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5FN256I	256	3.3	5.0	Lead-free fpBGA	256	141	I
	LC5256MV-75FN256I	256	3.3	7.5	Lead-free fpBGA	256	141	I
LC5512MV	LC5512MV-75QN208I	512	3.3	7.5	Lead-free PQFP	208	149	I
	LC5512MV-75FN256I	512	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5512MV-75FN484I	512	3.3	7.5	Lead-free fpBGA	484	253	I
LC5768MV	LC5768MV-75FN256I	768	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5768MV-75FN484I	768	3.3	7.5	Lead-free fpBGA	484	317	I
LC51024MV	LC51024MV-75FN484I	1024	3.3	7.5	Lead-free fpBGA	484	317	I
	LC51024MV-75FN672I	1024	3.3	7.5	Lead-free fpBGA	672	381	I

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- TN1000 – [sysIO Usage Guidelines for Lattice Devices](#)
- TN1003 – [sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices](#)
- TN1031 – [Power Estimation in ispXPLD 5000MX Devices](#)
- TN1030 – [Using Memory in ispXPLD 5000MX Devices](#)
- TN1026 – [ispXP Configuration Usage Guidelines](#)