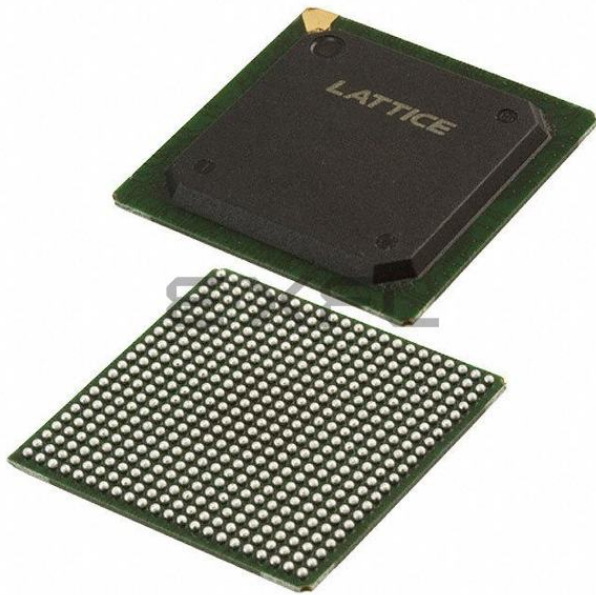




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	253
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75f484i



Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MC (Cont'd)	LC5512MC-45F484C	Discontinued	PCN#09-10
	LC5512MC-45FN484C		
	LC5512MC-75F484C		
	LC5512MC-75FN484C		
	LC5512MC-75F484I		
	LC5512MC-75FN484I		
LC5768MV	LC5768MV-5F256C	Active / Orderable	
	LC5768MV-5FN256C		
	LC5768MV-75F256C		
	LC5768MV-75FN256C		
	LC5768MV-75F256I		
	LC5768MV-75FN256I		
	LC5768MV-5F484C		
	LC5768MV-5FN484C		
	LC5768MV-75F484C		
	LC5768MV-75FN484C		
	LC5768MV-75F484I		
	LC5768MV-75FN484I		
	LC5768MB-5F256C	Discontinued	PCN#09-10
LC5768MB	LC5768MB-5FN256C		
	LC5768MB-75F256C		
	LC5768MB-75FN256C		
	LC5768MB-75F256I		
	LC5768MB-75FN256I		
	LC5768MB-5F484C		
	LC5768MB-5FN484C		
	LC5768MB-75F484C		
	LC5768MB-75FN484C		
	LC5768MB-75F484I		
	LC5768MB-75FN484I		
LC5768MC	LC5768MC-5F256C	Discontinued	PCN#09-10
	LC5768MC-5FN256C		
	LC5768MC-75F256C		
	LC5768MC-75FN256C		
	LC5768MC-75F256I		
	LC5768MC-75FN256I		
	LC5768MC-5F484C		
	LC5768MC-5FN484C		
	LC5768MC-75F484C		
	LC5768MC-75FN484C		
	LC5768MC-75F484I		
	LC5768MC-75FN484I		

Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

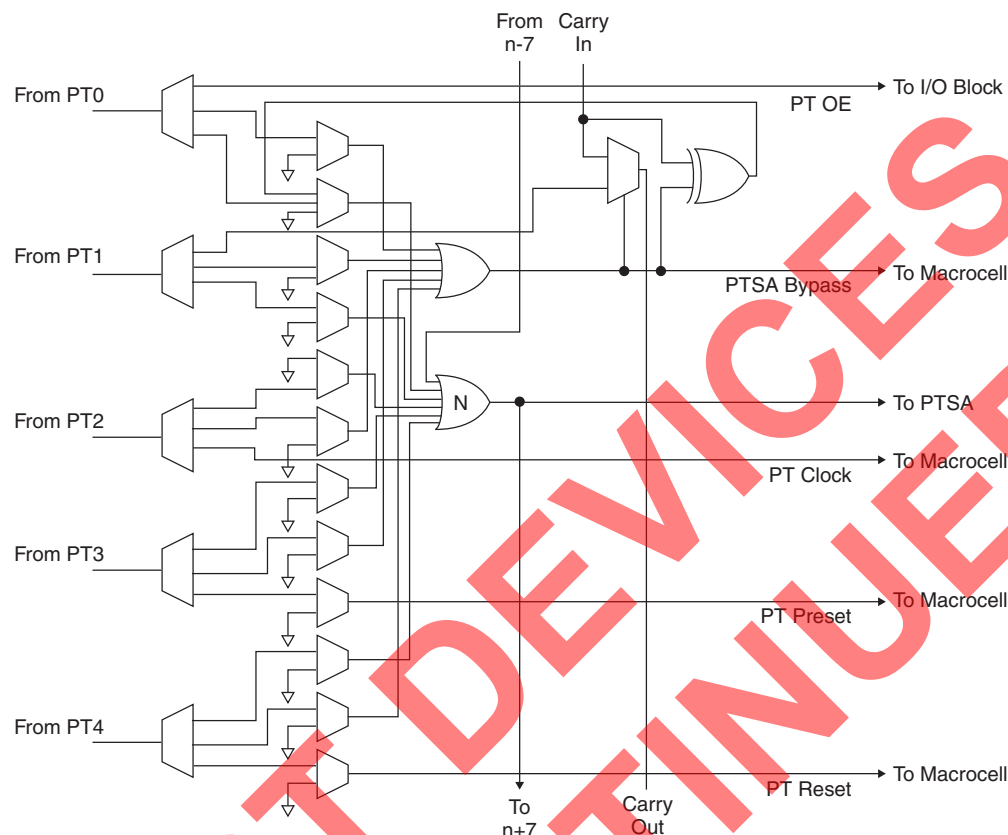
Mode	Cascading Function
Logic	Input Width. Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	Memory Width Expansion. Allows MFBs to be cascaded for greater width support.
CAM	Memory Width Expansion. Allows up to four MFBs to be cascaded for greater width support.

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	H → G → F → E
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

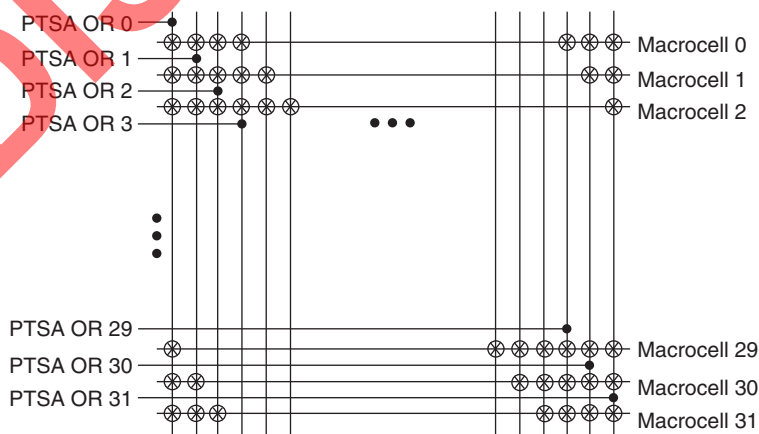
SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

Figure 6. Dual-OR PT Sharing Array

Product Term Sharing Array

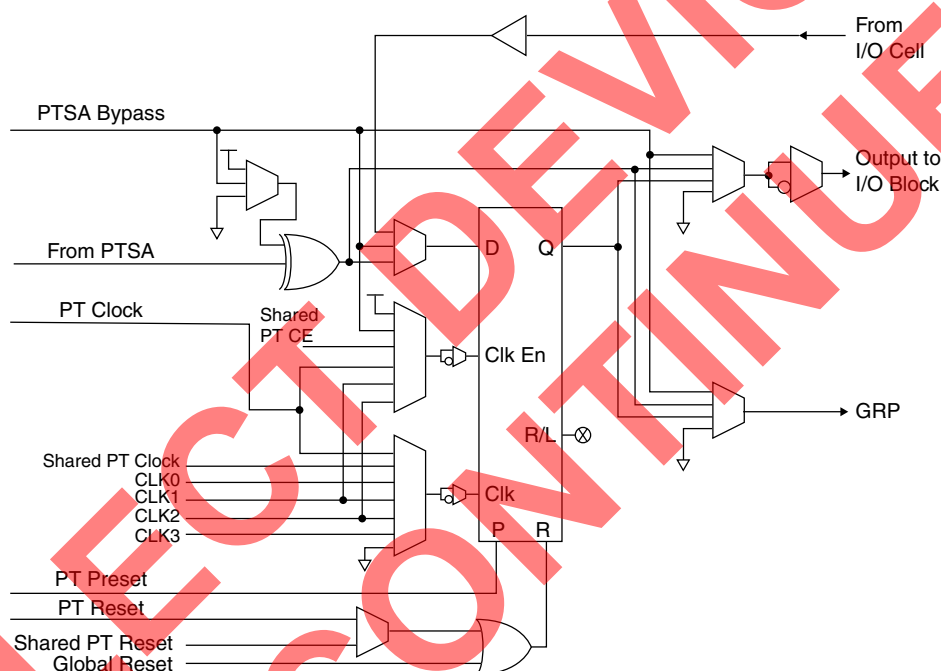
The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

Figure 7. Product Term Sharing Array (PTSA)

Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in TN1030, [Using Memory in ispXPLD 5000MX Devices](#).

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

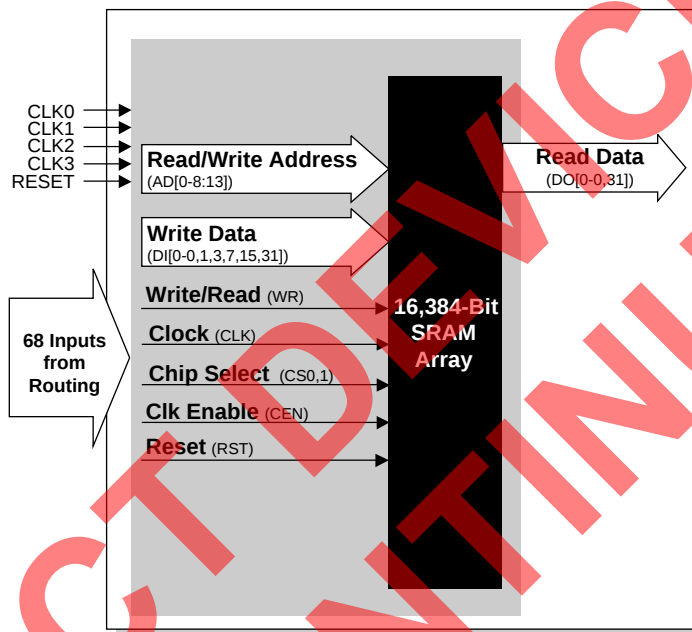
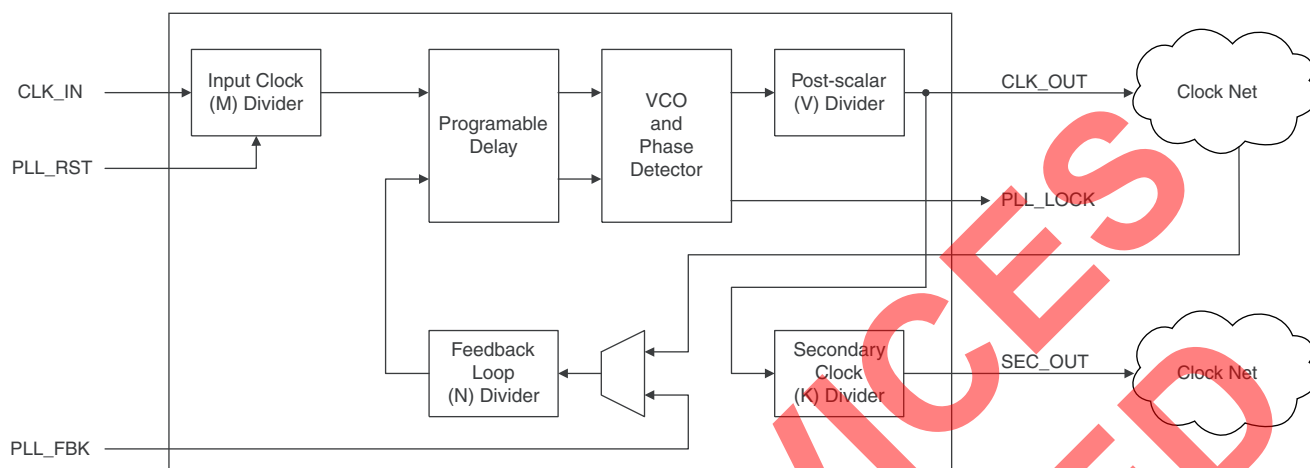
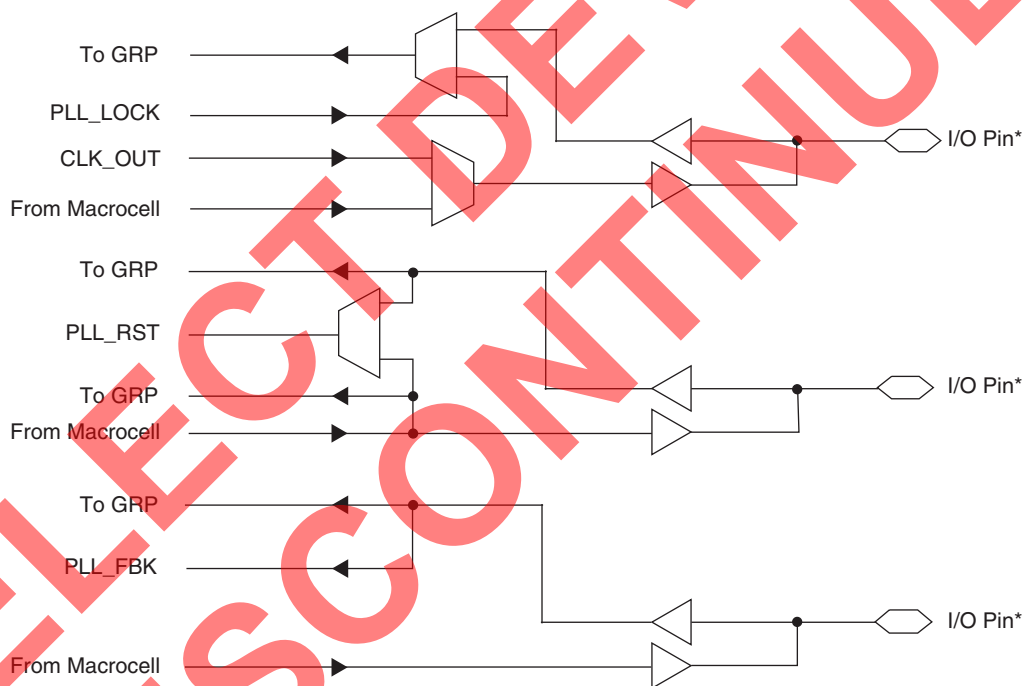


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Figure 15. PLL Block Diagram**Figure 16. Connection of Optional PLL Inputs and Outputs**

*See pinout table for details

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, [sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices](#).

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CAMWMSKS}	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMWMSKH}	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMRSTO}	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
t _{CAMRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
t _{CAMRSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
CAM – Compare Mode													
t _{CAMDATAS}	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
t _{CAMDATAH}	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMENMSKS}	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{CAMENMSKH}	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{CAMCASC}	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—	0.51	ns
t _{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—	9.63	ns
t _{CAMMATCH}	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—	10.22	ns
t _{CAMMMATCH}	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—	7.72	ns
t _{CAMRSTFLAG}	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—	4.11	ns
Single Port RAM													
t _{SPADDDATA}	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	7.76	ns
t _{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80	—	ns
t _{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
t _{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPDATAS}	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t _{SPDATAH}	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	9.86	ns
t _{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t _{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
t _{SPRSTPW}	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns
Pseudo Dual Port RAM													
t _{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPRCES}	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
t _{PDPRC EH}	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{PDPWCES}	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43	—	ns
t _{PDPWCEH}	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
t _{PDPRA DDS}	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPRA DDH}	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDPWADDS}	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t _{PDPWADDH}	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t _{PDP RWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

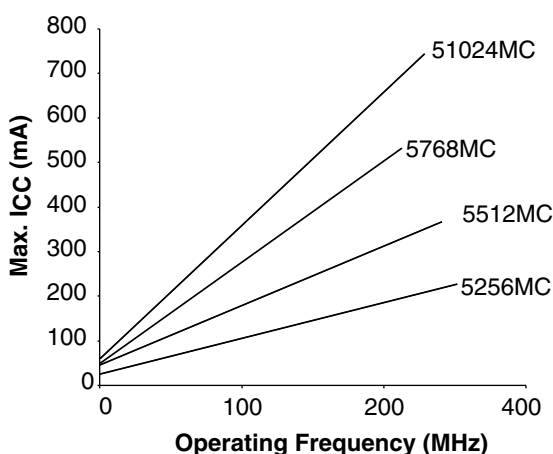
Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

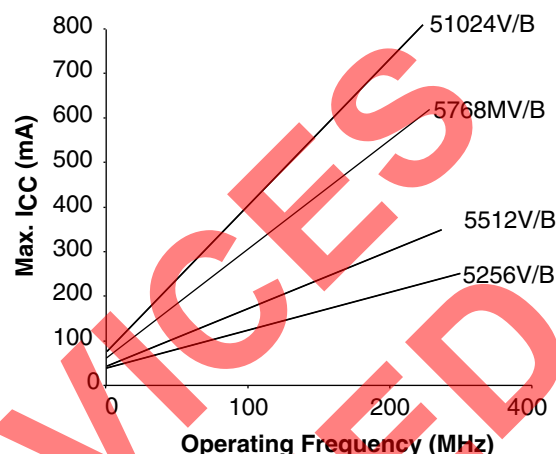
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – [Power Estimation in ispXPLD 5000MX Devices](#).

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input ($\mu\text{A}/\text{MHz}$)
- K1 = Current per Product Term ($\mu\text{A}/\text{MHz}$)
- K2 = Current per GRP from MFB ($\mu\text{A}/\text{MHz}$)
- K3 = Current per GRP from I/O ($\mu\text{A}/\text{MHz}$)
- K4 = Global clock tree current ($\mu\text{A}/\text{MHz}$)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder ($\mu\text{A}/\text{MHz}$)
- K11 = Current per column driver ($\mu\text{A}/\text{MHz}$)

Signals	208 PQFP ⁴	256 fpBGA ^{3,5}	484 fpBGA, 5 ³	672 fpBGA ^{3,5}
VCC	10, 49, 76, 114, 153, 180	D4, D13, F6, F11, L6, L11, N4, N13	A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4	AA21, AA6, F21, F6, G20, G7, J13, J14, K13, K14, L13, L14, M13, M14, N10, N11, N12, N15, N16, N17, N18, N9, P10, P11, P12, P15, P16, P17, P18, P9, R13, R14, T13, T14, U13, U14, V13, V14, Y20, Y7
VCCO0	5, 17, 189, 204	A1, F7, G6	B9, C3, G8, G9, H7, J2, J7, P4	H10, H11, H8, H9, J8, J9, K8, L8, M8, N8
VCCO1	42, 57, 72	K6, L7, T1	AA9, R7, T3, T8, Y3	P8, R8, T8, U8, V8, W9, W10, W11, W8, W9
VCCO2	85, 100, 107, 121	K11, L10, T16	AA14, R16, T15, T20, Y20	P19, R19, T19, U19, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19
VCCO3	146, 161, 176	A16, F10, G11	B14, C20, G14, G15, H16, J16, J21, P19	H12, H13, H14, H15, H16, H17, H18, H19, J18, J19, K19, L19, M19, N19
VCCP	136	J16	M22	N25
VCCJ	27	J1	M1	N4
GND	15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174	K1, C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3	N1, A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8	A11, A16, A2, A25, AE1, AE2, AE25, AE26, AF11, AF16, AF2, AF25, B1, B2, B25, B26, J10, J11, J12, J15, J16, J17, K10, K11, K12, K15, K16, K17, K18, K9, L1, L10, L11, L12, L15, L16, L17, L18, L26, L9, M10, M11, M12, M15, M16, M17, M18, M9, N13, N14, P13, P14, R10, R11, R12, R15, R16, R17, R18, R9, T1, T10, T11, T12, T15, T16, T17, T18, T26, T9, U10, U11, U12, U15, U16, U17, U18, U9, V10, V11, V12, V15, V16, V17
GNDP	134	K16	N22	P26
NC ²	—	5256MX: A2, A11, A12, A15, B2, B12, B15, B16, C4, C12, C15, C16, D1, D11, D14, D15, D16, E1, E4, E10, E11, E13, E14, F4, F5, F12, F13, L1, L4, M3, M7, M13, N2, N6, P1, P2, P5, P6, P13, P14, P15, P16, R1, R2, R4, R5, R6, R16, T2, T3, T4, T5, T6 5512MX/5768MX: L1	5512MX: P1, AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6 5768MX/51024MX: None	A12, A13, A14, A15, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA7, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AD11, AD12, AD13, AD14, AD15, AD16, AE11, AE12, AE13, AE14, AE15, AE16, AF12, AF13, AF14, AF15, B11, B12, B13, B14, B15, B16, C11, C12, C13, C14, C15, C16, C3, D10, D11, D12, D13, D14, D15, D16, D17, E10, E11, E12, E13, E14, E15, E16, E17, E6, E7, E8, F10, F11, F12, F13, F14, F15, F16, F17, G10, G11, G12, G13, G14, G15, G16, G17, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17

1. All grounds must be electrically connected at the board level.

2. NC pins should not be connected to any active signals, V_{CC} or GND.

3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

4. Pin orientation follows the conventional counter-clockwise order from pin 1 marking of the topside view.

5. Internal GNDs and I/O GNDs (Bank 0 - Bank 3) are connected inside package. V_{CCO} balls connect to four power planes within the package, one each for V_{CCOx}.

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
1	4N	A16/CSB	A9	B9	A17	L5
1	5P	A18/READ	A10	B10	A19	N1
1	5N	A20/CCLK	A11	B11	A21	M2
-	-	VCC	-	-	-	VCC
-	-	DONE	-	-	-	M4
1	6P	A22	A12	B12	A23	N3
1	6N	A24	A13	B13	A25	P4
1	7P	A26	A14	B14	A27	N5
1	7N	A28	A15	B15	A29	M6
-	-	PROGRAMB	-	-	-	R3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
-	-	VCCO1	-	-	-	VCCO1
-	-	CFG0	-	-	-	L8
1	8P	B2	A16	B16	B3	T7
1	8N	B4	A17	B17	-	R7
1	9P	B5	A18	B18	-	N7
1	9N	B6	A19	B19	B7	P7
1	10P	B8	A20	B20	B9	T8
1	10N	B10	A21	B21	B11	R8
1	11P	B12	A22	B22	B13	M8
1	11N	B14	A23	B23	B15	P8
1	-	B16/VREF1	-	-	B17	L9
1	12P	B18	A24	B24	B19	N8
1	12N	B20	A25	B25	-	M9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	13P	B21	A26	B26	-	N10
-	-	VCCO1	-	-	-	VCCO1
1	13N	B22	A27	B27	B23	T9
1	14P	B24	A28	B28	B25	T10
1	14N	B26	A29	B29	B27	R9
-	-	VCC	-	-	-	VCC
1	15P	B28	A30	B30	B29	P9
1	15N	B30	A31	B31	B31	N9
2	16P	C0	C0	D0	C1	T11
2	16N	C2	C1	D1	C3	T12
2	17P	C4	C2	D2	-	P10
2	17N	C5	C3	D3	-	R10
2	18P	C6	C4	D4	C7	R11
-	-	VCCO2	-	-	-	VCCO2
2	18N	C8	C5	D5	C9	M10
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	19P	C10	C6	D6	C11	M11
2	19N	C12	C7	D7	C13	T13

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V _{CCO1}	—	—	—	57	V _{CCO1}	V _{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7 ¹	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V _{CCO1}	—	—	—	—	V _{CCO1}	V _{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V _{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	V _{CCO1}	—	—	—	72	V _{CCO1}	V _{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	96N	M12	M23	O23	M13	196	B5	A10
0	96P	M10	M22	O22	M11	197	A3	A9
0	97N	M8	M21	O21	M9	198	B4	C9
0	97P	M6	M20	O20	M7	199	B3	D9
0	98N	M5	M19	O19	—	200	C5	F9
0	98P	M4	M18	O18	—	201	C6	E9
0	99N	M2	M1	O1	M3	202	D5	A8
—	—	V _{CC00}	—	—	—	—	V _{CC00}	V _{CC00}
0	99P	M0	M0	O0	M1	203	D6	B8
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	100N	N30	O29	—	N31	—	—	A7
0	100P	N28	O28	—	N29	—	—	B7
0	101N	N26	O27	—	N27	—	—	A5
0	101P	N24	O26	—	N25	—	—	B5
0	102N	N22	O25	—	N23	—	—	B6
0	102P	N21	O24	—	—	—	—	C7
0	103N	N20	O23	—	—	—	—	E8
0	103P	N18	O22	—	N19	—	—	E7
0	104N	N16	O21	—	N17	—	—	E6
0	104P	N14	O20	—	N15	—	—	D6
0	105N	N12	O19	—	N13	—	—	D8
—	—	V _{CC00}	—	—	—	204	V _{CC00}	V _{CC00}
0	105P	N10	O18	—	N11	—	—	F8
—	—	GND (Bank 0)	—	—	—	205	GND (Bank 0)	GND (Bank 0)
0	106N	N8	O17	—	N9	—	—	F7
0	106P	N6	O16	—	N7	—	—	D7
0	107N	N5	O15	—	—	206	A2	C6
0	107P	N4	O14	—	—	207	B2	C5
0	108N	N2	O13	—	N3	—	—	C4
0	108P	N0	O12	—	N1	—	—	D5

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	J6	T1
-	-	TDO	-	-	-	K2	V1
1	0P	A30/DATA0	C0	A0	A31	K3	W1
1	0N	A28/DATA1	C1	A1	A29	J3	Y1
1	1P	A26/DATA2	C2	A2	A27	J5	P3
1	1N	A24/DATA3	C3	A3	A25	J4	R3
1	2P	A22/DATA4	C4	A4	A23	L2	T2
1	2N	A20/DATA5	C5	A5	A21	M1	U2
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18/DATA6	C6	A6	A19	K4	V2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16/DATA7	C7	A7	A17	L3	W2
-	-	GND	-	-	-	GND	GND
1	4P	A14/INITB	C8	A8	A15	K5	R4
1	4N	A12/CSB	C9	A9	A13	L5	T4
1	5P	A10/READ	C10	A10	A11	N1	R6
1	5N	A8/CCLK	C11	A11	A9	M2	R5
1	6P	A6	-	-	A7	—	U3
-	-	VCC	-	-	-	VCC	VCC
1	6N	A4	-	-	A5	P1	V3
1	7P	A2	-	-	A3	M3	Y2
1	7N	A0	-	-	A1	L4	W3
1	8P	B30	D0	-	B31	N2	U5
1	8N	B28	D2	-	B29	P2	T5
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	9P	B26	D4	-	B27	R1	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	9N	B24	D6	-	B25	R2	V4
1	10P	B22	D8	-	B23	T2	AA3
1	10N	B20	D10	-	B21	T3	AB3
1	-	B18	D12	-	B19	—	Y4
-	-	DONE	-	-	-	M4	AA4
1	11P	B14	-	-	B15	—	AB2
1	11N	B12	-	-	B13	—	U6
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	12P	B10	-	-	B11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	12N	B8	-	-	B9	—	W6
1	13P	B6	C12	A12	B7	N3	AB4
1	13N	B4	C13	A13	B5	P4	AB5
1	14P	B2	C14	A14	B3	N5	T6
1	14N	B0	C15	A15	B1	M6	U7
-	-	PROGRAMB	-	-	-	R3	W5

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	79N	N10	P5	N5	N11	—	V26
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	80P	N12	P6	N6	N13	—	V22
2	80N	N14	P7	N7	N15	—	V23
2	81P	N16	P8	N8	N17	—	V24
2	81N	N18	P9	N9	N19	—	V25
2	82P	N20	P10	N10	N21	—	U20
2	82N	N22	P11	N11	N23	—	T20
2	83P	N24	P12	N12	N25	—	U26
2	83N	N26	P13	N13	N27	—	U25
2	84P	N28	P14	N14	N29	—	U21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	84N	N30	P15	N15	N31	—	T21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	85P	P0	P16	N16	P1	—	U22
2	85N	P2	P17	N17	P3	—	U23
2	86P	P4	P18	N18	P5	—	U24
2	86N	P6	P19	N19	P7	—	T24
2	87P	P8	P20	N20	P9	—	T23
2	87N	P10	P21	N21	P11	—	T22
2	88P	P12	P22	N22	P13	—	T25
-	-	VCC	-	-	-	VCC	VCC
2	88N	P14	P23	N23	P15	—	R26
-	-	GND	-	-	-	GND	GND
2	89P	P16	P24	N24	P17	—	R25
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	89N	P18	P25	N25	P19	—	R24
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	90P	P20	P26	N26	P21	—	R21
2	90N	P22	P27	N27	P23	—	P21
2	91P	P24	P28	N28	P25	—	R22
2	91N	P26	P29	N29	P27	—	R23
2	92P	P28	P30	N30	P29	—	R20
2	92N	P30	P31	N31	P31	—	P20
-	-	TOE	-	-	-	W22	P25
-	-	RESET	-	-	-	V22	P24
-	-	GOE0	-	-	-	T22	P23
-	-	GOE1	-	-	-	R22	P22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3N	GCLK2	-	-	-	P16	N26
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	