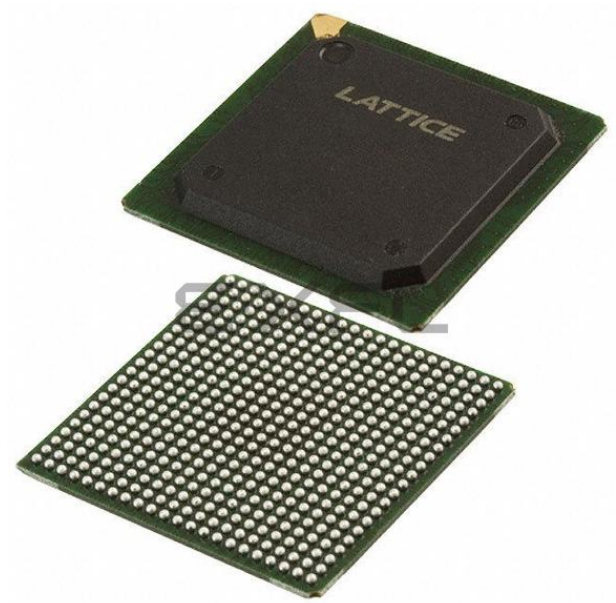
Lattice Semiconductor Corporation - LC5512MV-75FN484C Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	253
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75fn484c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC51024MV	LC51024MV-52F484C	Active / Orderable	
	LC51024MV-52FN484C		
	LC51024MV-75F484C		
	LC51024MV-75FN484C		
	LC51024MV-75F484I		
	LC51024MV-75FN484I		
	LC51024MV-52F672C		
	LC51024MV-52FN672C		
	LC51024MV-75F672C		
	LC51024MV-75FN672C		
	LC51024MV-75F672I		
	LC51024MV-75FN672I		
LC51024MB	LC51024MB-52F484C	**Discontinued**	PCN#09-10
	LC51024MB-52FN484C		
	LC51024MB-75F484C		
	LC51024MB-75FN484C		
	LC51024MB-75F484I		
	LC51024MB-75FN484I		
	LC51024MB-52F672C		
	LC51024MB-52FN672C		
	LC51024MB-75F672C		
	LC51024MB-75FN672C		
	LC51024MB-75F672I		
	LC51024MB-75FN672I		
LC51024MC	LC51024MC-52F484C	**Discontinued**	PCN#09-10
	LC51024MC-52FN484C		
	LC51024MC-75F484C		
	LC51024MC-75FN484C		
	LC51024MC-75F484I		
	LC51024MC-75FN484I		
	LC51024MC-52F672C		
	LC51024MC-52FN672C		
	LC51024MC-75F672C		
	LC51024MC-75FN672C		
	LC51024MC-75F672I		
	LC51024MC-75FN672I		

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

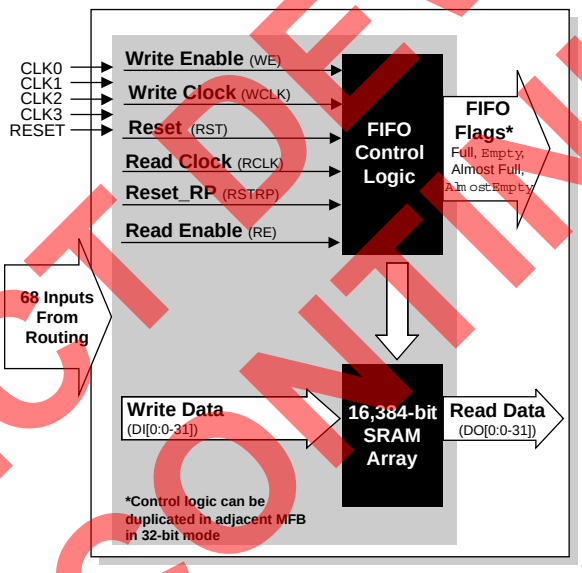


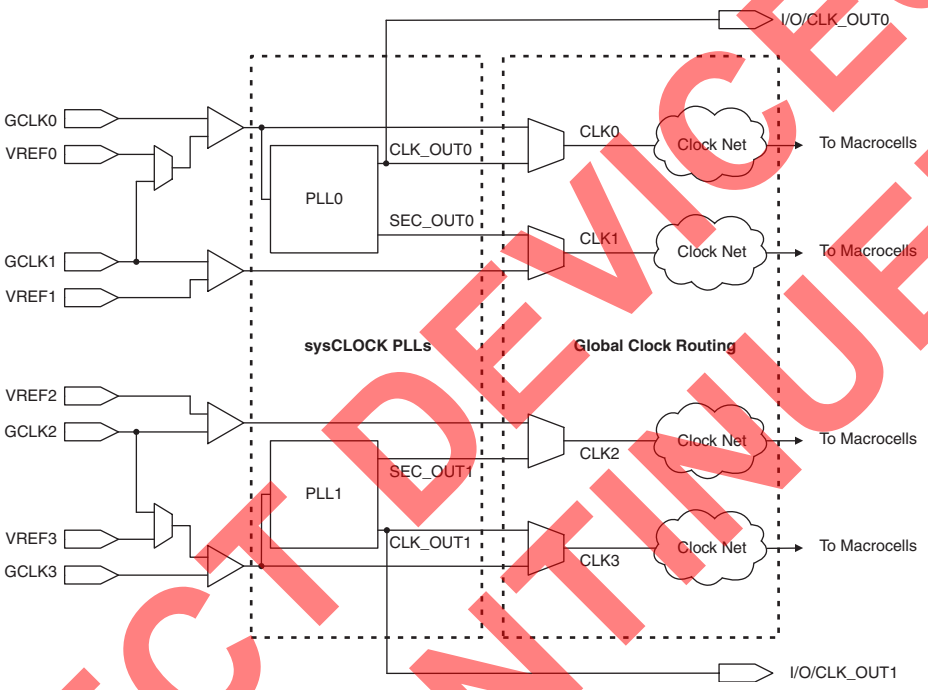
Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Figure 15. PLL Block Diagram

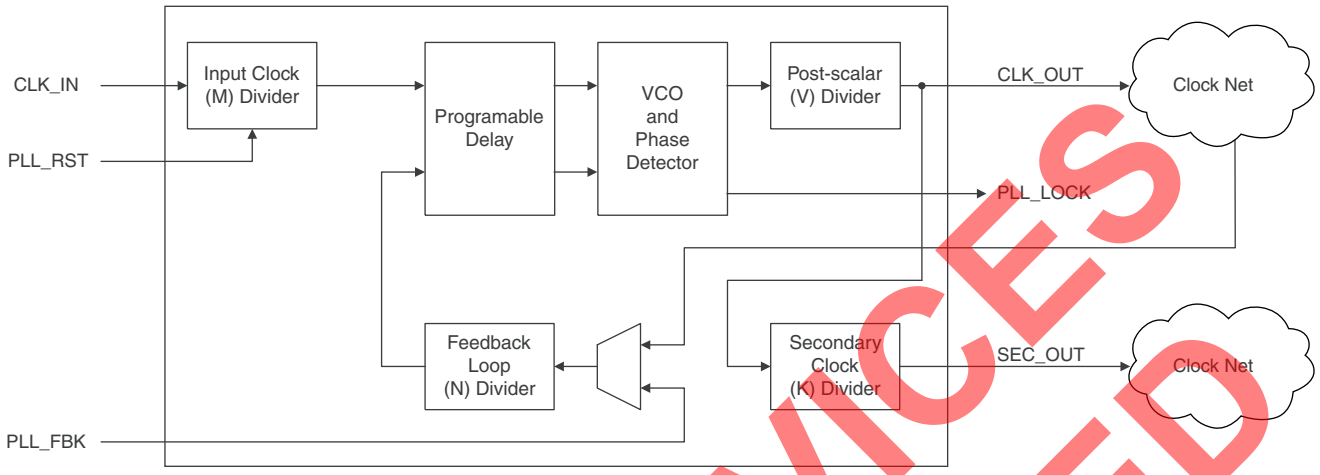
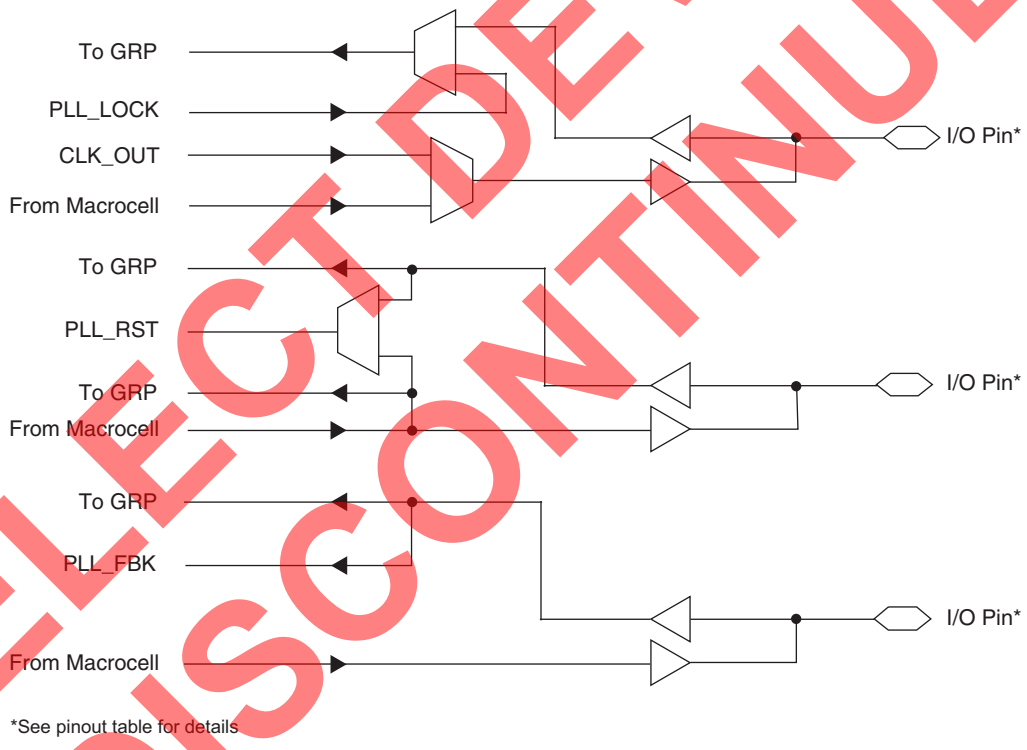


Figure 16. Connection of Optional PLL Inputs and Outputs



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

ispXPLD 5000MX Family External Switching Characteristics [1, 2, 3]

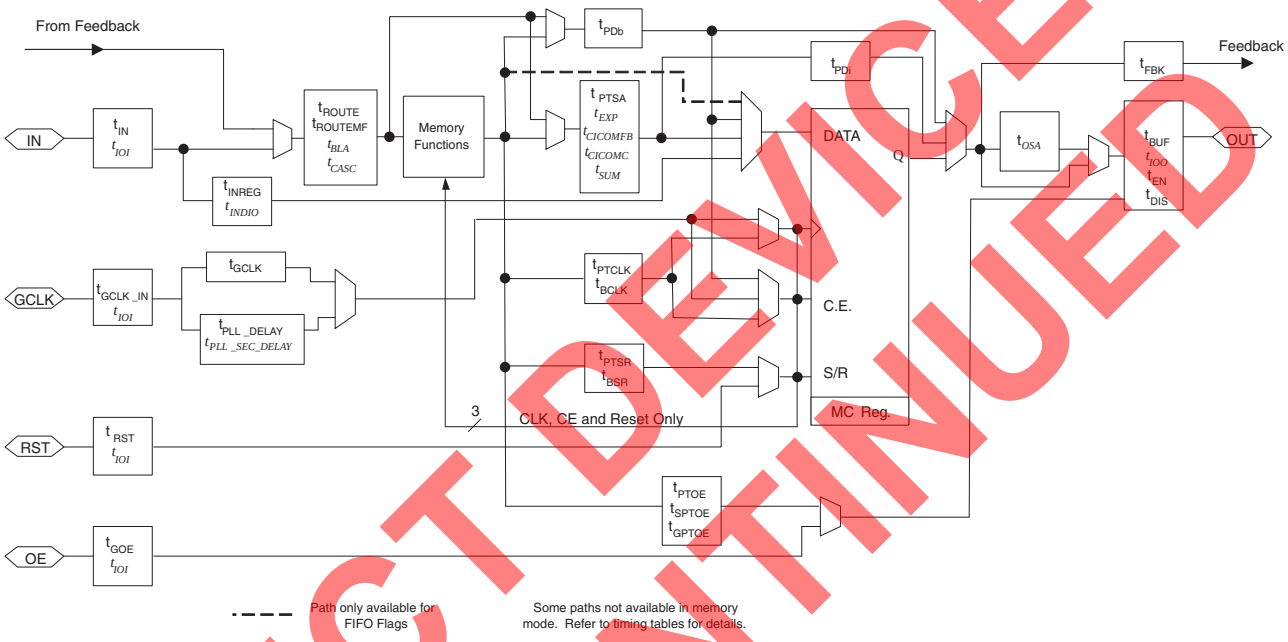
Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	9.5	ns
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	—	ns
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	—	ns
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	—	ns
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	—	ns
t_{CO}	MFB Register Clock-to-Output Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	5.0	ns
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	7.5	ns
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	10.5	ns
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	7.5	ns
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	1.0	ns
f_{MAX} [4]	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	150	MHz
f_{MAX} (Ext.)	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	105	MHz
f_{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	200	MHz
f_{MAX} (CAMC)[5]	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	168	MHz
f_{MAX} (CAM)[5]	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	90	MHz

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—	8.54	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
Dual Port RAM													
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84	—	ns
t_{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDAS}$	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDAH}$	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATAAS}$	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATAAH}$	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DPCEBS}	Clock Enable B Setup before Clock B Time	—	2.33	—	2.33	—	2.33	—	2.33	—	3.03	—	ns
t_{DPCEBH}	Clock Enable Hold B after Clock B Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDBS}$	Address B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDBH}$	Address B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWBS}	R/W B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWBH}	R/W B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATABS}$	Write Data B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATABH}$	Write Data B Hold after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	5.97	—	5.92	—	5.86	—	5.65	—	9.86	ns
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	5.16	—	5.16	—	5.16	—	5.16	—	6.71	ns
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.40	—	1.40	—	1.83	—	ns
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns

Timing v.1.8

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IOI} Input Adjusters													
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t_{IOO} Output Adjusters – Output Signal Modifiers													
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t_{IOO} Output Adjusters – Output Configurations													
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

Power Estimation Equations

ICC = ICC_DC + IMFB_CPLD + IMFB_ SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL_D

ICC_DC
Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) from the data sheet.

IMFB_CPLD
= ((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** * CPLD GRP from IFB) * AF+ **K4**) * FREQ / 1000µA/mA

IMFB_CAM
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

IMFB_ SRAM/PDPRAM/FIFO
= (WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (**K1** + 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * SRAM/PDPRAM/FIFO Memory MFBs * FREQ / 1000µA/mA

IMFB_ DPRAM
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs * FREQ / 1000µA/mA

IPLL_D
= **K5** * PLL_FREQ * number of PLLs used. IPPL_D is the PLL digital component of the VCC supply current.

Analog portion of PLL supply current consumption, from PLL power pin:

IPLL_A = (**K6** * PLL_FREQ + **K7**) * number of PLLs used

Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPLD 5256MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
0	61N	H30	G17	H17	H31	B1
0	61P	H28	G16	H16	H29	C1
0	62N	H26	G15	H15	H27	D3
0	62P	H24	G14	H14	H25	C2
0	63N	H22	G13	H13	H23	E3
0	63P	H21	G12	H12	-	D2
-	-	VCC	-	-	-	VCC
0	64N	H20	G11	H11	-	E2
0	64P	H18/CLK_OUT0	G10	H10	H19	F2
0	65N	H16	G9	H9	H17	F1
0	65P	H14	G8	H8	H15	G1
-	-	GND	-	-	-	GND
0	66N	H12	G7	H7	H13	F3
-	-	VCCO0	-	-	-	VCCO0
0	66P	H10	G6	H6	H11	G5
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	67N	H8	G5	H5	H9	H5
0	67P	H6/PLL_RST0	G4	H4	H7	G4
0	68N	H5	-	-	-	G3
0	68P	H4/PLL_FBK0	-	-	-	H3
0	69N	H2	-	-	H3	G2
0	69P	H0	-	-	H1	H1
-	GCLK0P	GCLK0	-	-	-	H2
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table
-	GCLK0N	GCLK1	-	-	-	J2
-	-	GND	-	-	-	GND
-	-	TDI	-	-	-	H6
-	-	TMS	-	-	-	H4
-	-	TCK	-	-	-	J6
-	-	TDO	-	-	-	K2
1	0P	A0/DATA0	A0	B0	A1	K3
1	0N	A2/DATA1	A1	B1	A3	J3
1	1P	A4/DATA2	A2	B2	-	J5
1	1N	A5/DATA3	A3	B3	-	J4
1	2P	A6/DATA4	A4	B4	A7	L2
1	2N	A8/DATA5	A5	B5	A9	M1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	3P	A10/DATA6	A6	B6	A11	K4
-	-	VCCO1	-	-	-	VCCO1
1	3N	A12/DATA7	A7	B7	A13	L3
-	-	GND	-	-	-	GND
1	4P	A14/INITB	A8	B8	A15	K5

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
2	20P	C14	-	-	C15	P11
2	20N	C16/VREF2	-	-	C17	T14
2	21P	C18	C8	D8	C19	R12
2	21N	C20	C9	D9	-	R13
2	22P	C21	C10	D10	-	N11
2	22N	C22	C11	D11	C23	T15
2	23P	C24	C12	D12	C25	R14
2	23N	C26	C13	D13	C27	N12
2	24P	C28	C14	D14	C29	P12
2	24N	C30	C15	D15	C31	R15
-	-	VCCO2	-	-	-	VCCO2
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	25P	D0	-	-	D1	N15
2	25N	D2	-	-	D3	N14
2	26P	D4	C16	D16	-	N16
2	26N	D5	C17	D17	-	M16
2	27P	D6	C18	D18	D7	M14
2	27N	D8	C19	D19	D9	M15
-	-	VCC	-	-	-	VCC
2	28P	D10	C20	D20	D11	L13
2	28N	D12	C21	D21	D13	L12
2	29P	D14	C22	D22	D15	L15
2	29N	D16	C23	D23	D17	L16
-	-	GND	-	-	-	GND
2	30P	D18	C24	D24	D19	L14
-	-	VCCO2	-	-	-	VCCO2
2	30N	D20	C25	D25	-	K15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	31P	D21	C26	D26	-	K14
2	31N	D22	C27	D27	D23	K12
2	32P	D24	C28	D28	D25	K13
2	32N	D26	C29	D29	D27	J13
2	33P	D28	C30	D30	D29	J14
2	33N	D30	C31	D31	D31	J12
-	-	TOE	-	-	-	J15
-	-	RESET	-	-	-	J11
-	-	GOE0	-	-	-	H11
-	-	GOE1	-	-	-	H13
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3N	GCLK2	-	-	-	H15
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3P	GCLK3	-	-	-	H16

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7[1]	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	143N	U22	U27	W27	U23	—	K6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	U20	U26	W26	U21	—	K3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	U18	U25	W25	U19	—	K5
0	144P	U16	U24	W24	U17	—	K2
0	145N	U14	U23	W23	U15	—	L5
0	145P	U12	U22	W22	U13	—	K1
0	146N	U10	U21	W21	U11	—	L6
0	146P	U8	U20	W20	U9	—	L1
0	147N	U6	U19	W19	U7	—	M5
0	147P	U4	U18	W18	U5	—	L2
0	148N	U2	U17	W17	U3	—	N5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	148P	U0	U16	W16	U1	—	L3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	149N	W30	U15	W15	W31	—	M6
0	149P	W28	U14	W14	W29	—	M2
0	150N	W26	U13	W13	W27	—	P5
-	-	VCC	-	-	-	VCC	VCC
0	150P	W24	U12	W12	W25	—	P6
0	151N	W22	U11	W11	W23	—	M3
0	151P	W20	U10	W10	W21	—	N6
0	152N	W18	U9	W9	W19	—	N2
0	152P	W16	U8	W8	W17	—	P1
-	-	GND	-	-	-	GND	GND
0	153N	W14	U7	W7	W15	—	N3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	153P	W12	U6	W6	W13	—	M8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	154N	W10	U5	W5	W11	—	N8
0	154P	W8	U4	W4	-	—	P2
0	155N	W6	U3	W3	W7	—	P8
0	155P	W4	U2	W2	W5	—	N4
0	156N	W2	U1	W1	W3	G2	H1
0	156P	W0	U0	W0	W1	H1	J1
-	GCLK0P	GCLK0	-	-	-	H2	N7
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	J2	P7
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	H6	R1
-	-	TMS	-	-	-	H4	R2

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	J6	T1
-	-	TDO	-	-	-	K2	V1
1	0P	A30/DATA0	C0	A0	A31	K3	W1
1	0N	A28/DATA1	C1	A1	A29	J3	Y1
1	1P	A26/DATA2	C2	A2	A27	J5	P3
1	1N	A24/DATA3	C3	A3	A25	J4	R3
1	2P	A22/DATA4	C4	A4	A23	L2	T2
1	2N	A20/DATA5	C5	A5	A21	M1	U2
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18/DATA6	C6	A6	A19	K4	V2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16/DATA7	C7	A7	A17	L3	W2
-	-	GND	-	-	-	GND	GND
1	4P	A14/INITB	C8	A8	A15	K5	R4
1	4N	A12/CSB	C9	A9	A13	L5	T4
1	5P	A10/READ	C10	A10	A11	N1	R6
1	5N	A8/CCLK	C11	A11	A9	M2	R5
1	6P	A6	-	-	A7	—	U3
-	-	VCC	-	-	-	VCC	VCC
1	6N	A4	-	-	A5	P1	V3
1	7P	A2	-	-	A3	M3	Y2
1	7N	A0	-	-	A1	L4	W3
1	8P	B30	D0	-	B31	N2	U5
1	8N	B28	D2	-	B29	P2	T5
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	9P	B26	D4	-	B27	R1	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	9N	B24	D6	-	B25	R2	V4
1	10P	B22	D8	-	B23	T2	AA3
1	10N	B20	D10	-	B21	T3	AB3
1	-	B18	D12	-	B19	—	Y4
-	-	DONE	-	-	-	M4	AA4
1	11P	B14	-	-	B15	—	AB2
1	11N	B12	-	-	B13	—	U6
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	12P	B10	-	-	B11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	12N	B8	-	-	B9	—	W6
1	13P	B6	C12	A12	B7	N3	AB4
1	13N	B4	C13	A13	B5	P4	AB5
1	14P	B2	C14	A14	B3	N5	T6
1	14N	B0	C15	A15	B1	M6	U7
-	-	PROGRAMB	-	-	-	R3	W5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	T1	P3
-	-	TDO	-	-	-	V1	P2
1	0P	A30	A0	C0	A31	—	P1
1	0N	A28	A1	C1	A29	—	R1
1	1P	A26	A2	C2	A27	—	P6
1	1N	A24	A3	C3	A25	—	R6
1	2P	A22	A4	C4	A23	—	P7
1	2N	A20	A5	C5	A21	—	R7
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18	A6	C6	A19	—	R4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16	A7	C7	A17	—	R5
-	-	GND	-	-	-	GND	GND
1	4P	A14	A8	C8	A15	—	R3
-	-	VCC	-	-	-	VCC	VCC
1	4N	A12	A9	C9	A13	—	R2
1	5P	A10	A10	C10	A11	—	T2
1	5N	A8	A11	C11	A9	—	T3
1	6P	A6	A12	C12	A7	—	T4
1	6N	A4	A13	C13	A5	—	T5
1	7P	A2	A14	C14	A3	—	U2
1	7N	A0	A15	C15	A1	—	U3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	8P	C30	A16	C16	C31	—	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	8N	C28	A17	C17	C29	—	U5
1	9P	C26	A18	C18	C27	—	T6
1	9N	C24	A19	C19	C25	—	U6
1	10P	C22	A20	C20	C23	—	T7
1	10N	C20	A21	C21	C21	—	U7
1	11P	C18	A22	C22	C19	—	U1
1	11N	C16	A23	C23	C17	—	V1
1	12P	C14	A24	C24	C15	—	V2
1	12N	C12	A25	C25	C13	—	V3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	13P	C10	A26	C26	C11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	13N	C8	A27	C27	C9	—	V4
-	-	GND	-	-	-	GND	GND
1	14P	C6	A28	C28	C7	—	W2
-	-	VCC	-	-	-	VCC	VCC
1	14N	C4	A29	C29	C5	—	W3
1	15P	C2	A30	C30	C3	—	W4

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	79N	N10	P5	N5	N11	—	V26
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	80P	N12	P6	N6	N13	—	V22
2	80N	N14	P7	N7	N15	—	V23
2	81P	N16	P8	N8	N17	—	V24
2	81N	N18	P9	N9	N19	—	V25
2	82P	N20	P10	N10	N21	—	U20
2	82N	N22	P11	N11	N23	—	T20
2	83P	N24	P12	N12	N25	—	U26
2	83N	N26	P13	N13	N27	—	U25
2	84P	N28	P14	N14	N29	—	U21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	84N	N30	P15	N15	N31	—	T21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	85P	P0	P16	N16	P1	—	U22
2	85N	P2	P17	N17	P3	—	U23
2	86P	P4	P18	N18	P5	—	U24
2	86N	P6	P19	N19	P7	—	T24
2	87P	P8	P20	N20	P9	—	T23
2	87N	P10	P21	N21	P11	—	T22
2	88P	P12	P22	N22	P13	—	T25
-	-	VCC	-	-	-	VCC	VCC
2	88N	P14	P23	N23	P15	—	R26
-	-	GND	-	-	-	GND	GND
2	89P	P16	P24	N24	P17	—	R25
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	89N	P18	P25	N25	P19	—	R24
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	90P	P20	P26	N26	P21	—	R21
2	90N	P22	P27	N27	P23	—	P21
2	91P	P24	P28	N28	P25	—	R22
2	91N	P26	P29	N29	P27	—	R23
2	92P	P28	P30	N30	P29	—	R20
2	92N	P30	P31	N31	P31	—	P20
-	-	TOE	-	-	-	W22	P25
-	-	RESET	-	-	-	V22	P24
-	-	GOE0	-	-	-	T22	P23
-	-	GOE1	-	-	-	R22	P22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3N	GCLK2	-	-	-	P16	N26
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	126N	W4	V11	U21	W5	B18	E19
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	126P	W6	V10	U20	W7	A18	E18
-	-	GND	-	-	-	GND	GND
3	127N	W8	V9	U18	W9	C17	C24
-	-	VCC	-	-	-	VCC	VCC
3	127P	W10	V8	U16	W11	B17	C23
3	128N	W12	V7	U12	W13	C16	D22
3	128P	W14	V6	U10	W15	B16	D21
3	129N	W16	V5	U8	W17	F13	E21
3	129P	W18	V4	U6	W19	F15	D20
3	130N	W20	V3	U5	W21	D16	D19
3	130P	W22	V2	U4	W23	E16	D18
3	131N	W24	V1	U2	W25	A16	C22
3	131P	W26	V0	U0	W27	A15	C21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	132N	W28	X15	V15	W29	B15	C20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	132P	W30	X14	V14	W31	A14	C19
3	133N	X0	X13	V13	X1	D15	C18
3	133P	X2	X12	V12	X3	E15	C17
3	134N	X4	X11	V11	X5	D14	B24
3	134P	X6	X10	V10	X7	F14	B23
3	135N	X8	X9	V9	X9	A13	B22
3	135P	X10	X8	V8	X11	B13	B21
3	136N	X12/VREF3	X29	V29	X13	C14	B20
3	136P	X14	X28	V28	X15	E14	B19
3	137N	X16	X7	V7	X17	E13	B18
3	137P	X18	X6	V6	X19	F12	B17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	138N	X20	X5	V5	X21	D13	A24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	138P	X22	X4	V4	X23	C13	A23
3	139N	X24	X3	V3	X25	E12	A22
-	-	GND	-	-	-	GND	GND
3	139P	X26	X2	V2	X27	C12	A21
-	-	VCC	-	-	-	VCC	VCC
3	140N	X28	X1	V1	X29	B12	A20
3	140P	X30	X0	V0	X31	A12	A19
0	141N	Y30	Y31	AA31	Y31	E11	A18
-	-	VCC	-	-	-	VCC	VCC
0	141P	Y28	Y30	AA30	Y29	C11	A17
-	-	GND	-	-	-	GND	GND

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193	I
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193	C
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193	C
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317	C
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193	I
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I