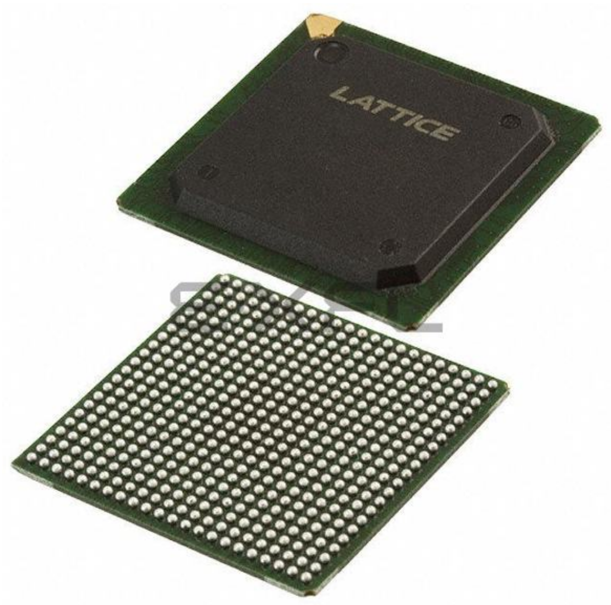

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	253
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75fn484i

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

Figure 3. MFB in SuperWIDE Logic Mode†

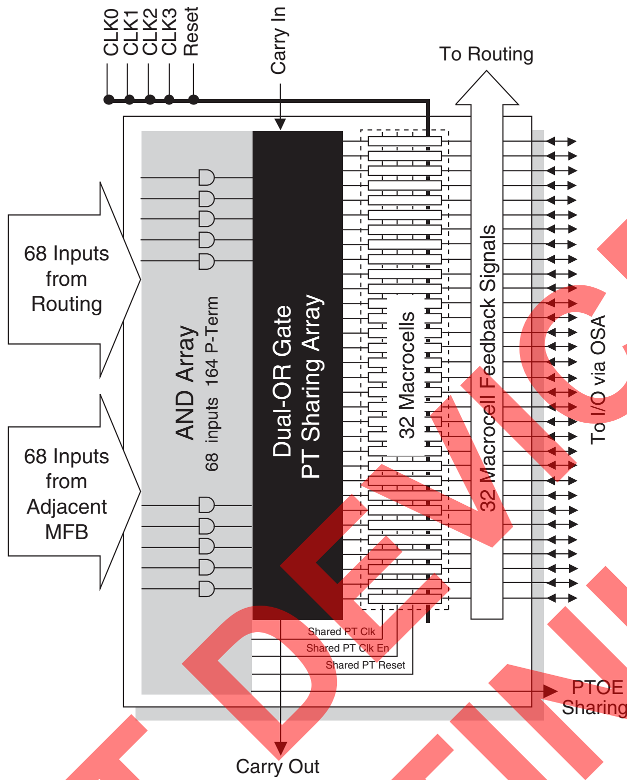
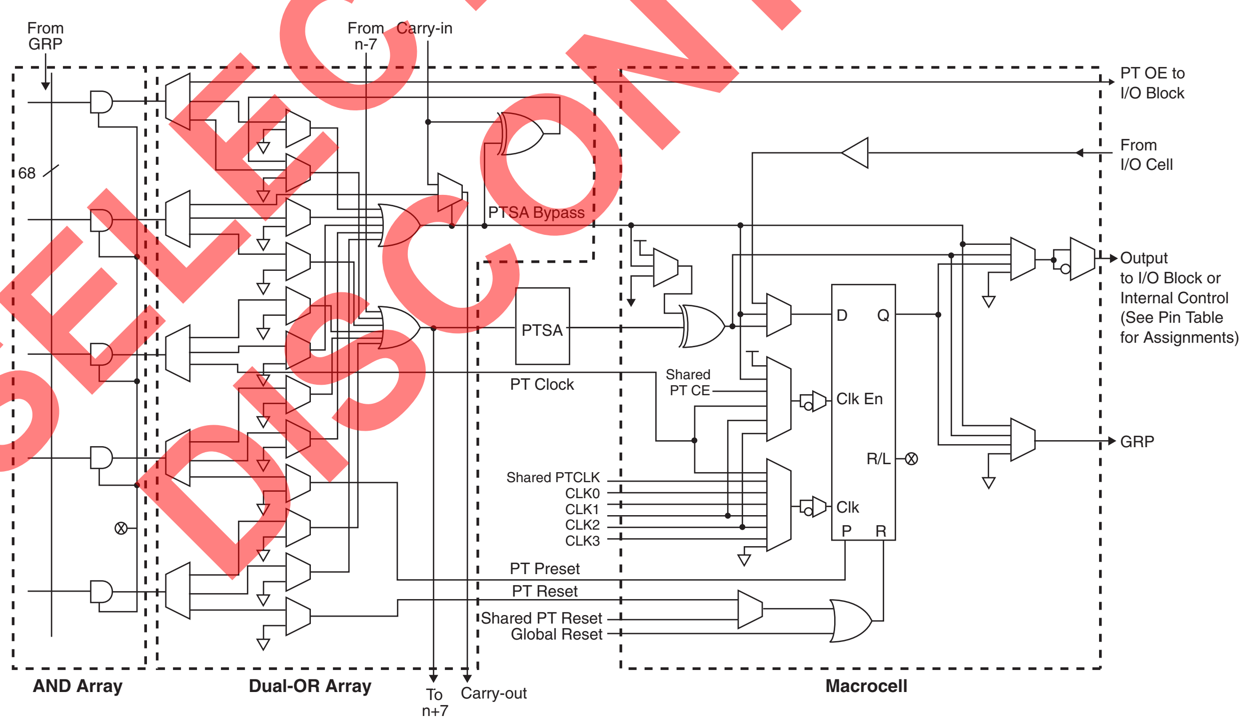


Figure 4. Macrocell Slice in Logic Mode AND-Array



Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

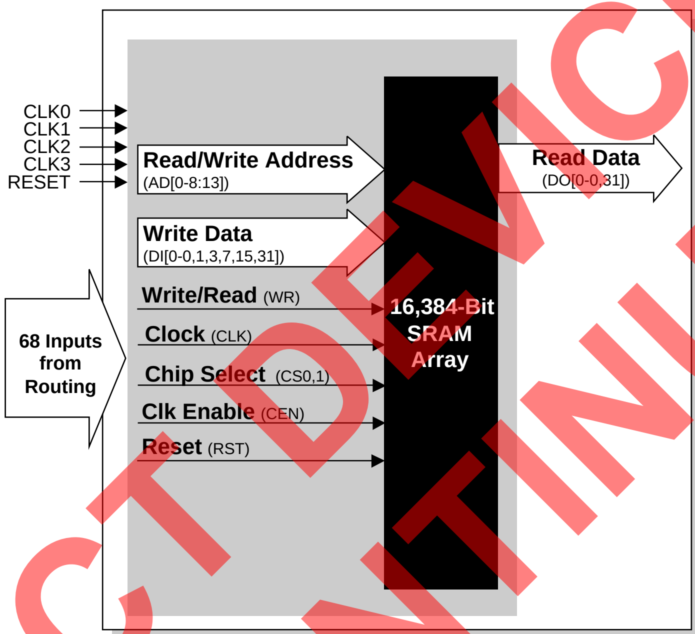


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

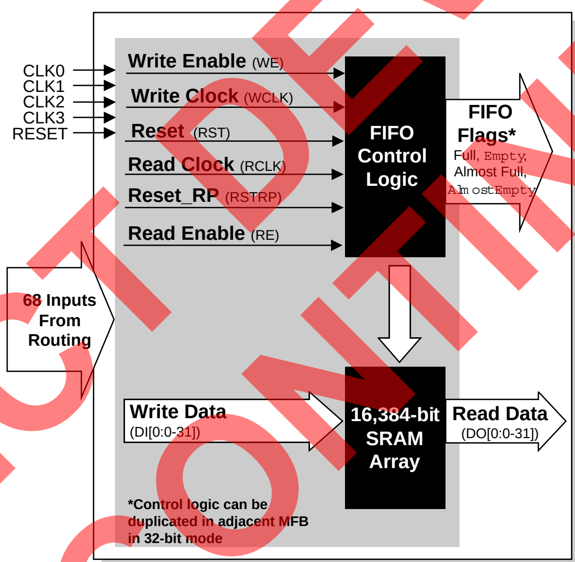


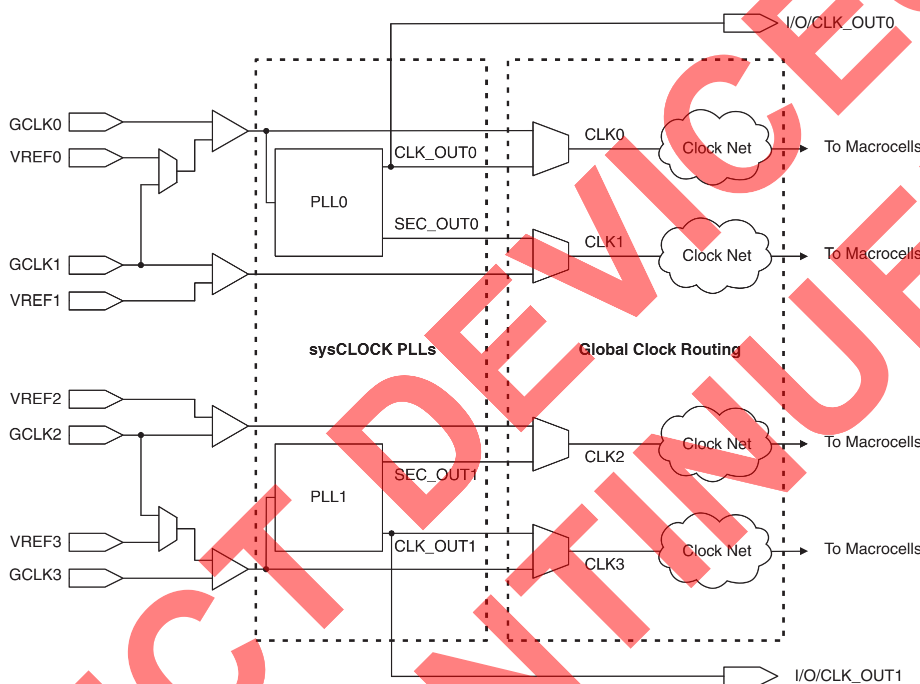
Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Output Sharing Array (OSA)

A number of I/O pads are available in each sysIO bank to route the selected number of macrocells from the MFB outputs directly to the I/O pads in logic mode. In the ispXPLD 5000MX, the large number of inputs and PTs to the MFB as well as the presence of the PTSA can cover most routing flexibility of signals to I/O cells. The Output Sharing Array gives additional routing capability and I/O access to an MFB when a wide output function takes up the whole MFB and cannot be easily divided across multiple MFBs. By using the OSA, the wide output function, such as 32-bit FIFO, can have all of its output signals from the one MFB routed to I/O cells. In a given I/O block, the wide output functions must share the I/O pads with other logic functions.

The OSA bypass option routes the MFB signal directly to the I/O cell, allowing a direct connection to the I/O cell. The logic functions use the option to provide faster speed to the outputs. The Logic Signal Connection tables list the OSA bypass as the primary macrocell and OSA options as alternate macrocells. Similarly, the Alternate Input listing in the table shows the alternate macrocell input connection for a given I/O pin. Figure 17 shows the alternate macrocell connections in an I/O cell.

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedback line to its associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The MFBs are grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PTOE signal is derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) < V_{IN} ð 3.6V	—	—	40	µA
I_{IH}[4]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}[3]	I/O Active Pullup Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{CCO} * 0.35	—	V_{CCO} * 0.65	µA
C1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz
3. I_{PU} on JTAG pins has a maximum of -175µA for 5512MX devices.
4. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[2]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	—	—	—
LVCMOS 2.5	2.3	2.5	2.7	—	—	—
LVCMOS 1.8[1]	1.65	1.8	1.95	—	—	—
LVTTL	3.0	3.3	3.6	—	—	—
PCI 3.3	3.0	3.3	3.6	—	—	—
AGP-1X	3.15	3.3	3.45	—	—	—
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	—	0.9	—
HSTL Class IV	1.4	1.5	1.6	—	0.9	—
GTL+	1.4	—	3.6	0.882	1.0	1.122
LVDS	2.3	2.5/3.3	3.6	—	—	—

1. Design tools default setting.
2. Inputs are independent of V_{CCO} setting. However, V_{CCO} must be set within the valid operating range for one of the supported standards.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DPCEBS}	Clock Enable B Setup before Clock B Time	—	2.33	—	2.33	—	2.33	—	2.33	—	3.03	—	ns
t_{DPCEBH}	Clock Enable Hold B after Clock B Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDBS}$	Address B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDBH}$	Address B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWBS}	R/W B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWBH}	R/W B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATABS}$	Write Data B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATABH}$	Write Data B Hold after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	5.97	—	5.92	—	5.86	—	5.65	—	9.86	ns
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	5.16	—	5.16	—	5.16	—	5.16	—	6.71	ns
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.40	—	1.40	—	1.83	—	ns
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns

Timing v.1.8

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4 Min.	-4 Max.	-45 Min.	-45 Max.	-5 Min.	-5 Max.	-52 Min.	-52 Max.	-75 Min.	-75 Max.	Units
t_{IOI} Input Adjusters													
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t_{IOO} Output Adjusters – Output Signal Modifiers													
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t_{IOO} Output Adjusters – Output Configurations													
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_out	Using HSTL 2.5V, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns

Timing v.1.8

Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the IEEE 1149.1 state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data out.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the registers in the device. The global polarity for this pin is selectable on a global basis.þ The default is active low. An external pull-down is required when polarity is set to active high.
yzz	Input/Output – These are the general purpose I/O used by the logic array. *y* is the MFB reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs (see Figure 14 for differential pairing).
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GNDP	GND – Ground for PLLs.
V_{CCP}	V_{CC} – The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG interface.
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2CMOS or IEEE 1149.1 TAP.
PROGRAMB	Input – Controls the programming of SRAM. Hold high for normal operation. Toggle low to reload SRAM from E^2 memory.
CCLK[1]	Input – Clock for sysCONFIG interface. Reads and writes occur on the rising edge of the clock.
READ[1]	Input – Drive high to perform reads from the sysCONFIG interface.
INITB	I/O – Indicates status of configuration. Can be driven low to inhibit configuration.
DONE	Output (open drain) – Indicates status of configuration.

1. These inputs should not toggle during power up for proper power-up configuration.

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	34N	E30	-	-	E31	H14
3	34P	E28	-	-	E29	G16
3	35N	E26	-	-	E27	G15
3	35P	E24/PLL_FBK1	-	-	E25	F15
3	36N	E22/PLL_RST1	E27	F27	E23	H12
3	36P	E21	E26	F26	-	G14
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	37N	E20	E25	F25	-	F16
-	-	VCCO3	-	-	-	VCCO3
3	37P	E18	E24	F24	E19	E16
-	-	GND	-	-	-	GND
3	38N	E16	E23	F23	E17	G13
3	38P	E14	E22	F22	E15	G12
3	39N	E12	E21	F21	E13	F14
3	39P	E10/CLK_OUT1	E20	F20	E11	E15
-	-	VCC	-	-	-	VCC
3	40N	E8	E19	F19	E9	D12
3	40P	E6	E18	F18	E7	B14
3	41N	E5	E17	F17	-	C13
3	41P	E4	E16	F16	-	A14
3	42N	E2	E31	F31	E3	A13
3	42P	E0	E30	F30	E1	B13
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
-	-	VCCO3	-	-	-	VCCO3
3	43N	F30	E15	F15	F31	B11
3	43P	F28	E14	F14	F29	C11
3	44N	F26	E13	F13	F27	B10
3	44P	F24	E12	F12	F25	A10
3	45N	F22	E11	F11	F23	C10
3	45P	F21	E10	F10	-	D10
3	46N	F20	E9	F9	-	C9
3	46P	F18	E8	F8	F19	E9
3	47N	F16/VREF3	E29	F29	F17	D9
3	47P	F14	E28	F28	F15	F9
3	48N	F12	E7	F7	F13	A9
3	48P	F10	E6	F6	F11	F8
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	49N	F8	E5	F5	F9	E8
-	-	VCCO3	-	-	-	VCCO3
3	49P	F6	E4	F4	F7	A8
3	50N	F5	E3	F3	-	B9
3	50P	F4	E2	F2	-	D8
-	-	VCC	-	-	-	VCC

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	B4
0	109P	O28	O10	P16	O29	1	E4	A4
0	110N	O26	M17	O17	O27	2	B1	B3
0	110P	O24	M16	O16	O25	3	C1	A3
0	111N	O22	M15	O15	O23	4	D3	F5
—	—	V_{CCO0}	—	—	—	5	V_{CCO0}	V_{CCO0}
0	111P	O20	M14	O14	O21	6	C2	G6
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	GND (Bank 0)
0	112N	O18	M13	O13	O19	8	E3	H6
0	112P	O16	M12	O12	O17	9	D2	G5
0	113N	O14	O9	P14	O15	—	—	D3
0	113P	O12	O8	P12	O13	—	—	D2
0	114N	O10	O7	P10	O11	—	—	E4
0	114P	O8	O6	P8	O9	—	—	E3
0	115N	O6	O5	P6	O7	—	—	F4
0	115P	O4	O4	P4	O5	—	—	G4
0	116N	O2	O3	P2	O3	—	—	C2
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	V_{CCO0}
0	116P	O0	O2	P0	O1	—	—	C1
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	117N	P30	O1	—	P31	—	D1	F3
0	117P	P28	O0	—	P29	—	E1	G3
0	118N	P26	O31	—	P27	—	F4	H4
—	—	V_{CC}	—	—	—	10	V_{CC}	V_{CC}
0	118P	P24	O30	—	P25	—	F5	J4
0	119N	P22	M11	O11	P23	11	E2	H5
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	J5
0	120N	P18	M9	O9	P19	13	F1	E2
0	120P	P16	M8	O8	P17	14	G1	F2
—	—	GND	—	—	—	15	GND	GND
0	121N	P14	M7	O7	P15	16	F3	D1
—	—	V_{CCO0}	—	—	—	17	V_{CCO0}	V_{CCO0}
0	121P	P12	M6	O6	P13	18	G5	E1
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	GND (Bank 0)
0	122N	P10	M5	O5	P11	20	H5	J3
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	H2
0	123N	P6	—	—	P7	22	G3	G2
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	G1
0	124N	P2	—	—	P3	24	G2	H1
0	124P	P0	—	—	P1	25	H1	J1
—	GCLK0P	GCLK0	—	—	—	26	H2	N7
—	—	V_{CCJ}	—	—	—	See Power Supply and NC Connections Table		

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	B4
0	127P	S20	S10	T16	S21	E4	A4
0	128N	S18	Q17	S17	S19	B1	B3
0	128P	S16	Q16	S16	S17	C1	A3
0	129N	S14	Q15	S15	S15	D3	F5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	129P	S12	Q14	S14	S13	C2	G6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	130N	S10	Q13	S13	S11	E3	H6
0	130P	S8	Q12	S12	S9	D2	G5
0	131N	S6	S9	T14	S7	—	D3
0	131P	S4	S8	T12	S5	—	D2
0	132N	S2	S7	T10	S3	—	E4
-	-	VCC	-	-	-	VCC	VCC
0	132P	S0	S6	T8	S1	—	E3
-	-	GND	-	-	-	GND	GND
0	133N	T30	S5	T6	T31	—	F4
0	133P	T28	S4	T4	T29	—	G4
0	134N	T26	S3	T2	T27	—	C2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	134P	T24	S2	T0	T25	—	C1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	135N	T22	S1	-	T23	D1	F3
0	135P	T20	S0	-	T21	E1	G3
0	136N	T18	S31	-	T19	F4	H4
-	-	VCC	-	-	-	VCC	VCC
0	136P	T16	S30	-	T17	F5	J4
0	137N	T14	Q11	S11	T15	E2	H5
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	J5
0	138N	T10	Q9	S9	T11	F1	E2
0	138P	T8	Q8	S8	T9	G1	F2
-	-	GND	-	-	-	GND	GND
0	139N	T6	Q7	S7	T7	F3	D1
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	139P	T4	Q6	S6	T5	G5	E1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	140N	T2	Q5	S5	T3	H5	J3
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	H2
0	141N	U30	U31	W31	U31	G3	G2
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	G1
0	142N	U26	U29	W29	U27	—	J6
0	142P	U24	U28	W28	U25	—	K4

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	T1	P3
-	-	TDO	-	-	-	V1	P2
1	0P	A30	A0	C0	A31	—	P1
1	0N	A28	A1	C1	A29	—	R1
1	1P	A26	A2	C2	A27	—	P6
1	1N	A24	A3	C3	A25	—	R6
1	2P	A22	A4	C4	A23	—	P7
1	2N	A20	A5	C5	A21	—	R7
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18	A6	C6	A19	—	R4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16	A7	C7	A17	—	R5
-	-	GND	-	-	-	GND	GND
1	4P	A14	A8	C8	A15	—	R3
-	-	VCC	-	-	-	VCC	VCC
1	4N	A12	A9	C9	A13	—	R2
1	5P	A10	A10	C10	A11	—	T2
1	5N	A8	A11	C11	A9	—	T3
1	6P	A6	A12	C12	A7	—	T4
1	6N	A4	A13	C13	A5	—	T5
1	7P	A2	A14	C14	A3	—	U2
1	7N	A0	A15	C15	A1	—	U3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	8P	C30	A16	C16	C31	—	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	8N	C28	A17	C17	C29	—	U5
1	9P	C26	A18	C18	C27	—	T6
1	9N	C24	A19	C19	C25	—	U6
1	10P	C22	A20	C20	C23	—	T7
1	10N	C20	A21	C21	C21	—	U7
1	11P	C18	A22	C22	C19	—	U1
1	11N	C16	A23	C23	C17	—	V1
1	12P	C14	A24	C24	C15	—	V2
1	12N	C12	A25	C25	C13	—	V3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	13P	C10	A26	C26	C11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	13N	C8	A27	C27	C9	—	V4
-	-	GND	-	-	-	GND	GND
1	14P	C6	A28	C28	C7	—	W2
-	-	VCC	-	-	-	VCC	VCC
1	14N	C4	A29	C29	C5	—	W3
1	15P	C2	A30	C30	C3	—	W4

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	110N	U4	X25	V25	U5	H21	J21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	110P	U6	X24	V24	U7	G21	H21
-	-	GND	-	-	-	GND	GND
3	111N	U8	X23	V23	U9	D22	G25
3	111P	U10	X22	V22	U11	D21	G24
3	112N	U12	X21	V21	U13	J20	G23
3	112P	U14/CLK_OUT1	X20	V20	U15	J19	G22
3	113N	U16	V31	-	U17	E20	J20
-	-	VCC	-	-	-	VCC	VCC
3	113P	U18	V30	U30	U19	F20	H20
3	114N	U20	V29	U28	U21	H17	G26
3	114P	U22	V28	U26	U23	H18	F25
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	115N	U24	V27	-	U25	J18	F24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	115P	U26	V26	-	U27	H19	F23
3	116N	U28	V25	-	U29	G20	G21
3	116P	U30	V24	-	U31	G19	F22
-	-	GND	-	-	-	GND	GND
3	117N	V0	V23	-	V1	C22	F26
-	-	VCC	-	-	-	VCC	VCC
3	117P	V2	V22	-	V3	C21	E26
3	118N	V4	V21	-	V5	D20	E25
3	118P	V6	V20	-	V7	C19	E24
3	119N	V8	V19	-	V9	F19	E23
3	119P	V10	V18	-	V11	E19	E22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	120N	V12	V17	-	V13	G18	D26
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	120P	V14	V16	-	V15	F18	D25
3	121N	V16	V15	-	V17	B20	D24
3	121P	V18	V14	-	V19	B19	D23
3	122N	V20	V13	-	V21	A20	C26
3	122P	V22	V12	-	V23	A19	C25
3	123N	V24	X19	V19	V25	D18	G19
3	123P	V26	X18	V18	V27	C18	F19
3	124N	V28	X17	V17	V29	G17	G18
3	124P	V30	X16	V16	V31	F16	F18
3	125N	W0	X31	V31	W1	E17	F20
3	125P	W2	X30	V30	W3	D17	E20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)