Lattice Semiconductor Corporation - LC5512MV-75Q208I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	149
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75q208i

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

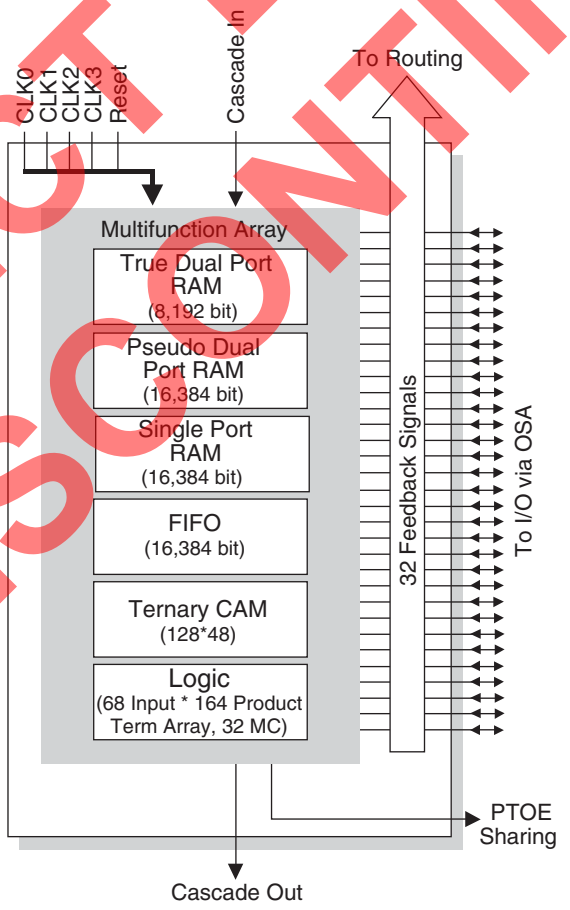
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram



Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width support.

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	H -> G -> F -> E
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size[1]
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output
The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation
In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width
Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

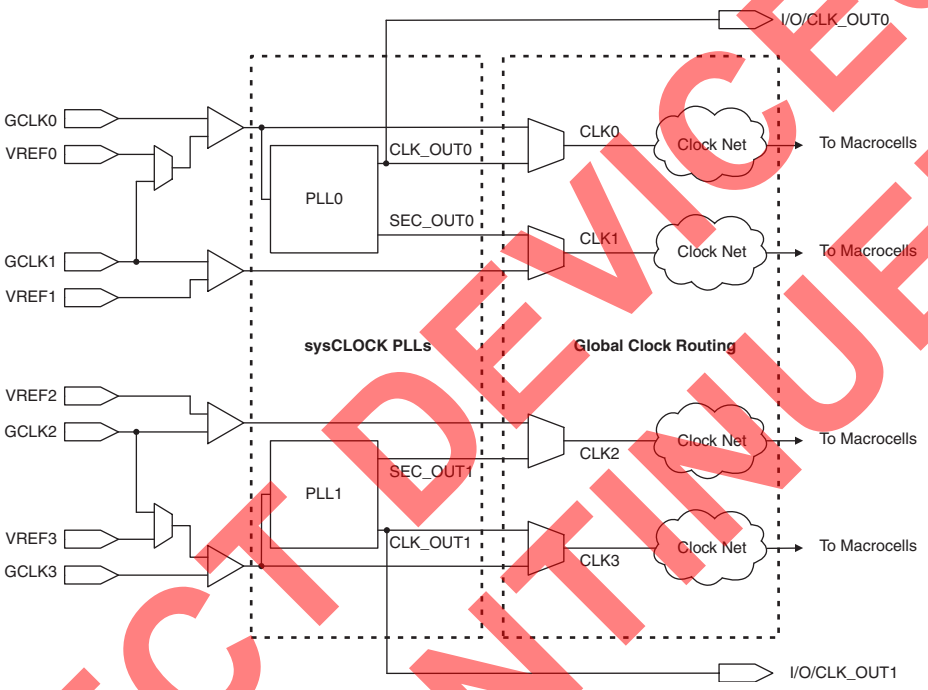
The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching
All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to TN1000 – sysIO Usage Guidelines for Lattice Devices.

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. The JTAG TAP pins support only LVCMOS 3.3, 2.5 and 1.8V standards. The voltage is controlled by V_{CCJ}. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

sysIO Differential DC Electrical Characteristics

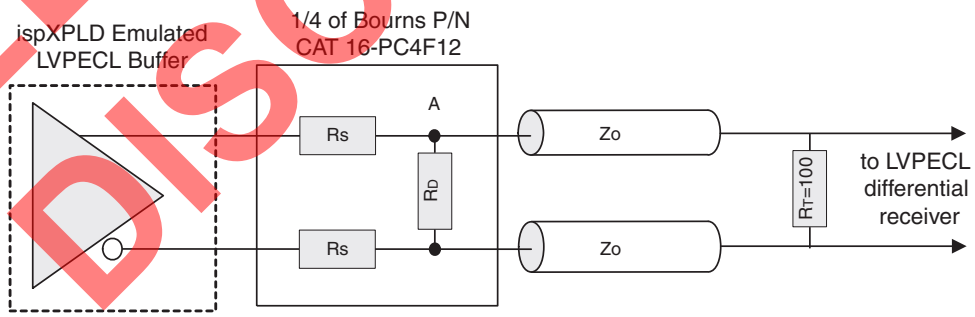
Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS					
V_{INP}	Input Voltage		0V	—	2.4V
V_{THD}	Differential Input Threshold	0.2 ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input Current	Power On	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50mV
V_{OS}	Output Voltage Offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125V	1.20V	1.375V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—	24mA

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input voltage	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 19). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V

Figure 19. LVPECL Driver with Three Resistor Pack



ispXPLD 5000MX Family External Switching Characteristics (Continued)[1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (RAM)[5]	Clock Frequency to RAM in:											
	Single Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Dual Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—	106	MHz
f_{MAX} (FIFO)[5]	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—	132	MHz
t_{PWR_ON}	Power-on Time	—	200	—	200	—	200	—	200	—	200	µs

Timing v.1.8

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

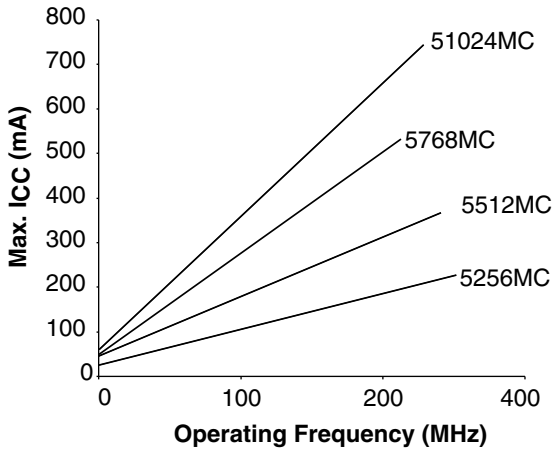
ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	"Don't Care" Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	"Don't Care" Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

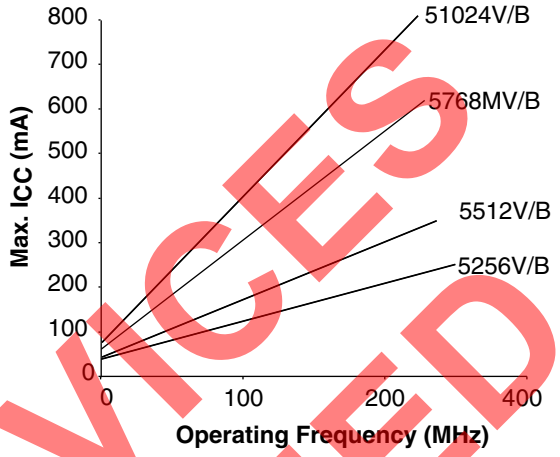
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the IEEE 1149.1 state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data out.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the registers in the device. The global polarity for this pin is selectable on a global basis.þ The default is active low. An external pull-down is required when polarity is set to active high.
yzz	Input/Output – These are the general purpose I/O used by the logic array. *y* is the MFB reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs (see Figure 14 for differential pairing).
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GNDP	GND – Ground for PLLs.
V_{CCP}	V_{CC} – The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG interface.
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2CMOS or IEEE 1149.1 TAP.
PROGRAMB	Input – Controls the programming of SRAM. Hold high for normal operation. Toggle low to reload SRAM from E^2 memory.
CCLK[1]	Input – Clock for sysCONFIG interface. Reads and writes occur on the rising edge of the clock.
READ[1]	Input – Drive high to perform reads from the sysCONFIG interface.
INITB	I/O – Indicates status of configuration. Can be driven low to inhibit configuration.
DONE	Output (open drain) – Indicates status of configuration.

1. These inputs should not toggle during power up for proper power-up configuration.

ispXPLD 5000MX Power Supply and NC Connections[1]

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	143N	U22	U27	W27	U23	—	K6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	U20	U26	W26	U21	—	K3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	U18	U25	W25	U19	—	K5
0	144P	U16	U24	W24	U17	—	K2
0	145N	U14	U23	W23	U15	—	L5
0	145P	U12	U22	W22	U13	—	K1
0	146N	U10	U21	W21	U11	—	L6
0	146P	U8	U20	W20	U9	—	L1
0	147N	U6	U19	W19	U7	—	M5
0	147P	U4	U18	W18	U5	—	L2
0	148N	U2	U17	W17	U3	—	N5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	148P	U0	U16	W16	U1	—	L3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	149N	W30	U15	W15	W31	—	M6
0	149P	W28	U14	W14	W29	—	M2
0	150N	W26	U13	W13	W27	—	P5
-	-	VCC	-	-	-	VCC	VCC
0	150P	W24	U12	W12	W25	—	P6
0	151N	W22	U11	W11	W23	—	M3
0	151P	W20	U10	W10	W21	—	N6
0	152N	W18	U9	W9	W19	—	N2
0	152P	W16	U8	W8	W17	—	P1
-	-	GND	-	-	-	GND	GND
0	153N	W14	U7	W7	W15	—	N3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	153P	W12	U6	W6	W13	—	M8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	154N	W10	U5	W5	W11	—	N8
0	154P	W8	U4	W4	-	—	P2
0	155N	W6	U3	W3	W7	—	P8
0	155P	W4	U2	W2	W5	—	N4
0	156N	W2	U1	W1	W3	G2	H1
0	156P	W0	U0	W0	W1	H1	J1
-	GCLK0P	GCLK0	-	-	-	H2	N7
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	J2	P7
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	H6	R1
-	-	TMS	-	-	-	H4	R2

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	126N	S26	S13	-	S27	—	C4
0	126P	S24	S12	-	S25	—	D5

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	126N	W4	V11	U21	W5	B18	E19
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	126P	W6	V10	U20	W7	A18	E18
-	-	GND	-	-	-	GND	GND
3	127N	W8	V9	U18	W9	C17	C24
-	-	VCC	-	-	-	VCC	VCC
3	127P	W10	V8	U16	W11	B17	C23
3	128N	W12	V7	U12	W13	C16	D22
3	128P	W14	V6	U10	W15	B16	D21
3	129N	W16	V5	U8	W17	F13	E21
3	129P	W18	V4	U6	W19	F15	D20
3	130N	W20	V3	U5	W21	D16	D19
3	130P	W22	V2	U4	W23	E16	D18
3	131N	W24	V1	U2	W25	A16	C22
3	131P	W26	V0	U0	W27	A15	C21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	132N	W28	X15	V15	W29	B15	C20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	132P	W30	X14	V14	W31	A14	C19
3	133N	X0	X13	V13	X1	D15	C18
3	133P	X2	X12	V12	X3	E15	C17
3	134N	X4	X11	V11	X5	D14	B24
3	134P	X6	X10	V10	X7	F14	B23
3	135N	X8	X9	V9	X9	A13	B22
3	135P	X10	X8	V8	X11	B13	B21
3	136N	X12/VREF3	X29	V29	X13	C14	B20
3	136P	X14	X28	V28	X15	E14	B19
3	137N	X16	X7	V7	X17	E13	B18
3	137P	X18	X6	V6	X19	F12	B17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	138N	X20	X5	V5	X21	D13	A24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	138P	X22	X4	V4	X23	C13	A23
3	139N	X24	X3	V3	X25	E12	A22
-	-	GND	-	-	-	GND	GND
3	139P	X26	X2	V2	X27	C12	A21
-	-	VCC	-	-	-	VCC	VCC
3	140N	X28	X1	V1	X29	B12	A20
3	140P	X30	X0	V0	X31	A12	A19
0	141N	Y30	Y31	AA31	Y31	E11	A18
-	-	VCC	-	-	-	VCC	VCC
0	141P	Y28	Y30	AA30	Y29	C11	A17
-	-	GND	-	-	-	GND	GND

ispXPLD 5000MC (1.8V) Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5768MC	LC5768MC-5F256C	768	1.8	5.0	fpBGA	256	193	C
	LC5768MC-75F256C	768	1.8	7.5	fpBGA	256	193	C
	LC5768MC-5F484C	768	1.8	5.0	fpBGA	484	317	C
	LC5768MC-75F484C	768	1.8	7.5	fpBGA	484	317	C
LC51024MC	LC51024MC-52F484C	1024	1.8	5.2	fpBGA	484	317	C
	LC51024MC-75F484C	1024	1.8	7.5	fpBGA	484	317	C
	LC51024MC-52F672C	1024	1.8	5.2	fpBGA	672	381	C
	LC51024MC-75F672C	1024	1.8	7.5	fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5F256I	256	1.8	5.0	fpBGA	256	141	I
	LC5256MC-75F256I	256	1.8	7.5	fpBGA	256	141	I
LC5512MC	LC5512MC-75Q208I	512	1.8	7.5	PQFP	208	149	I
	LC5512MC-75F256I	512	1.8	7.5	fpBGA	256	193	I
	LC5512MC-75F484I	512	1.8	7.5	fpBGA	484	253	I
LC5768MC	LC5768MC-75F256I	768	1.8	7.5	fpBGA	256	193	I
	LC5768MC-75F484I	768	1.8	7.5	fpBGA	484	317	I
LC51024MC	LC51024MC-75F484I	1024	1.8	7.5	fpBGA	484	317	I
	LC51024MC-75F672I	1024	1.8	7.5	fpBGA	672	381	I

ispXPLD 5000MB (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4F256C	256	2.5	4.0	fpBGA	256	141	C
	LC5256MB-5F256C	256	2.5	5.0	fpBGA	256	141	C
	LC5256MB-75F256C	256	2.5	7.5	fpBGA	256	141	C
LC5512MB	LC5512MB-45Q208C	512	2.5	4.5	PQFP	208	149	C
	LC5512MB-75Q208C	512	2.5	7.5	PQFP	208	149	C
	LC5512MB-45F256C	512	2.5	4.5	fpBGA	256	193	C
	LC5512MB-75F256C	512	2.5	7.5	fpBGA	256	193	C
	LC5512MB-45F484C	512	2.5	4.5	fpBGA	484	253	C
	LC5512MB-75F484C	512	2.5	7.5	fpBGA	484	253	C
LC5768MB	LC5768MB-5F256C	768	2.5	5.0	fpBGA	256	193	C
	LC5768MB-75F256C	768	2.5	7.5	fpBGA	256	193	C
	LC5768MB-5F484C	768	2.5	5.0	fpBGA	484	317	C
	LC5768MB-75F484C	768	2.5	7.5	fpBGA	484	317	C
LC51024MB	LC51024MB-52F484C	1024	2.5	5.2	fpBGA	484	317	C
	LC51024MB-75F484C	1024	2.5	7.5	fpBGA	484	317	C
	LC51024MB-52F672C	1024	2.5	5.2	fpBGA	672	381	C
	LC51024MB-75F672C	1024	2.5	7.5	fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4FN256C	256	2.5	4.0	Lead-free fpBGA	256	141	C
	LC5256MB-5FN256C	256	2.5	5.0	Lead-free fpBGA	256	141	C
	LC5256MB-75FN256C	256	2.5	7.5	Lead-free fpBGA	256	141	C
LC5512MB	LC5512MB-45QN208C	512	2.5	4.5	Lead-free PQFP	208	149	C
	LC5512MB-75QN208C	512	2.5	7.5	Lead-free PQFP	208	149	C
	LC5512MB-45FN256C	512	2.5	4.5	Lead-free fpBGA	256	193	C
	LC5512MB-75FN256C	512	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5512MB-45FN484C	512	2.5	4.5	Lead-free fpBGA	484	253	C
	LC5512MB-75FN484C	512	2.5	7.5	Lead-free fpBGA	484	253	C
LC5768MB	LC5768MB-5FN256C	768	2.5	5.0	Lead-free fpBGA	256	193	C
	LC5768MB-75FN256C	768	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5768MB-5FN484C	768	2.5	5.0	Lead-free fpBGA	484	317	C
	LC5768MB-75FN484C	768	2.5	7.5	Lead-free fpBGA	484	317	C
LC51024MB	LC51024MB-52FN484C	1024	2.5	5.2	Lead-free fpBGA	484	317	C
	LC51024MB-75FN484C	1024	2.5	7.5	Lead-free fpBGA	484	317	C
	LC51024MB-52FN672C	1024	2.5	5.2	Lead-free fpBGA	672	381	C
	LC51024MB-75FN672C	1024	2.5	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5FN256I	256	2.5	5.0	Lead-free fpBGA	256	141	I
	LC5256MB-75FN256I	256	2.5	7.5	Lead-free fpBGA	256	141	I
LC5512MB	LC5512MB-75QN208I	512	2.5	7.5	Lead-free PQFP	208	149	I
	LC5512MB-75FN256I	512	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5512MB-75FN484I	512	2.5	7.5	Lead-free fpBGA	484	253	I
LC5768MB	LC5768MB-75FN256I	768	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5768MB-75FN484I	768	2.5	7.5	Lead-free fpBGA	484	317	I
LC51024MB	LC51024MB-75FN484I	1024	2.5	7.5	Lead-free fpBGA	484	317	I
	LC51024MB-75FN672I	1024	2.5	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4FN256C	256	3.3	4.0	Lead-free fpBGA	256	141	C
	LC5256MV-5FN256C	256	3.3	5.0	Lead-free fpBGA	256	141	C
	LC5256MV-75FN256C	256	3.3	7.5	Lead-free fpBGA	256	141	C