Lattice Semiconductor Corporation - LC5512MV-75QN208C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	149
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75qn208c

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

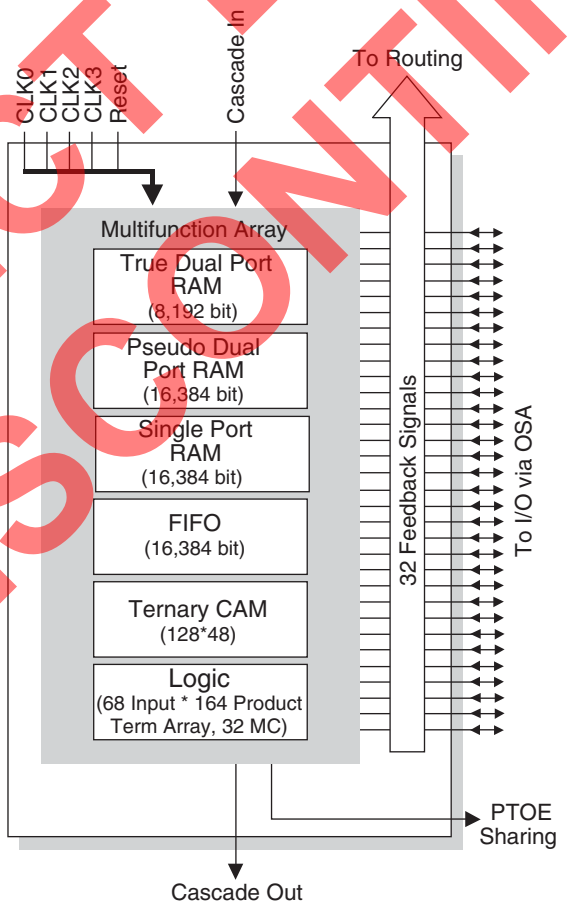
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

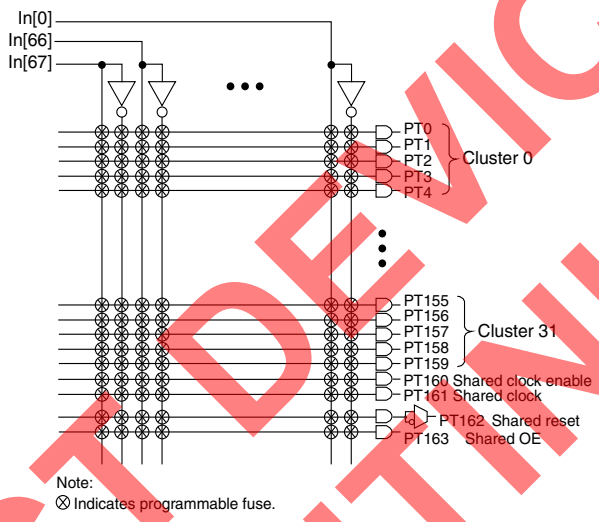
Figure 2. MFB Block Diagram



AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array



Dual-OR Array (Including Arithmetic Support)

The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

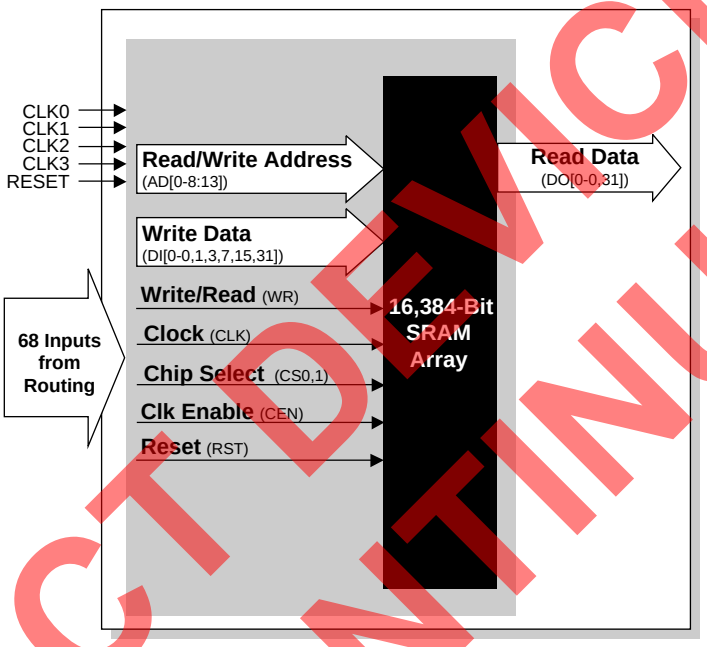


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

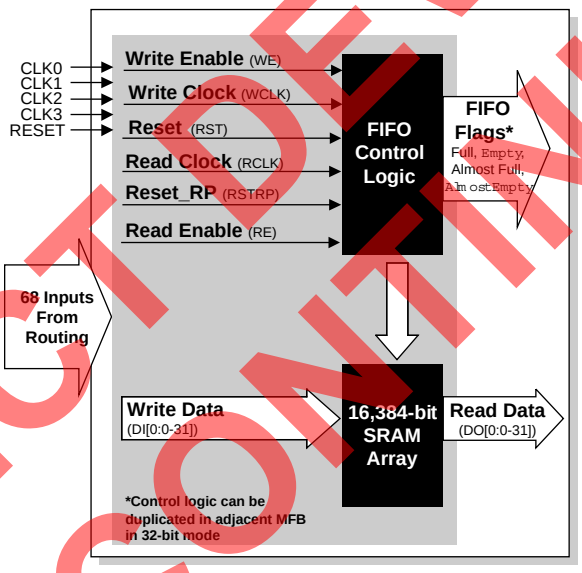


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Figure 15. PLL Block Diagram

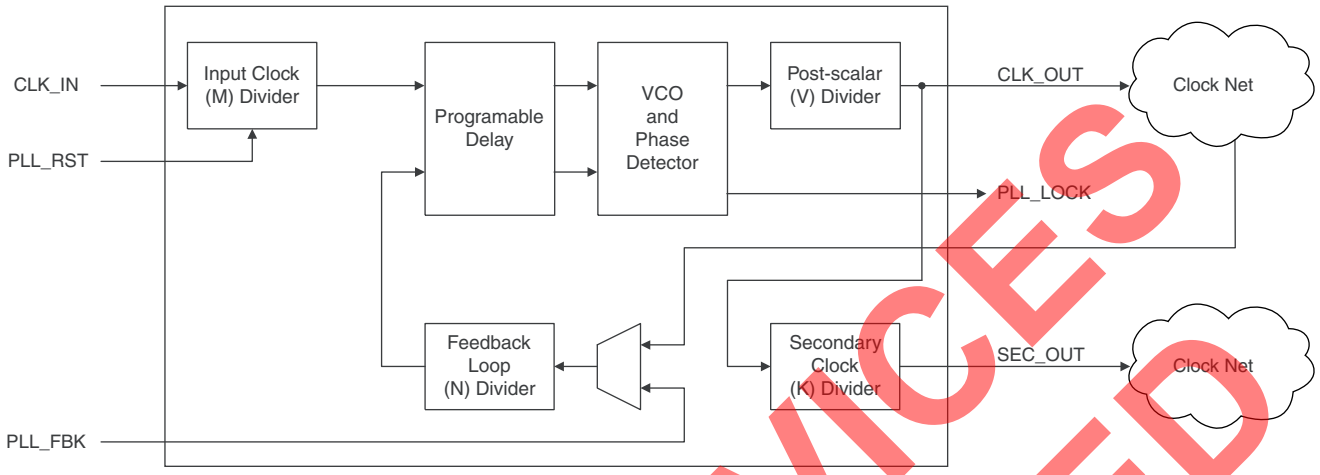
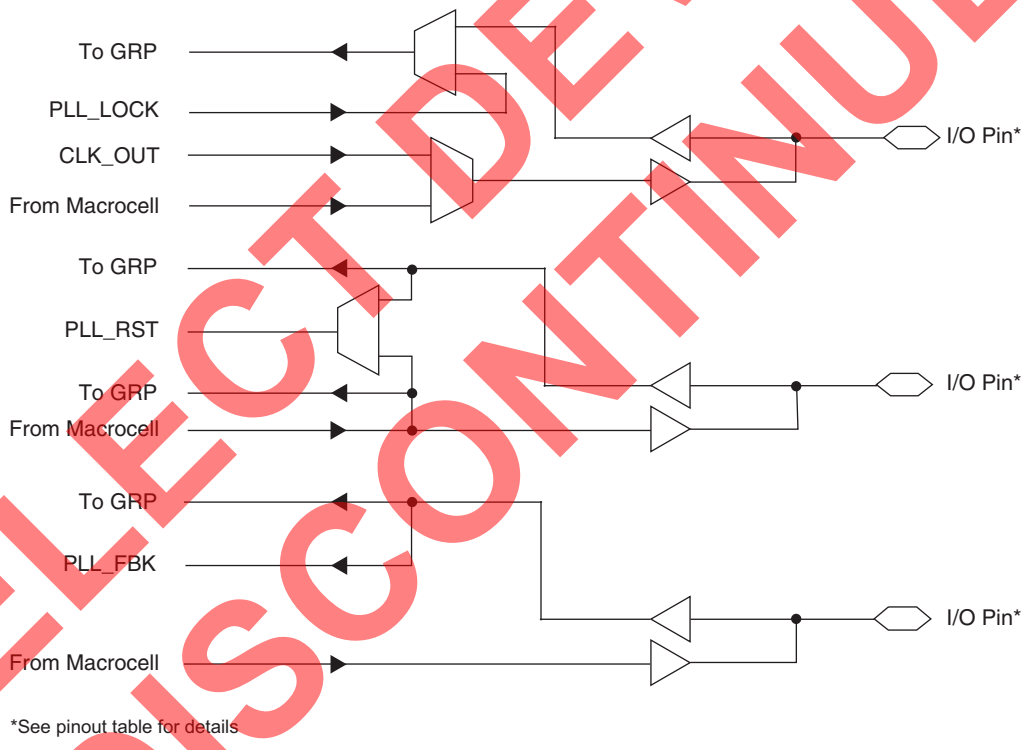


Figure 16. Connection of Optional PLL Inputs and Outputs



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to TN1000 – sysIO Usage Guidelines for Lattice Devices.

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. The JTAG TAP pins support only LVCMOS 3.3, 2.5 and 1.8V standards. The voltage is controlled by V_{CCJ}. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Registered Delays													
t_S	D-Register Setup Time, Global Clock	—	0.28	—	0.31	—	0.35	—	0.55	—	0.52	—	ns
t_{S_PT}	D-Register Setup Time, PT Clock	—	-0.13	—	-0.11	—	-0.10	—	-0.10	—	-0.07	—	ns
t_H	D-Register Hold Time	—	1.90	—	2.56	—	2.50	—	2.40	—	4.00	—	ns
t_{COi}	Register Clock to OSA Time	—	—	0.72	—	1.03	—	0.68	—	0.93	—	1.50	ns
t_{CESi}	Clock Enable Setup Time	—	1.07	—	1.20	—	1.33	—	1.33	—	2.00	—	ns
t_{CEHi}	Clock Enable Hold Time	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{SIR}	D-Input Register Setup Time, Global Clock	—	0.66	—	0.20	—	0.53	—	0.12	—	0.08	—	ns
t_{SIR_PT}	D-Input Register Setup Time, PT Clock	—	0.42	—	0.37	—	0.34	—	0.34	—	0.22	—	ns
t_{HIR}	D-Input Register Hold Time, Global Clock	—	0.84	—	1.31	—	1.01	—	1.41	—	2.91	—	ns
t_{HIR_PT}	D-Input Register Hold Time, PT Clock	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
Latched Delays													
t_{SL}	Latch Setup Time, Global Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{SL_PT}	Latch Setup Time, PT Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.34	—	ns
t_{HL}	Latch Hold Time	—	-0.06	—	0.00	—	0.00	—	0.00	—	-0.03	—	ns
t_{GOi}	Latch Gate to OSA Time	—	—	0.07	—	0.08	—	0.08	—	0.08	—	0.13	ns
t_{PDLi}	Propagation Delay through Latch to OSA Transparent	—	—	0.52	—	0.58	—	0.65	—	0.65	—	0.97	ns
Reset and Set Delays													
t_{SRi}	Asynchronous Reset or Set to OSA Delay	—	—	0.23	—	0.26	—	0.29	—	0.29	—	0.43	ns
t_{SRR}	Asynchronous Reset or Set Recovery	—	—	0.42	—	0.47	—	0.53	—	0.55	—	0.79	ns
eXtended Function Routing Delays													
$t_{ROUTEMF}$	Delay through SRP when Implementing Memory Functions	—	—	2.00	—	2.25	—	2.51	—	2.61	—	3.76	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—	1.33	ns
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—	0.66	ns
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—	0.19	ns
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—	4.91	ns
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	2.89	—	3.21	—	3.34	—	4.82	ns
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—	1.50	ns
Optional Adjusters													
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—	0.07	ns
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—	0.99	ns
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—	0.94	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—	0.91	ns
t_{INEXP}	MFB Input Extender	t_{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—	1.16	ns
Input and Output Buffer Delays													
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables										ns
t_{IOO}	Output Buffer Selection Adder	t_{BUF}											ns
FIFO													
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—	4.00	ns
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—	4.01	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{SPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{SPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	9.86	ns
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns
Pseudo Dual Port RAM													
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCES}$	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{PDPRCEH}$	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPWCES}$	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43	—	ns
$t_{PDPWCEH}$	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPRADDS}$	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPRADDH}$	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPWADDS}$	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPWADDH}$	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{PDPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—	8.54	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
Dual Port RAM													
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84	—	ns
t_{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDAS}$	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDAH}$	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATAAS}$	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATAAH}$	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{DPCEBS}	Clock Enable B Setup before Clock B Time	—	2.33	—	2.33	—	2.33	—	2.33	—	3.03	—	ns
t_{DPCEBH}	Clock Enable Hold B after Clock B Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDBS}$	Address B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDBH}$	Address B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWBS}	R/W B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWBH}	R/W B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATABS}$	Write Data B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATABH}$	Write Data B Hold after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	5.97	—	5.92	—	5.86	—	5.65	—	9.86	ns
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	5.16	—	5.16	—	5.16	—	5.16	—	6.71	ns
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.40	—	1.40	—	1.83	—	ns
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns

Timing v.1.8

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	Output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 250	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 150	ps
$T_{JIT(PERIOD)}$[2]	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 300	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 150	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	600	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		—	1.8	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay (t_{PLL_DELAY})		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specification.
2. Accumulated jitter measured over 10,000 waveform samples.
3. Internal timing for reference only.

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

ispXPLD 5000MX Power Supply and NC Connections[1]

ispXPLD 5256MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
0	61N	H30	G17	H17	H31	B1
0	61P	H28	G16	H16	H29	C1
0	62N	H26	G15	H15	H27	D3
0	62P	H24	G14	H14	H25	C2
0	63N	H22	G13	H13	H23	E3
0	63P	H21	G12	H12	-	D2
-	-	VCC	-	-	-	VCC
0	64N	H20	G11	H11	-	E2
0	64P	H18/CLK_OUT0	G10	H10	H19	F2
0	65N	H16	G9	H9	H17	F1
0	65P	H14	G8	H8	H15	G1
-	-	GND	-	-	-	GND
0	66N	H12	G7	H7	H13	F3
-	-	VCCO0	-	-	-	VCCO0
0	66P	H10	G6	H6	H11	G5
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	67N	H8	G5	H5	H9	H5
0	67P	H6/PLL_RST0	G4	H4	H7	G4
0	68N	H5	-	-	-	G3
0	68P	H4/PLL_FBK0	-	-	-	H3
0	69N	H2	-	-	H3	G2
0	69P	H0	-	-	H1	H1
-	GCLK0P	GCLK0	-	-	-	H2
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table
-	GCLK0N	GCLK1	-	-	-	J2
-	-	GND	-	-	-	GND
-	-	TDI	-	-	-	H6
-	-	TMS	-	-	-	H4
-	-	TCK	-	-	-	J6
-	-	TDO	-	-	-	K2
1	0P	A0/DATA0	A0	B0	A1	K3
1	0N	A2/DATA1	A1	B1	A3	J3
1	1P	A4/DATA2	A2	B2	-	J5
1	1N	A5/DATA3	A3	B3	-	J4
1	2P	A6/DATA4	A4	B4	A7	L2
1	2N	A8/DATA5	A5	B5	A9	M1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	3P	A10/DATA6	A6	B6	A11	K4
-	-	VCCO1	-	-	-	VCCO1
1	3N	A12/DATA7	A7	B7	A13	L3
-	-	GND	-	-	-	GND
1	4P	A14/INITB	A8	B8	A15	K5

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7[1]	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10[1]	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	B4
0	127P	S20	S10	T16	S21	E4	A4
0	128N	S18	Q17	S17	S19	B1	B3
0	128P	S16	Q16	S16	S17	C1	A3
0	129N	S14	Q15	S15	S15	D3	F5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	129P	S12	Q14	S14	S13	C2	G6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	130N	S10	Q13	S13	S11	E3	H6
0	130P	S8	Q12	S12	S9	D2	G5
0	131N	S6	S9	T14	S7	—	D3
0	131P	S4	S8	T12	S5	—	D2
0	132N	S2	S7	T10	S3	—	E4
-	-	VCC	-	-	-	VCC	VCC
0	132P	S0	S6	T8	S1	—	E3
-	-	GND	-	-	-	GND	GND
0	133N	T30	S5	T6	T31	—	F4
0	133P	T28	S4	T4	T29	—	G4
0	134N	T26	S3	T2	T27	—	C2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	134P	T24	S2	T0	T25	—	C1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	135N	T22	S1	-	T23	D1	F3
0	135P	T20	S0	-	T21	E1	G3
0	136N	T18	S31	-	T19	F4	H4
-	-	VCC	-	-	-	VCC	VCC
0	136P	T16	S30	-	T17	F5	J4
0	137N	T14	Q11	S11	T15	E2	H5
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	J5
0	138N	T10	Q9	S9	T11	F1	E2
0	138P	T8	Q8	S8	T9	G1	F2
-	-	GND	-	-	-	GND	GND
0	139N	T6	Q7	S7	T7	F3	D1
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	139P	T4	Q6	S6	T5	G5	E1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	140N	T2	Q5	S5	T3	H5	J3
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	H2
0	141N	U30	U31	W31	U31	G3	G2
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	G1
0	142N	U26	U29	W29	U27	—	J6
0	142P	U24	U28	W28	U25	—	K4

ispXPLD 51024MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	159N	AA22	AA11	AB18	AA23	B4	C2
0	159P	AA20	AA10	AB16	AA21	A4	C1
0	160N	AA18	Y17	AA17	AA19	B3	D4
0	160P	AA16	Y16	AA16	AA17	A3	D3
0	161N	AA14	Y15	AA15	AA15	F5	D2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	161P	AA12	Y14	AA14	AA13	G6	D1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	162N	AA10	Y13	AA13	AA11	H6	E5
0	162P	AA8	Y12	AA12	AA9	G5	E4
0	163N	AA6	AA9	AB14	AA7	D3	E3
0	163P	AA4	AA8	AB12	AA5	D2	E2
0	164N	AA2	AA7	AB10	AA3	E4	E1
-	-	VCC	-	-	-	VCC	VCC
0	164P	AA0	AA6	AB8	AA1	E3	F2
-	-	GND	-	-	-	GND	GND
0	165N	AB30	AA5	AB6	AB31	F4	F5
0	165P	AB28	AA4	AB4	AB29	G4	G6
0	166N	AB26	AA3	AB2	AB27	C2	F4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	166P	AB24	AA2	AB0	AB25	C1	F3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	167N	AB22	AA1	-	AB23	F3	F1
0	167P	AB20	AA0	-	AB21	G3	G1
0	168N	AB18	AA31	-	AB19	H4	G5
-	-	VCC	-	-		VCC	VCC
0	168P	AB16	AA30	-	AB17	J4	G4
0	169N	AB14	Y11	AA11	AB15	H5	H7
0	169P	AB12/CLK_OUT0	Y10	AA10	AB13	J5	J7
0	170N	AB10	Y9	AA9	AB11	E2	G3
0	170P	AB8	Y8	AA8	AB9	F2	G2
-	-	GND	-	-	-	GND	GND
0	171N	AB6	Y7	AA7	AB7	D1	H6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	171P	AB4	Y6	AA6	AB5	E1	J6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	172N	AB2	Y5	AA5	AB3	J3	H5
0	172P	AB0/PLL_RST0	Y4	AA4	AB1	H2	H4
0	173N	AC30	AC31	AE31	AC31	G2	H3
0	173P	AC28/PLL_FBK0	AC30	AE30	AC29	G1	H2
0	174N	AC26	AC29	AE29	AC27	J6	H1
0	174P	AC24	AC28	AE28	AC25	K4	J1

Lead-Free Packaging

ispXPLD 5000MC (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4FN256C	256	1.8	4.0	Lead-free fpBGA	256	141	C
	LC5256MC-5FN256C	256	1.8	5.0	Lead-free fpBGA	256	141	C
	LC5256MC-75FN256C	256	1.8	7.5	Lead-free fpBGA	256	141	C
LC5512MC	LC5512MC-45QN208C	512	1.8	4.5	Lead-free PQFP	208	149	C
	LC5512MC-75QN208C	512	1.8	7.5	Lead-free PQFP	208	149	C
	LC5512MC-45FN256C	512	1.8	4.5	Lead-free fpBGA	256	193	C
	LC5512MC-75FN256C	512	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5512MC-45FN484C	512	1.8	4.5	Lead-free fpBGA	484	253	C
	LC5512MC-75FN484C	512	1.8	7.5	Lead-free fpBGA	484	253	C
LC5768MC	LC5768MC-5FN256C	768	1.8	5.0	Lead-free fpBGA	256	193	C
	LC5768MC-75FN256C	768	1.8	7.5	Lead-free fpBGA	256	193	C
	LC5768MC-5FN484C	768	1.8	5.0	Lead-free fpBGA	484	317	C
	LC5768MC-75FN484C	768	1.8	7.5	Lead-free fpBGA	484	317	C
LC51024MC	LC51024MC-52FN484C	1024	1.8	5.2	Lead-free fpBGA	484	317	C
	LC51024MC-75FN484C	1024	1.8	7.5	Lead-free fpBGA	484	317	C
	LC51024MC-52FN672C	1024	1.8	5.2	Lead-free fpBGA	672	381	C
	LC51024MC-75FN672C	1024	1.8	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5FN256I	256	1.8	5.0	Lead-free fpBGA	256	141	I
	LC5256MC-75FN256I	256	1.8	7.5	Lead-free fpBGA	256	141	I
LC5512MC	LC5512MC-75QN208I	512	1.8	7.5	Lead-free PQFP	208	149	I
	LC5512MC-75FN256I	512	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5512MC-75FN484I	512	1.8	7.5	Lead-free fpBGA	484	253	I
LC5768MC	LC5768MC-75FN256I	768	1.8	7.5	Lead-free fpBGA	256	193	I
	LC5768MC-75FN484I	768	1.8	7.5	Lead-free fpBGA	484	317	I
LC51024MC	LC51024MC-75FN484I	1024	1.8	7.5	Lead-free fpBGA	484	317	I
	LC51024MC-75FN672I	1024	1.8	7.5	Lead-free fpBGA	672	381	I