Lattice Semiconductor Corporation - LC5512MV-75QN208I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	512
Number of Gates	-
Number of I/O	149
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5512mv-75qn208i

Figure 1. ispXPLD 5000MX Block Diagram

Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

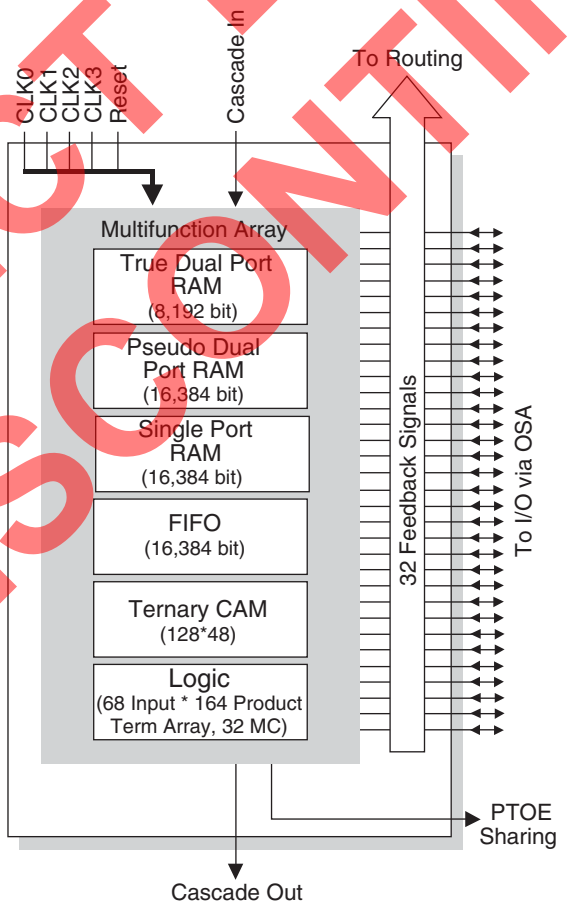
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

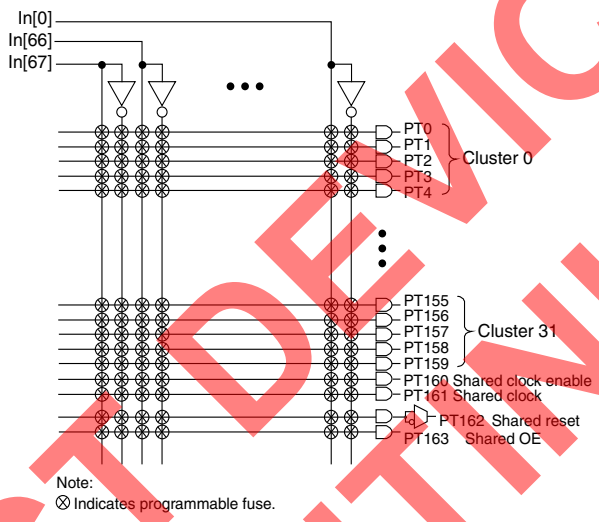
Figure 2. MFB Block Diagram



AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array



Dual-OR Array (Including Arithmetic Support)

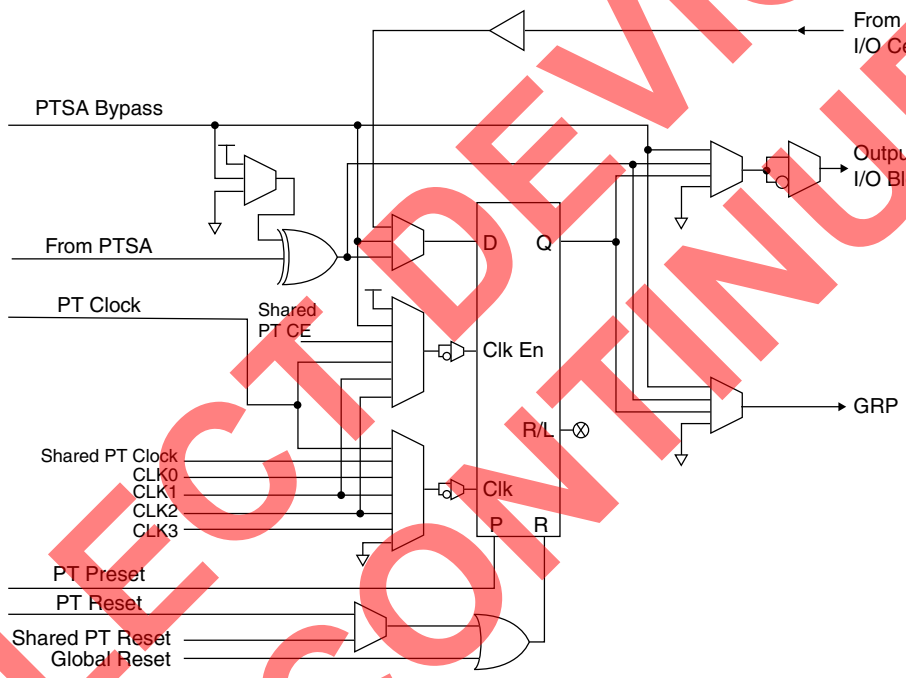
The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in TN1030, Using Memory in ispXPLD 5000MX Devices.

Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size[1]
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output
The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation
In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width
Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching
All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

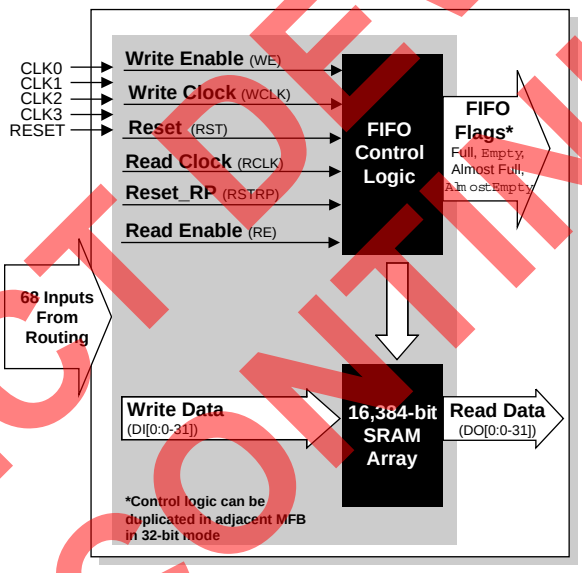


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

Supply Current (Continued)

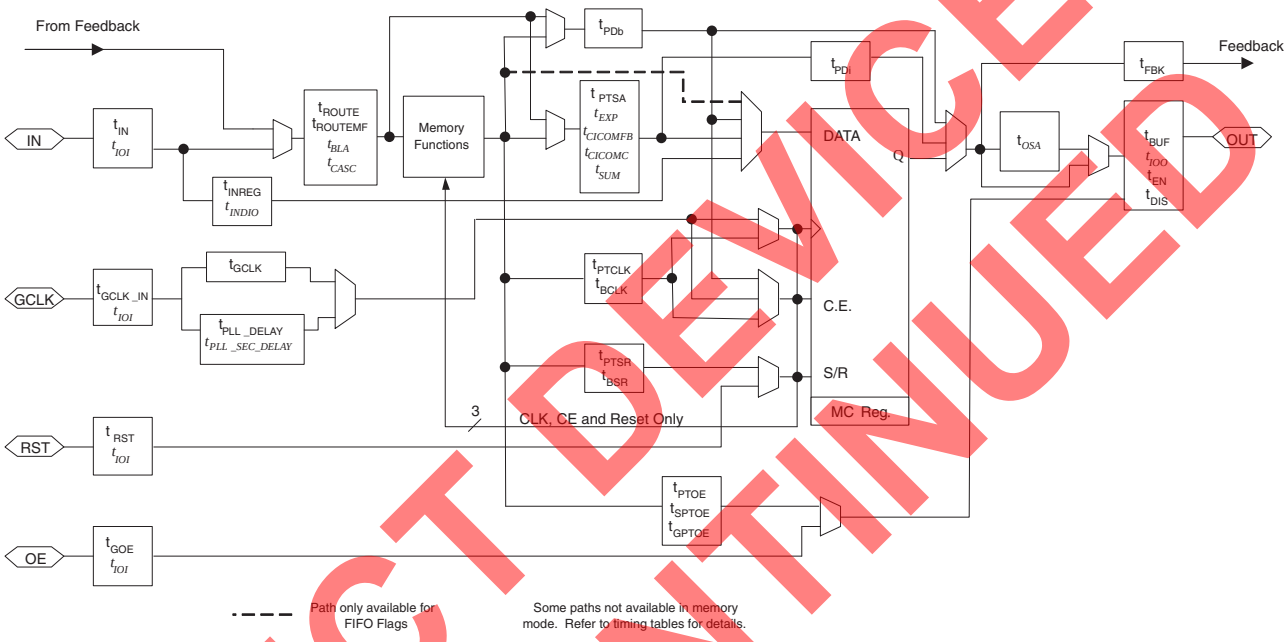
Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 51024						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	75	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	75	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	55	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

1. Device configured with 16-bit counters.
2. ICC varies with specific device configuration and operating frequency.
3. T_A = 25°C

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	96N	M12	M23	O23	M13	196	B5	A10
0	96P	M10	M22	O22	M11	197	A3	A9
0	97N	M8	M21	O21	M9	198	B4	C9
0	97P	M6	M20	O20	M7	199	B3	D9
0	98N	M5	M19	O19	—	200	C5	F9
0	98P	M4	M18	O18	—	201	C6	E9
0	99N	M2	M1	O1	M3	202	D5	A8
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	V_{CCO0}
0	99P	M0	M0	O0	M1	203	D6	B8
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	100N	N30	O29	—	N31	—	—	A7
0	100P	N28	O28	—	N29	—	—	B7
0	101N	N26	O27	—	N27	—	—	A5
0	101P	N24	O26	—	N25	—	—	B5
0	102N	N22	O25	—	N23	—	—	B6
0	102P	N21	O24	—	—	—	—	C7
0	103N	N20	O23	—	—	—	—	E8
0	103P	N18	O22	—	N19	—	—	E7
0	104N	N16	O21	—	N17	—	—	E6
0	104P	N14	O20	—	N15	—	—	D6
0	105N	N12	O19	—	N13	—	—	D8
—	—	V_{CCO0}	—	—	—	204	V_{CCO0}	V_{CCO0}
0	105P	N10	O18	—	N11	—	—	F8
—	—	GND (Bank 0)	—	—	—	205	GND (Bank 0)	GND (Bank 0)
0	106N	N8	O17	—	N9	—	—	F7
0	106P	N6	O16	—	N7	—	—	D7
0	107N	N5	O15	—	—	206	A2	C6
0	107P	N4	O14	—	—	207	B2	C5
0	108N	N2	O13	—	N3	—	—	C4
0	108P	N0	O12	—	N1	—	—	D5

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	B4
0	127P	S20	S10	T16	S21	E4	A4
0	128N	S18	Q17	S17	S19	B1	B3
0	128P	S16	Q16	S16	S17	C1	A3
0	129N	S14	Q15	S15	S15	D3	F5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	129P	S12	Q14	S14	S13	C2	G6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	130N	S10	Q13	S13	S11	E3	H6
0	130P	S8	Q12	S12	S9	D2	G5
0	131N	S6	S9	T14	S7	—	D3
0	131P	S4	S8	T12	S5	—	D2
0	132N	S2	S7	T10	S3	—	E4
-	-	VCC	-	-	-	VCC	VCC
0	132P	S0	S6	T8	S1	—	E3
-	-	GND	-	-	-	GND	GND
0	133N	T30	S5	T6	T31	—	F4
0	133P	T28	S4	T4	T29	—	G4
0	134N	T26	S3	T2	T27	—	C2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	134P	T24	S2	T0	T25	—	C1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	135N	T22	S1	-	T23	D1	F3
0	135P	T20	S0	-	T21	E1	G3
0	136N	T18	S31	-	T19	F4	H4
-	-	VCC	-	-	-	VCC	VCC
0	136P	T16	S30	-	T17	F5	J4
0	137N	T14	Q11	S11	T15	E2	H5
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	J5
0	138N	T10	Q9	S9	T11	F1	E2
0	138P	T8	Q8	S8	T9	G1	F2
-	-	GND	-	-	-	GND	GND
0	139N	T6	Q7	S7	T7	F3	D1
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	139P	T4	Q6	S6	T5	G5	E1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	140N	T2	Q5	S5	T3	H5	J3
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	H2
0	141N	U30	U31	W31	U31	G3	G2
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	G1
0	142N	U26	U29	W29	U27	—	J6
0	142P	U24	U28	W28	U25	—	K4

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	J6	T1
-	-	TDO	-	-	-	K2	V1
1	0P	A30/DATA0	C0	A0	A31	K3	W1
1	0N	A28/DATA1	C1	A1	A29	J3	Y1
1	1P	A26/DATA2	C2	A2	A27	J5	P3
1	1N	A24/DATA3	C3	A3	A25	J4	R3
1	2P	A22/DATA4	C4	A4	A23	L2	T2
1	2N	A20/DATA5	C5	A5	A21	M1	U2
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18/DATA6	C6	A6	A19	K4	V2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16/DATA7	C7	A7	A17	L3	W2
-	-	GND	-	-	-	GND	GND
1	4P	A14/INITB	C8	A8	A15	K5	R4
1	4N	A12/CSB	C9	A9	A13	L5	T4
1	5P	A10/READ	C10	A10	A11	N1	R6
1	5N	A8/CCLK	C11	A11	A9	M2	R5
1	6P	A6	-	-	A7	—	U3
-	-	VCC	-	-	-	VCC	VCC
1	6N	A4	-	-	A5	P1	V3
1	7P	A2	-	-	A3	M3	Y2
1	7N	A0	-	-	A1	L4	W3
1	8P	B30	D0	-	B31	N2	U5
1	8N	B28	D2	-	B29	P2	T5
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	9P	B26	D4	-	B27	R1	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	9N	B24	D6	-	B25	R2	V4
1	10P	B22	D8	-	B23	T2	AA3
1	10N	B20	D10	-	B21	T3	AB3
1	-	B18	D12	-	B19	—	Y4
-	-	DONE	-	-	-	M4	AA4
1	11P	B14	-	-	B15	—	AB2
1	11N	B12	-	-	B13	—	U6
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	12P	B10	-	-	B11	—	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	12N	B8	-	-	B9	—	W6
1	13P	B6	C12	A12	B7	N3	AB4
1	13N	B4	C13	A13	B5	P4	AB5
1	14P	B2	C14	A14	B3	N5	T6
1	14N	B0	C15	A15	B1	M6	U7
-	-	PROGRAMB	-	-	-	R3	W5

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	46N	G6	H19	-	G7	—	AB19
2	47P	G8	H20	-	G9	—	AA19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	47N	G10	H21	-	G11	—	U17
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	48P	G12	H22	-	G13	—	V18
2	48N	G14	H23	-	G15	—	AB21
2	49P	G16	H24	-	G17	—	U18
2	49N	G18	H25	-	G19	—	T17
2	50P	G20	H26	-	G21	R16	AB20
2	50N	G22	H27	-	G23	P16	AA20
2	51P	G24	H28	-	G25	N15	Y19
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	51N	G26	H29	-	G27	N14	V19
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	52P	G28	F16	H16	G29	N16	T18
2	52N	G30	F17	H17	G31	M16	R17
2	53P	H0	F18	H18	H1	M14	U19
2	53N	H2	F19	H19	H3	M15	T19
2	54P	H4	H30	E24	H5	—	V20
-	-	VCC	-	-	-	VCC	VCC
2	54N	H6	H31	E26	H7	—	U20
2	55P	H8	F20	H20	H9	L13	W20
2	55N	H10	F21	H21	H11	L12	Y21
2	56P	H12	F22	H22	H13	L15	R18
2	56N	H14	F23	H23	H15	L16	R19
-	-	GND	-	-	-	GND	GND
2	57P	H16	F24	H24	H17	L14	W21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	57N	H18	F25	H25	H19	K15	Y22
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	58P	H20	F26	H26	H21	K14	R20
2	58N	H22	F27	H27	H23	K12	P20
2	59P	H24	F28	H28	H25	K13	T21
2	59N	H26	F29	H29	H27	J13	R21
2	60P	H28	F30	H30	H29	J14	U21
2	60N	H30	F31	H31	H31	J12	V21
-	-	TOE	-	-	-	J15	W22
-	-	RESET	-	-	-	J11	V22
-	-	GOE0	-	-	-	H11	T22
-	-	GOE1	-	-	-	H13	R22
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 51024MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	159N	AA22	AA11	AB18	AA23	B4	C2
0	159P	AA20	AA10	AB16	AA21	A4	C1
0	160N	AA18	Y17	AA17	AA19	B3	D4
0	160P	AA16	Y16	AA16	AA17	A3	D3
0	161N	AA14	Y15	AA15	AA15	F5	D2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	161P	AA12	Y14	AA14	AA13	G6	D1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	162N	AA10	Y13	AA13	AA11	H6	E5
0	162P	AA8	Y12	AA12	AA9	G5	E4
0	163N	AA6	AA9	AB14	AA7	D3	E3
0	163P	AA4	AA8	AB12	AA5	D2	E2
0	164N	AA2	AA7	AB10	AA3	E4	E1
-	-	VCC	-	-	-	VCC	VCC
0	164P	AA0	AA6	AB8	AA1	E3	F2
-	-	GND	-	-	-	GND	GND
0	165N	AB30	AA5	AB6	AB31	F4	F5
0	165P	AB28	AA4	AB4	AB29	G4	G6
0	166N	AB26	AA3	AB2	AB27	C2	F4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	166P	AB24	AA2	AB0	AB25	C1	F3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	167N	AB22	AA1	-	AB23	F3	F1
0	167P	AB20	AA0	-	AB21	G3	G1
0	168N	AB18	AA31	-	AB19	H4	G5
-	-	VCC	-	-		VCC	VCC
0	168P	AB16	AA30	-	AB17	J4	G4
0	169N	AB14	Y11	AA11	AB15	H5	H7
0	169P	AB12/CLK_OUT0	Y10	AA10	AB13	J5	J7
0	170N	AB10	Y9	AA9	AB11	E2	G3
0	170P	AB8	Y8	AA8	AB9	F2	G2
-	-	GND	-	-	-	GND	GND
0	171N	AB6	Y7	AA7	AB7	D1	H6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	171P	AB4	Y6	AA6	AB5	E1	J6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	172N	AB2	Y5	AA5	AB3	J3	H5
0	172P	AB0/PLL_RST0	Y4	AA4	AB1	H2	H4
0	173N	AC30	AC31	AE31	AC31	G2	H3
0	173P	AC28/PLL_FBK0	AC30	AE30	AC29	G1	H2
0	174N	AC26	AC29	AE29	AC27	J6	H1
0	174P	AC24	AC28	AE28	AC25	K4	J1

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18

ispXPLD 5000MC (1.8V) Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5768MC	LC5768MC-5F256C	768	1.8	5.0	fpBGA	256	193	C
	LC5768MC-75F256C	768	1.8	7.5	fpBGA	256	193	C
	LC5768MC-5F484C	768	1.8	5.0	fpBGA	484	317	C
	LC5768MC-75F484C	768	1.8	7.5	fpBGA	484	317	C
LC51024MC	LC51024MC-52F484C	1024	1.8	5.2	fpBGA	484	317	C
	LC51024MC-75F484C	1024	1.8	7.5	fpBGA	484	317	C
	LC51024MC-52F672C	1024	1.8	5.2	fpBGA	672	381	C
	LC51024MC-75F672C	1024	1.8	7.5	fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5F256I	256	1.8	5.0	fpBGA	256	141	I
	LC5256MC-75F256I	256	1.8	7.5	fpBGA	256	141	I
LC5512MC	LC5512MC-75Q208I	512	1.8	7.5	PQFP	208	149	I
	LC5512MC-75F256I	512	1.8	7.5	fpBGA	256	193	I
	LC5512MC-75F484I	512	1.8	7.5	fpBGA	484	253	I
LC5768MC	LC5768MC-75F256I	768	1.8	7.5	fpBGA	256	193	I
	LC5768MC-75F484I	768	1.8	7.5	fpBGA	484	317	I
LC51024MC	LC51024MC-75F484I	1024	1.8	7.5	fpBGA	484	317	I
	LC51024MC-75F672I	1024	1.8	7.5	fpBGA	672	381	I

ispXPLD 5000MB (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4F256C	256	2.5	4.0	fpBGA	256	141	C
	LC5256MB-5F256C	256	2.5	5.0	fpBGA	256	141	C
	LC5256MB-75F256C	256	2.5	7.5	fpBGA	256	141	C
LC5512MB	LC5512MB-45Q208C	512	2.5	4.5	PQFP	208	149	C
	LC5512MB-75Q208C	512	2.5	7.5	PQFP	208	149	C
	LC5512MB-45F256C	512	2.5	4.5	fpBGA	256	193	C
	LC5512MB-75F256C	512	2.5	7.5	fpBGA	256	193	C
	LC5512MB-45F484C	512	2.5	4.5	fpBGA	484	253	C
	LC5512MB-75F484C	512	2.5	7.5	fpBGA	484	253	C
LC5768MB	LC5768MB-5F256C	768	2.5	5.0	fpBGA	256	193	C
	LC5768MB-75F256C	768	2.5	7.5	fpBGA	256	193	C
	LC5768MB-5F484C	768	2.5	5.0	fpBGA	484	317	C
	LC5768MB-75F484C	768	2.5	7.5	fpBGA	484	317	C
LC51024MB	LC51024MB-52F484C	1024	2.5	5.2	fpBGA	484	317	C
	LC51024MB-75F484C	1024	2.5	7.5	fpBGA	484	317	C
	LC51024MB-52F672C	1024	2.5	5.2	fpBGA	672	381	C
	LC51024MB-75F672C	1024	2.5	7.5	fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4FN256C	256	2.5	4.0	Lead-free fpBGA	256	141	C
	LC5256MB-5FN256C	256	2.5	5.0	Lead-free fpBGA	256	141	C
	LC5256MB-75FN256C	256	2.5	7.5	Lead-free fpBGA	256	141	C
LC5512MB	LC5512MB-45QN208C	512	2.5	4.5	Lead-free PQFP	208	149	C
	LC5512MB-75QN208C	512	2.5	7.5	Lead-free PQFP	208	149	C
	LC5512MB-45FN256C	512	2.5	4.5	Lead-free fpBGA	256	193	C
	LC5512MB-75FN256C	512	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5512MB-45FN484C	512	2.5	4.5	Lead-free fpBGA	484	253	C
	LC5512MB-75FN484C	512	2.5	7.5	Lead-free fpBGA	484	253	C
LC5768MB	LC5768MB-5FN256C	768	2.5	5.0	Lead-free fpBGA	256	193	C
	LC5768MB-75FN256C	768	2.5	7.5	Lead-free fpBGA	256	193	C
	LC5768MB-5FN484C	768	2.5	5.0	Lead-free fpBGA	484	317	C
	LC5768MB-75FN484C	768	2.5	7.5	Lead-free fpBGA	484	317	C
LC51024MB	LC51024MB-52FN484C	1024	2.5	5.2	Lead-free fpBGA	484	317	C
	LC51024MB-75FN484C	1024	2.5	7.5	Lead-free fpBGA	484	317	C
	LC51024MB-52FN672C	1024	2.5	5.2	Lead-free fpBGA	672	381	C
	LC51024MB-75FN672C	1024	2.5	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5FN256I	256	2.5	5.0	Lead-free fpBGA	256	141	I
	LC5256MB-75FN256I	256	2.5	7.5	Lead-free fpBGA	256	141	I
LC5512MB	LC5512MB-75QN208I	512	2.5	7.5	Lead-free PQFP	208	149	I
	LC5512MB-75FN256I	512	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5512MB-75FN484I	512	2.5	7.5	Lead-free fpBGA	484	253	I
LC5768MB	LC5768MB-75FN256I	768	2.5	7.5	Lead-free fpBGA	256	193	I
	LC5768MB-75FN484I	768	2.5	7.5	Lead-free fpBGA	484	317	I
LC51024MB	LC51024MB-75FN484I	1024	2.5	7.5	Lead-free fpBGA	484	317	I
	LC51024MB-75FN672I	1024	2.5	7.5	Lead-free fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4FN256C	256	3.3	4.0	Lead-free fpBGA	256	141	C
	LC5256MV-5FN256C	256	3.3	5.0	Lead-free fpBGA	256	141	C
	LC5256MV-75FN256C	256	3.3	7.5	Lead-free fpBGA	256	141	C

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
December 2003	07	Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers).
		Updated ispXPLD 5000MX timing numbers (version v.1.7).
		Added lead-free package designator.
		Removed ispXPLD 5000MC industrial temperature grade ordering part numbers.
January 2004	08	Lead-free package release for the ispXPLD 5000MC and 5000MV devices.
		Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers).
March 2004	08.1	Updated the MFB Cascade Chain table for the ispXPLD 5256MX device.
May 2004	09	Updated the ispXPLD 5000MX timig numbers (version v.1.8) ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release
		Updated typical supply current data and condition.
		ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14.
August 2004	10	Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ.
		Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free).
October 2004	10.1	Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer)
November 2004	11	Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers.
December 2004	11.1	Pin name RESETB has been updated to RESET.
March 2005	12	208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices.
April 2005	12.1	Page 23, clarification of footnote regarding IDK specification.
March 2006	12.2	Signal description for RESET has been updated.
April 2009	12.3	Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format.
February 2010	12.4	References to "system gates" changed to "functional gates."