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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	193
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768mb-75f256i

Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width support.

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	H -> G -> F -> E
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

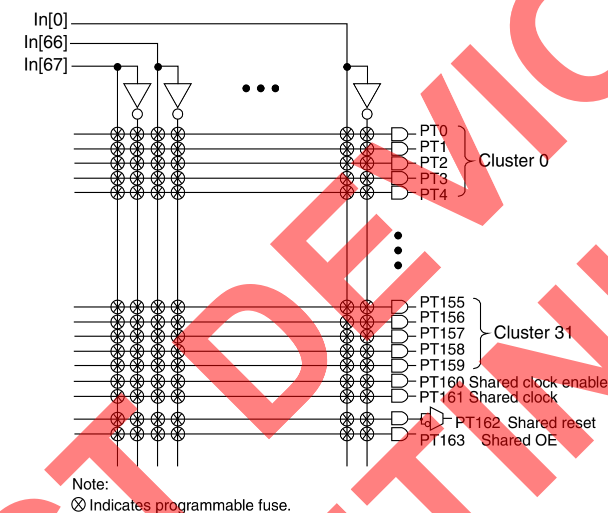
SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array



Dual-OR Array (Including Arithmetic Support)

The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

True Dual-Port SRAM Mode

In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two independent read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are supported by the MFB. Figure 9 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Resets are asynchronous. All inputs on the same port share the same clock, clock enable, and reset selections. All outputs on the same port share the same clock, clock enable, and reset selections. Selections may be made independently between both inputs and outputs and ports. Table 5 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 9. Dual-Port SRAM Block Diagram

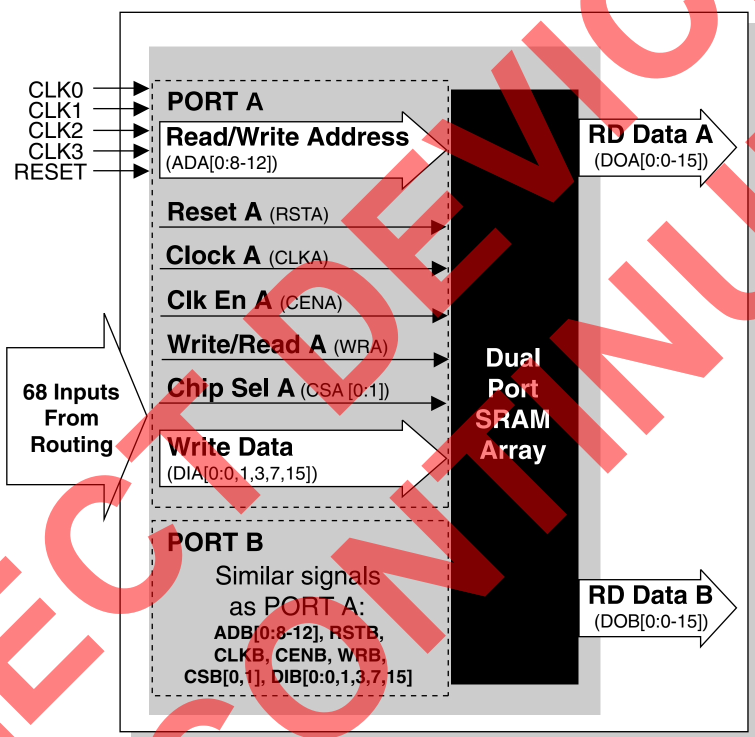


Table 5. Register Clock, Clock Enable, and Reset in Dual-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLKA (CLKB) or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	CENA (CENB) or one of the global clocks (CLK1 - CLK 2). The selected signal can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RSTA (RSTB). RSTA (RSTB) can be inverted is desired.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Registered Delays													
t_S	D-Register Setup Time, Global Clock	—	0.28	—	0.31	—	0.35	—	0.55	—	0.52	—	ns
t_{S_PT}	D-Register Setup Time, PT Clock	—	-0.13	—	-0.11	—	-0.10	—	-0.10	—	-0.07	—	ns
t_H	D-Register Hold Time	—	1.90	—	2.56	—	2.50	—	2.40	—	4.00	—	ns
t_{COi}	Register Clock to OSA Time	—	—	0.72	—	1.03	—	0.68	—	0.93	—	1.50	ns
t_{CESi}	Clock Enable Setup Time	—	1.07	—	1.20	—	1.33	—	1.33	—	2.00	—	ns
t_{CEHi}	Clock Enable Hold Time	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{SIR}	D-Input Register Setup Time, Global Clock	—	0.66	—	0.20	—	0.53	—	0.12	—	0.08	—	ns
t_{SIR_PT}	D-Input Register Setup Time, PT Clock	—	0.42	—	0.37	—	0.34	—	0.34	—	0.22	—	ns
t_{HIR}	D-Input Register Hold Time, Global Clock	—	0.84	—	1.31	—	1.01	—	1.41	—	2.91	—	ns
t_{HIR_PT}	D-Input Register Hold Time, PT Clock	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
Latched Delays													
t_{SL}	Latch Setup Time, Global Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{SL_PT}	Latch Setup Time, PT Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.34	—	ns
t_{HL}	Latch Hold Time	—	-0.06	—	0.00	—	0.00	—	0.00	—	-0.03	—	ns
t_{GOi}	Latch Gate to OSA Time	—	—	0.07	—	0.08	—	0.08	—	0.08	—	0.13	ns
t_{PDLi}	Propagation Delay through Latch to OSA Transparent	—	—	0.52	—	0.58	—	0.65	—	0.65	—	0.97	ns
Reset and Set Delays													
t_{SRi}	Asynchronous Reset or Set to OSA Delay	—	—	0.23	—	0.26	—	0.29	—	0.29	—	0.43	ns
t_{SRR}	Asynchronous Reset or Set Recovery	—	—	0.42	—	0.47	—	0.53	—	0.55	—	0.79	ns
eXtended Function Routing Delays													
$t_{ROUTEMF}$	Delay through SRP when Implementing Memory Functions	—	—	2.00	—	2.25	—	2.51	—	2.61	—	3.76	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	"Don't Care" Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	"Don't Care" Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

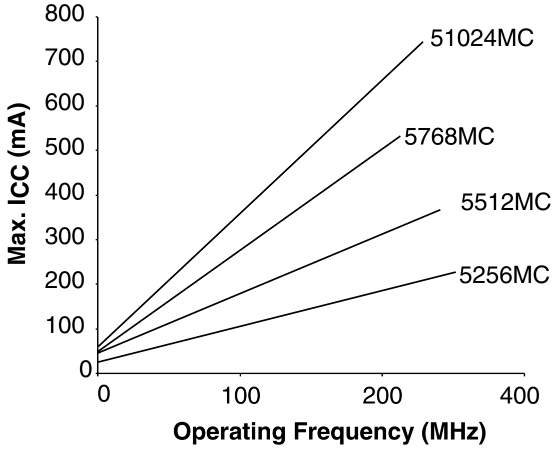
Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—	8.54	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
Dual Port RAM													
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84	—	ns
t_{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27	—	ns
$t_{DPADDAS}$	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPADDAH}$	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATAAS}$	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{DPDATAAH}$	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4 Min.	-4 Max.	-45 Min.	-45 Max.	-5 Min.	-5 Max.	-52 Min.	-52 Max.	-75 Min.	-75 Max.	Units
t_{IOI} **Input Adjusters**													
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t_{IOO} **Output Adjusters – Output Signal Modifiers**													
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t_{IOO} **Output Adjusters – Output Configurations**													
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

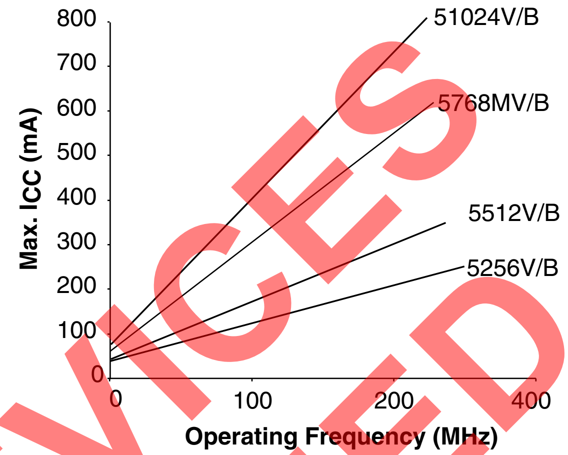
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Power Estimation Equations

ICC = ICC_DC + IMFB_CPLD + IMFB_ SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL_D

ICC_DC
Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) from the data sheet.

IMFB_CPLD
= ((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** * CPLD GRP from IFB) * AF+ **K4**) * FREQ / 1000µA/mA

IMFB_CAM
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

IMFB_ SRAM/PDPRAM/FIFO
= (WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (**K1** + 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * SRAM/PDPRAM/FIFO Memory MFBs * FREQ / 1000µA/mA

IMFB_ DPRAM
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs * FREQ / 1000µA/mA

IPLL_D
= **K5** * PLL_FREQ * number of PLLs used. IPPL_D is the PLL digital component of the VCC supply current.

Analog portion of PLL supply current consumption, from PLL power pin:

IPLL_A = (**K6** * PLL_FREQ + **K7**) * number of PLLs used

Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the IEEE 1149.1 state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data out.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the registers in the device. The global polarity for this pin is selectable on a global basis.þ The default is active low. An external pull-down is required when polarity is set to active high.
yzz	Input/Output – These are the general purpose I/O used by the logic array. *y* is the MFB reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs (see Figure 14 for differential pairing).
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GNDP	GND – Ground for PLLs.
V_{CCP}	V_{CC} – The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG interface.
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2CMOS or IEEE 1149.1 TAP.
PROGRAMB	Input – Controls the programming of SRAM. Hold high for normal operation. Toggle low to reload SRAM from E^2 memory.
CCLK[1]	Input – Clock for sysCONFIG interface. Reads and writes occur on the rising edge of the clock.
READ[1]	Input – Drive high to perform reads from the sysCONFIG interface.
INITB	I/O – Indicates status of configuration. Can be driven low to inhibit configuration.
DONE	Output (open drain) – Indicates status of configuration.

1. These inputs should not toggle during power up for proper power-up configuration.

ispXPLD 5000MX Power Supply and NC Connections[1]

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	34N	E30	-	-	E31	H14
3	34P	E28	-	-	E29	G16
3	35N	E26	-	-	E27	G15
3	35P	E24/PLL_FBK1	-	-	E25	F15
3	36N	E22/PLL_RST1	E27	F27	E23	H12
3	36P	E21	E26	F26	-	G14
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	37N	E20	E25	F25	-	F16
-	-	VCCO3	-	-	-	VCCO3
3	37P	E18	E24	F24	E19	E16
-	-	GND	-	-	-	GND
3	38N	E16	E23	F23	E17	G13
3	38P	E14	E22	F22	E15	G12
3	39N	E12	E21	F21	E13	F14
3	39P	E10/CLK_OUT1	E20	F20	E11	E15
-	-	VCC	-	-	-	VCC
3	40N	E8	E19	F19	E9	D12
3	40P	E6	E18	F18	E7	B14
3	41N	E5	E17	F17	-	C13
3	41P	E4	E16	F16	-	A14
3	42N	E2	E31	F31	E3	A13
3	42P	E0	E30	F30	E1	B13
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
-	-	VCCO3	-	-	-	VCCO3
3	43N	F30	E15	F15	F31	B11
3	43P	F28	E14	F14	F29	C11
3	44N	F26	E13	F13	F27	B10
3	44P	F24	E12	F12	F25	A10
3	45N	F22	E11	F11	F23	C10
3	45P	F21	E10	F10	-	D10
3	46N	F20	E9	F9	-	C9
3	46P	F18	E8	F8	F19	E9
3	47N	F16/VREF3	E29	F29	F17	D9
3	47P	F14	E28	F28	F15	F9
3	48N	F12	E7	F7	F13	A9
3	48P	F10	E6	F6	F11	F8
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	49N	F8	E5	F5	F9	E8
-	-	VCCO3	-	-	-	VCCO3
3	49P	F6	E4	F4	F7	A8
3	50N	F5	E3	F3	-	B9
3	50P	F4	E2	F2	-	D8
-	-	VCC	-	-	-	VCC

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	51N	F2	E1	F1	F3	B8
3	51P	F0	E0	F0	F1	C8
0	52N	G30	G31	H31	G31	B7
0	52P	G28	G30	H30	G29	A7
-	-	GND	-	-	-	NC
0	53N	G26	G29	H29	G27	D7
0	53P	G24	G28	H28	G25	C7
0	54N	G22	G27	H27	G23	B6
-	-	VCCO0	-	-	-	VCCO0
0	54P	G21	G26	H26	-	E7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	55N	G20	G25	H25	-	E6
0	55P	G18	G24	H24	G19	A6
0	56N	G16/VREF0	G3	H3	G17	A5
0	56P	G14	G2	H2	G15	A4
0	57N	G12	G23	H23	G13	B5
0	57P	G10	G22	H22	G11	A3
0	58N	G8	G21	H21	G9	B4
0	58P	G6	G20	H20	G7	B3
0	59N	G5	G19	H19	-	C5
0	59P	G4	G18	H18	-	C6
0	60N	G2	G1	H1	G3	D5
0	60P	G0	G0	H0	G1	D6
-	-	VCCO0	-	-	-	VCCO0
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10[1]	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	96N	M12	M23	O23	M13	196	B5	A10
0	96P	M10	M22	O22	M11	197	A3	A9
0	97N	M8	M21	O21	M9	198	B4	C9
0	97P	M6	M20	O20	M7	199	B3	D9
0	98N	M5	M19	O19	—	200	C5	F9
0	98P	M4	M18	O18	—	201	C6	E9
0	99N	M2	M1	O1	M3	202	D5	A8
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	V_{CCO0}
0	99P	M0	M0	O0	M1	203	D6	B8
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	100N	N30	O29	—	N31	—	—	A7
0	100P	N28	O28	—	N29	—	—	B7
0	101N	N26	O27	—	N27	—	—	A5
0	101P	N24	O26	—	N25	—	—	B5
0	102N	N22	O25	—	N23	—	—	B6
0	102P	N21	O24	—	—	—	—	C7
0	103N	N20	O23	—	—	—	—	E8
0	103P	N18	O22	—	N19	—	—	E7
0	104N	N16	O21	—	N17	—	—	E6
0	104P	N14	O20	—	N15	—	—	D6
0	105N	N12	O19	—	N13	—	—	D8
—	—	V_{CCO0}	—	—	—	204	V_{CCO0}	V_{CCO0}
0	105P	N10	O18	—	N11	—	—	F8
—	—	GND (Bank 0)	—	—	—	205	GND (Bank 0)	GND (Bank 0)
0	106N	N8	O17	—	N9	—	—	F7
0	106P	N6	O16	—	N7	—	—	D7
0	107N	N5	O15	—	—	206	A2	C6
0	107P	N4	O14	—	—	207	B2	C5
0	108N	N2	O13	—	N3	—	—	C4
0	108P	N0	O12	—	N1	—	—	D5

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	B4
0	127P	S20	S10	T16	S21	E4	A4
0	128N	S18	Q17	S17	S19	B1	B3
0	128P	S16	Q16	S16	S17	C1	A3
0	129N	S14	Q15	S15	S15	D3	F5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	129P	S12	Q14	S14	S13	C2	G6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	130N	S10	Q13	S13	S11	E3	H6
0	130P	S8	Q12	S12	S9	D2	G5
0	131N	S6	S9	T14	S7	—	D3
0	131P	S4	S8	T12	S5	—	D2
0	132N	S2	S7	T10	S3	—	E4
-	-	VCC	-	-	-	VCC	VCC
0	132P	S0	S6	T8	S1	—	E3
-	-	GND	-	-	-	GND	GND
0	133N	T30	S5	T6	T31	—	F4
0	133P	T28	S4	T4	T29	—	G4
0	134N	T26	S3	T2	T27	—	C2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	134P	T24	S2	T0	T25	—	C1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	135N	T22	S1	-	T23	D1	F3
0	135P	T20	S0	-	T21	E1	G3
0	136N	T18	S31	-	T19	F4	H4
-	-	VCC	-	-	-	VCC	VCC
0	136P	T16	S30	-	T17	F5	J4
0	137N	T14	Q11	S11	T15	E2	H5
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	J5
0	138N	T10	Q9	S9	T11	F1	E2
0	138P	T8	Q8	S8	T9	G1	F2
-	-	GND	-	-	-	GND	GND
0	139N	T6	Q7	S7	T7	F3	D1
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	139P	T4	Q6	S6	T5	G5	E1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	140N	T2	Q5	S5	T3	H5	J3
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	H2
0	141N	U30	U31	W31	U31	G3	G2
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	G1
0	142N	U26	U29	W29	U27	—	J6
0	142P	U24	U28	W28	U25	—	K4

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	143N	U22	U27	W27	U23	—	K6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	U20	U26	W26	U21	—	K3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	U18	U25	W25	U19	—	K5
0	144P	U16	U24	W24	U17	—	K2
0	145N	U14	U23	W23	U15	—	L5
0	145P	U12	U22	W22	U13	—	K1
0	146N	U10	U21	W21	U11	—	L6
0	146P	U8	U20	W20	U9	—	L1
0	147N	U6	U19	W19	U7	—	M5
0	147P	U4	U18	W18	U5	—	L2
0	148N	U2	U17	W17	U3	—	N5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	148P	U0	U16	W16	U1	—	L3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	149N	W30	U15	W15	W31	—	M6
0	149P	W28	U14	W14	W29	—	M2
0	150N	W26	U13	W13	W27	—	P5
-	-	VCC	-	-	-	VCC	VCC
0	150P	W24	U12	W12	W25	—	P6
0	151N	W22	U11	W11	W23	—	M3
0	151P	W20	U10	W10	W21	—	N6
0	152N	W18	U9	W9	W19	—	N2
0	152P	W16	U8	W8	W17	—	P1
-	-	GND	-	-	-	GND	GND
0	153N	W14	U7	W7	W15	—	N3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	153P	W12	U6	W6	W13	—	M8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	154N	W10	U5	W5	W11	—	N8
0	154P	W8	U4	W4	-	—	P2
0	155N	W6	U3	W3	W7	—	P8
0	155P	W4	U2	W2	W5	—	N4
0	156N	W2	U1	W1	W3	G2	H1
0	156P	W0	U0	W0	W1	H1	J1
-	GCLK0P	GCLK0	-	-	-	H2	N7
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	J2	P7
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	H6	R1
-	-	TMS	-	-	-	H4	R2

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	63P	K8	L20	-	K9	AA19	AA18
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	63N	K10	L21	-	K11	U17	Y18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	64P	K12	L22	-	K13	V18	AD25
2	64N	K14	L23	-	K15	AB21	AD26
2	65P	K16	L24	-	K17	U18	AC23
2	65N	K18	L25	-	K19	T17	AC24
2	66P	K20	L26	-	K21	AB20	AC25
2	66N	K22	L27	-	K23	AA20	AC26
2	67P	K24	L28	-	K25	Y19	AB22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	67N	K26	L29	-	K27	V19	AB23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	68P	K28	J16	L16	K29	T18	AB24
2	68N	K30	J17	L17	K31	R17	AB25
2	69P	L0	J18	L18	L1	U19	AB26
2	69N	L2	J19	L19	L3	T19	AA26
2	70P	L4	L30	I24	L5	V20	AA22
-	-	VCC	-	-	-	VCC	VCC
2	70N	L6	L31	I26	L7	U20	Y21
2	71P	L8	J20	L20	L9	W20	AA23
2	71N	L10	J21	L21	L11	Y21	AA24
2	72P	L12	J22	L22	L13	R18	AA25
2	72N	L14	J23	L23	L15	R19	Y26
-	-	GND	-	-	-	GND	GND
2	73P	L16	J24	L24	L17	W21	Y22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	73N	L18	J25	L25	L19	Y22	Y23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	74P	L20	J26	L26	L21	R20	W20
2	74N	L22	J27	L27	L23	P20	V20
2	75P	L24	J28	L28	L25	T21	W21
2	75N	L26	J29	L29	L27	R21	V21
2	76P	L28	J30	L30	L29	U21	Y24
2	76N	L30	J31	L31	L31	V21	Y25
2	77P	N0	P0	N0	N1	—	W22
2	77N	N2	P1	N1	N3	—	W23
2	78P	N4	P2	N2	N5	—	W24
-	-	VCC	-	-	-	VCC	VCC
2	78N	N6	P3	N3	N7	—	W25
-	-	GND	-	-	-	GND	GND
2	79P	N8	P4	N4	N9	—	W26

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193	I
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193	C
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193	C
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317	C
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193	I
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I