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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	2.3V ~ 2.7V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	317
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768mb-75f484i

Figure 1. ispXPLD 5000MX Block Diagram

SELECT DEVICES DISCONTINUED

Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

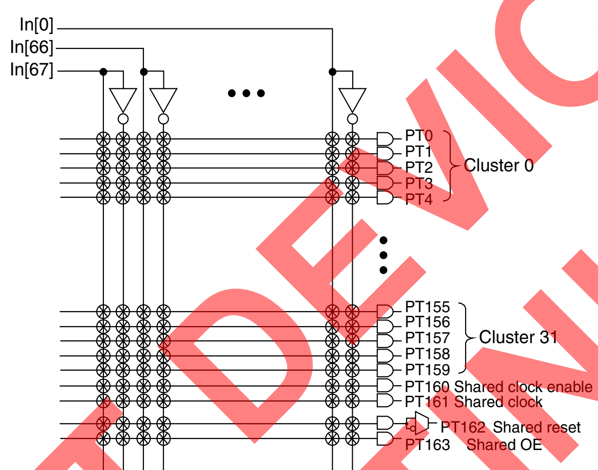
Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array



Note:
⊗ Indicates programmable fuse.

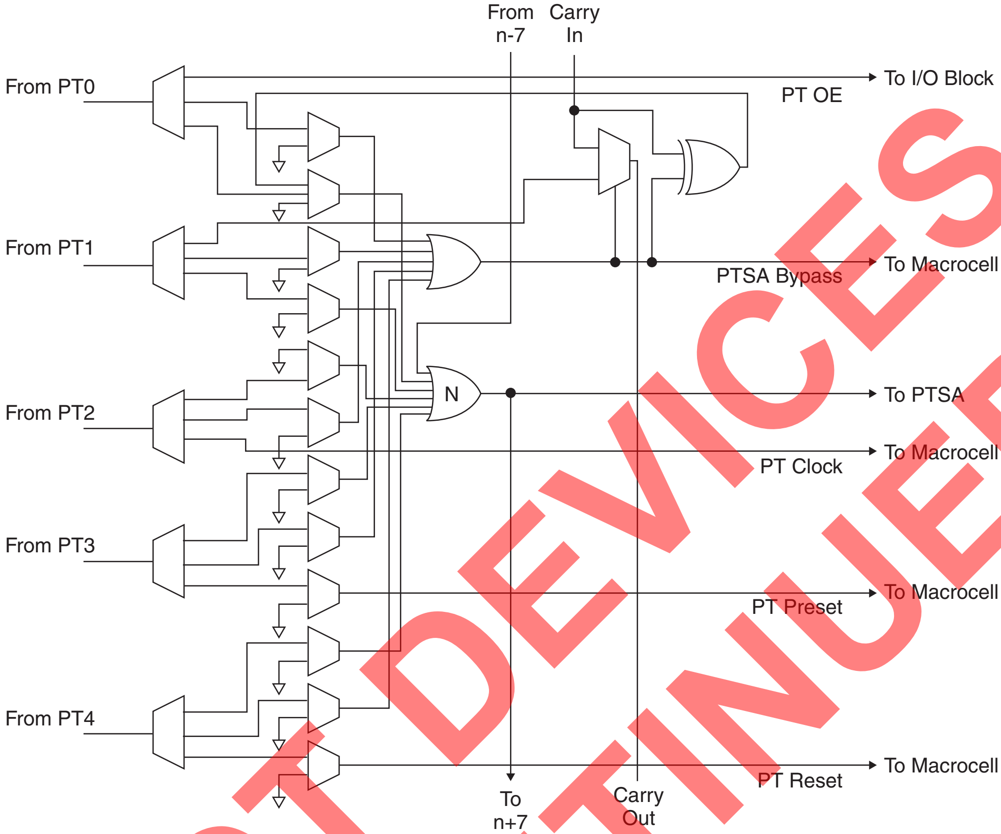
Dual-OR Array (Including Arithmetic Support)

The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

SELECT DEVICES DISCONTINUED

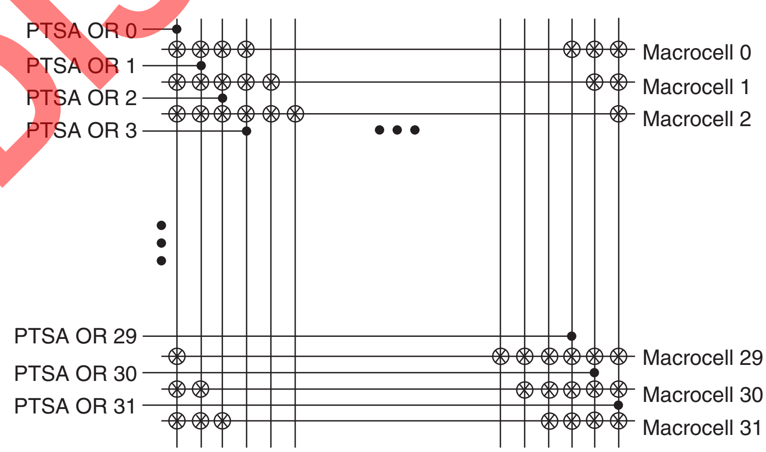
Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

Figure 7. Product Term Sharing Array (PTSA)



SELECT DEVICES DISCONTINUED

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

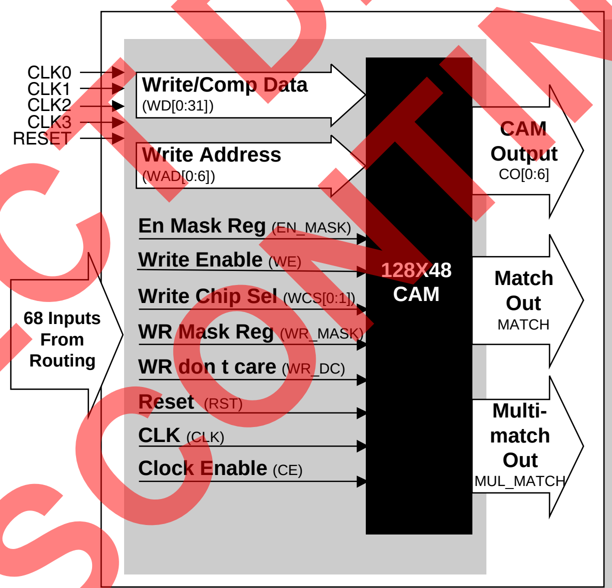


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

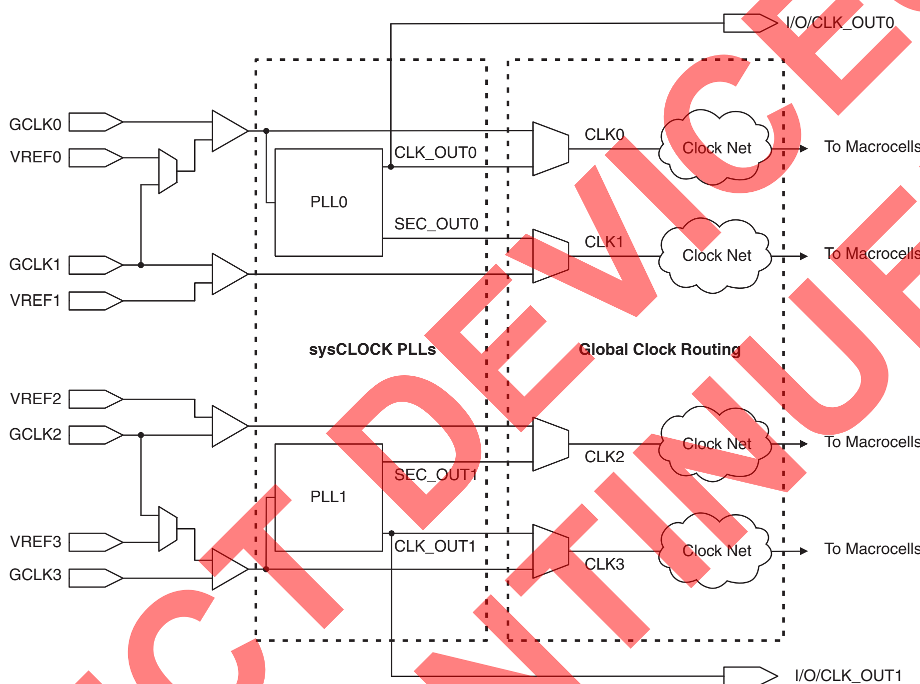
Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

SELECT DEVICES DISCONTINUED

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

SELECT DEVICES DISCONTINUED

Figure 15. PLL Block Diagram

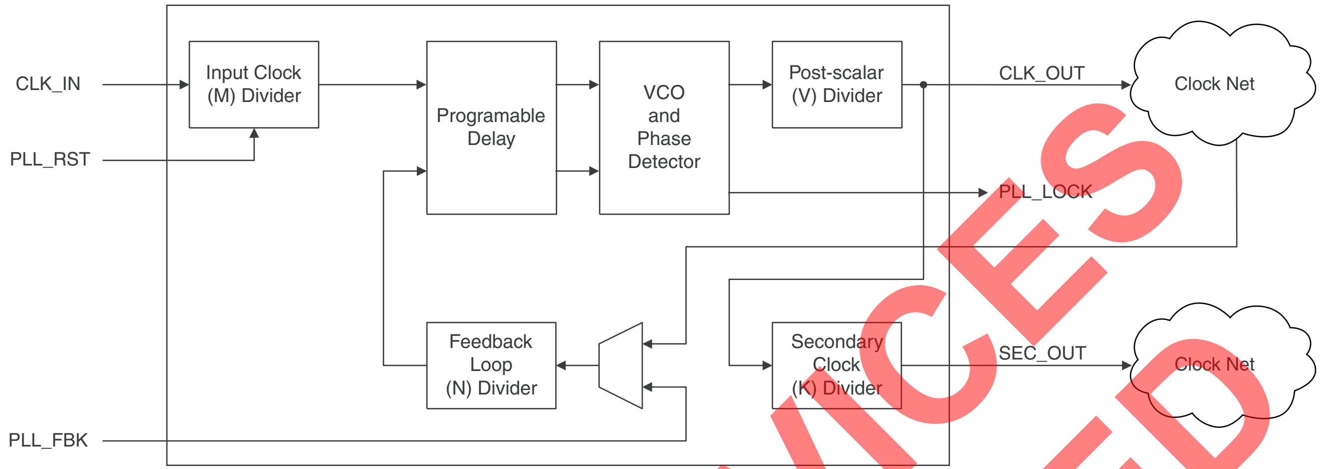
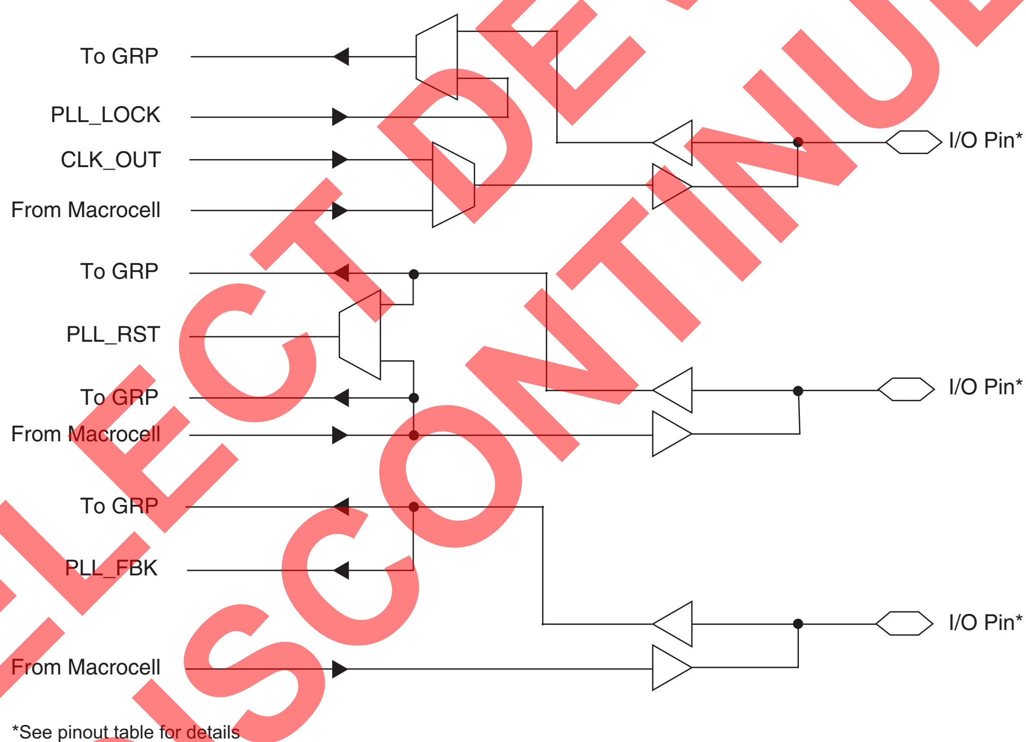


Figure 16. Connection of Optional PLL Inputs and Outputs



SELECT DEVICES DISCONTINUED

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices.

Figure 17. I/O Cell

Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 12 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}. For more information on the sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays													
t_{IN}	Input Buffer Delay	—	—	0.70	—	0.91	—	0.96	—	1.11	—	1.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.40	—	0.35	—	0.35	—	0.35	—	0.55	ns
t_{RST}	Global RESET Pin Delay	—	—	3.77	—	4.24	—	4.71	—	4.71	—	7.07	ns
t_{GOE}	Global OE Pin Delay	—	—	1.98	—	2.66	—	2.34	—	2.87	—	3.27	ns
t_{BUF}	Delay through Output Buffer	—	—	1.16	—	1.30	—	1.45	—	1.60	—	2.17	ns
t_{EN}	Output Enable Time	—	—	2.52	—	2.84	—	3.16	—	3.63	—	4.23	ns
t_{DIS}	Output Disable Time	—	—	1.92	—	2.40	—	2.40	—	2.40	—	3.60	ns
Routing Delays													
t_{ROUTE}	Delay through SRP	—	—	1.95	—	2.06	—	2.34	—	2.24	—	3.66	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.60	—	0.60	—	0.60	—	0.47	—	1.63	ns
t_{PTSA}	Product Term Sharing Array Delay	—	—	0.50	—	0.50	—	0.53	—	0.83	—	1.34	ns
t_{FBK}	Internal Feedback Delay	—	—	0.19	—	0.02	—	0.39	—	0.03	—	0.60	ns
t_{GCLK}	Global Clock Tree Delay	—	—	0.52	—	0.32	—	0.72	—	0.82	—	0.78	ns
t_{BCLK}	Block PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.30	—	0.30	—	0.30	—	0.30	ns
t_{BSR}	Block PT Reset Delay	—	—	0.72	—	0.81	—	0.90	—	0.94	—	1.35	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	—	0.60	—	0.75	—	0.75	—	0.75	—	1.13	ns
t_{LPTOE}	Macrocell PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t_{SPTOE}	Segment PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t_{OSA}	Output Sharing Array Delay	—	—	0.80	—	0.90	—	1.00	—	1.00	—	1.50	ns
t_{PTOE}	Global PT OE Delay	—	—	0.83	—	1.04	—	1.04	—	1.04	—	1.56	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	—	0.20	—	0.23	—	0.25	—	0.25	—	0.38	ns
t_{PDI}	Macrocell Propagation Delay	—	—	0.50	—	0.93	—	0.72	—	0.72	—	1.04	ns

SELECT DEVICES DISCONTINUED

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	"Don't Care" Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	"Don't Care" Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

SELECT DEVICES DISCONTINUED

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

SELECT DEVICES DISCONTINUED

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	51N	F2	E1	F1	F3	B8
3	51P	F0	E0	F0	F1	C8
0	52N	G30	G31	H31	G31	B7
0	52P	G28	G30	H30	G29	A7
-	-	GND	-	-	-	NC
0	53N	G26	G29	H29	G27	D7
0	53P	G24	G28	H28	G25	C7
0	54N	G22	G27	H27	G23	B6
-	-	VCCO0	-	-	-	VCCO0
0	54P	G21	G26	H26	-	E7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	55N	G20	G25	H25	-	E6
0	55P	G18	G24	H24	G19	A6
0	56N	G16/VREF0	G3	H3	G17	A5
0	56P	G14	G2	H2	G15	A4
0	57N	G12	G23	H23	G13	B5
0	57P	G10	G22	H22	G11	A3
0	58N	G8	G21	H21	G9	B4
0	58P	G6	G20	H20	G7	B3
0	59N	G5	G19	H19	-	C5
0	59P	G4	G18	H18	-	C6
0	60N	G2	G1	H1	G3	D5
0	60P	G0	G0	H0	G1	D6
-	-	VCCO0	-	-	-	VCCO0
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

SELECT DEVICES DISCONTINUED

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	V_{CCO2}
2	29N	E10	F5	H5	E11	86	M10	U12
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	GND (Bank 2)
2	30P	E12	F6	H6	E13	88	M11	AB13
2	30N	E16	F7	H7	E17	89	T13	Y13
2	31P	E18	—	—	E19	90	P11	V13
2	31N	E20/V_{REF2}	—	—	E21	91	T14	W13
2	32P	E22	F8	H8	E23	92	R12	V14
2	32N	E24	F9	H9	E25	93	R13	W14
2	33P	E26	F10	H10	E27	94	N11	Y14
2	33N	E28	F11	H11	E29	95	T15	AB14
2	34P	F0	F12	H12	F1	96	R14	AB15
2	34N	F2	F13	H13	F3	97	N12	AA15
2	35P	F4	F14	H14	F5	98	P12	U13
—	—	V_{CCO2}	—	—	—	—	V_{CCO2}	V_{CCO2}
2	35N	F6	F15	H15	F7	99	R15	U14
—	—	GND (Bank 2)	—	—	—	—	GND (Bank 2)	GND (Bank 2)
2	36P	F8	E0	—	F9	—	—	W15
2	36N	F10	E2	—	F11	—	—	W16
2	37P	F12	E4	—	F13	—	—	Y16
2	37N	F16	E6	—	F17	—	—	AA16
2	38P	F18	E8	—	F19	—	—	AB16
2	38N	F20	E10	—	F21	—	—	AA17
2	39P	F22	E12	—	F23	—	—	Y17
2	39N	F24	E16	—	F25	—	—	AA18
2	40P	F26	E20	—	F27	—	—	W17
2	40N	F28	E22	—	F29	—	—	W18
2	41P	G0	—	—	G1	—	—	V15
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	V_{CCO2}
2	41N	G2	—	—	G3	—	—	U15
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	GND (Bank 2)
2	42P	G4	—	—	G5	102	P13	Y18
2	42N	G6	—	—	G7	103	P15	V17
2	43P	G8	—	—	G9	—	M13	V16
2	43N	G10	—	—	G11	—	P14	U16
2	44P	G12	—	—	G13	—	—	AB18
2	44N	G14	—	—	G15	—	—	AB19
2	45P	G16	—	—	G17	—	—	U18
2	45N	G18	—	—	G19	—	—	T17
2	46P	G20	—	—	G21	104	R16	AB20
2	46N	G22	—	—	G23	105	P16	AA20
2	47P	G24	—	—	G25	106	N15	Y19
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	V_{CCO2}

SELECT DEVICES DISCONTINUED

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	61N	I14	I23	K23	I15	149	G13	D22
3	61P	I12	I22	K22	I13	150	G12	D21
3	62N	I10	I21	K21	I11	151	F14	J20
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	J19
3	63N	I6	K31	—	I7	—	F12	E20
—	—	V_{CC}	—	—	—	153	VCC	VCC
3	63P	I4	K30	L30	I5	—	F13	F20
3	64N	I2	K29	L28	I3	—	D16	H17
3	64P	I0	K28	L26	I1	—	D15	H18
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	65N	J30	K27	—	J31	—	—	J18
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	65P	J28	K26	—	J29	—	—	H19
3	66N	J26	K25	—	J27	—	—	G20
3	66P	J24	K24	—	J25	—	—	G19
3	67N	J22	K23	—	J23	—	—	C22
3	67P	J20	K22	—	J21	—	—	C21
3	68N	J18	K21	—	J19	—	—	D20
3	68P	J16	K20	—	J17	—	—	C19
3	69N	J14	K19	—	J15	—	C16	F19
3	69P	J12	K18	—	J13	—	B16	E19
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	70N	J10	K17	—	J11	—	C15	G18
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	70P	J8	K16	—	J9	—	B15	F18
3	71N	J6	K15	—	J7	—	E14	B20
3	71P	J4	K14	—	J5	—	D14	B19
3	72N	J2	K13	—	J3	—	E13	A20
3	72P	J0	K12	—	J1	—	A15	A19
3	73N	K30	I19	K19	K31	154	D12	D18
3	73P	K28	I18	K18	K29	155	B14	C18
3	74N	K26	I17	K17	K27	156	C13	G17
3	74P	K24	I16	K16	K25	157	A14	F16
3	75N	K22	I31	K31	K23	158	A13	E17
3	75P	K21	I30	K30	—	159	B13	D17
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	GND (Bank 3)
3	76N	K20	K11	L21	—	—	D11	B18
—	—	V_{CCO3}	—	—	—	161	V_{CCO3}	V_{CCO3}
3	76P	K18	K10	L20	K19	—	B12	A18
3	77N	K16	K9	L18	K17	—	C12	C17
3	77P	K14	K8	L16	K15	—	E11	B17
3	78N	K12	K7	L12	K13	—	—	C16
3	78P	K10	K6	L10	K11	—	—	B16

SELECT DEVICES DISCONTINUED

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	F13
3	79P	K6	K4	L6	K7	—	—	F15
3	80N	K5	K3	L5	—	—	—	D16
3	80P	K4	K2	L4	—	—	E10[1]	E16
3	81N	K2	K1	L2	K3	—	A12	A16
3	81P	K0	K0	L0	K1	—	A11	A15
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	—	GND
—	—	GND	—	—	—	—	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10

SELECT DEVICES DISCONTINUED

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	—	AA6
1	18N	C12	-	-	C13	—	AA7
1	19P	C10	-	-	C11	—	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

SELECT DEVICES DISCONTINUED

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

SELECT DEVICES DISCONTINUED

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	63P	K8	L20	-	K9	AA19	AA18
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	63N	K10	L21	-	K11	U17	Y18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	64P	K12	L22	-	K13	V18	AD25
2	64N	K14	L23	-	K15	AB21	AD26
2	65P	K16	L24	-	K17	U18	AC23
2	65N	K18	L25	-	K19	T17	AC24
2	66P	K20	L26	-	K21	AB20	AC25
2	66N	K22	L27	-	K23	AA20	AC26
2	67P	K24	L28	-	K25	Y19	AB22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	67N	K26	L29	-	K27	V19	AB23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	68P	K28	J16	L16	K29	T18	AB24
2	68N	K30	J17	L17	K31	R17	AB25
2	69P	L0	J18	L18	L1	U19	AB26
2	69N	L2	J19	L19	L3	T19	AA26
2	70P	L4	L30	I24	L5	V20	AA22
-	-	VCC	-	-	-	VCC	VCC
2	70N	L6	L31	I26	L7	U20	Y21
2	71P	L8	J20	L20	L9	W20	AA23
2	71N	L10	J21	L21	L11	Y21	AA24
2	72P	L12	J22	L22	L13	R18	AA25
2	72N	L14	J23	L23	L15	R19	Y26
-	-	GND	-	-	-	GND	GND
2	73P	L16	J24	L24	L17	W21	Y22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	73N	L18	J25	L25	L19	Y22	Y23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	74P	L20	J26	L26	L21	R20	W20
2	74N	L22	J27	L27	L23	P20	V20
2	75P	L24	J28	L28	L25	T21	W21
2	75N	L26	J29	L29	L27	R21	V21
2	76P	L28	J30	L30	L29	U21	Y24
2	76N	L30	J31	L31	L31	V21	Y25
2	77P	N0	P0	N0	N1	—	W22
2	77N	N2	P1	N1	N3	—	W23
2	78P	N4	P2	N2	N5	—	W24
-	-	VCC	-	-	-	VCC	VCC
2	78N	N6	P3	N3	N7	—	W25
-	-	GND	-	-	-	GND	GND
2	79P	N8	P4	N4	N9	—	W26

SELECT DEVICES DISCONTINUED

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	142N	Y26	Y29	AA29	Y27	B11	A10
0	142P	Y24	Y28	AA28	Y25	A11	A9
0	143N	Y22	Y27	AA27	Y23	F11	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	Y20	Y26	AA26	Y21	F10	A7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	Y18	Y25	AA25	Y19	E10	A6
0	144P	Y16	Y24	AA24	Y17	C10	A5
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	A4
0	145P	Y12	Y2	AA2	Y13	B10	A3
0	146N	Y10	Y23	AA23	Y11	A10	B10
0	146P	Y8	Y22	AA22	Y9	A9	B9
0	147N	Y6	Y21	AA21	Y7	C9	B8
0	147P	Y4	Y20	AA20	Y5	D9	B7
0	148N	Y2	Y19	AA19	Y3	F9	B6
0	148P	Y0	Y18	AA18	Y1	E9	B5
0	149N	Z30	Y1	AA1	Z31	A8	B4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	149P	Z28	Y0	AA0	Z29	B8	B3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	150N	Z26	AA29	-	Z27	A7	C10
0	150P	Z24	AA28	-	Z25	B7	C9
0	151N	Z22	AA27	-	Z23	A5	C8
0	151P	Z20	AA26	-	Z21	B5	C7
0	152N	Z18	AA25	-	Z19	B6	C6
0	152P	Z16	AA24	-	Z17	C7	C5
0	153N	Z14	AA23	-	Z15	E8	C4
0	153P	Z12	AA22	-	Z13	E7	D5
0	154N	Z10	AA21	-	Z11	E6	D9
-	-	VCC	-	-	-	VCC	VCC
0	154P	Z8	AA20	-	Z9	D6	D8
-	-	GND	-	-	-	GND	GND
0	155N	Z6	AA19	-	Z7	D8	D7
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	155P	Z4	AA18	-	Z5	F8	D6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	156N	Z2	AA17	-	Z3	F7	F9
0	156P	Z0	AA16	-	Z1	D7	E9
0	157N	AA30	AA15	-	AA31	C6	F7
0	157P	AA28	AA14	-	AA29	C5	F8
0	158N	AA26	AA13	-	AA27	C4	G8
0	158P	AA24	AA12	-	AA25	D5	G9

SELECT DEVICES DISCONTINUED

SELECT DEVICES DISCONTINUED

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5512MV	LC5512MV-45QN208C	512	3.3	4.5	Lead-free PQFP	208	149	C
	LC5512MV-75QN208C	512	3.3	7.5	Lead-free PQFP	208	149	C
	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	193	C
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	253	C
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	253	C
LC5768MV	LC5768MV-5FN256C	768	3.3	5.0	Lead-free fpBGA	256	193	C
	LC5768MV-75FN256C	768	3.3	7.5	Lead-free fpBGA	256	193	C
	LC5768MV-5FN484C	768	3.3	5.0	Lead-free fpBGA	484	317	C
	LC5768MV-75FN484C	768	3.3	7.5	Lead-free fpBGA	484	317	C
LC51024MV	LC51024MV-52FN484C	1024	3.3	5.2	Lead-free fpBGA	484	317	C
	LC51024MV-75FN484C	1024	3.3	7.5	Lead-free fpBGA	484	317	C
	LC51024MV-52FN672C	1024	3.3	5.2	Lead-free fpBGA	672	381	C
	LC51024MV-75FN672C	1024	3.3	7.5	Lead-free fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5FN256I	256	3.3	5.0	Lead-free fpBGA	256	141	I
	LC5256MV-75FN256I	256	3.3	7.5	Lead-free fpBGA	256	141	I
LC5512MV	LC5512MV-75QN208I	512	3.3	7.5	Lead-free PQFP	208	149	I
	LC5512MV-75FN256I	512	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5512MV-75FN484I	512	3.3	7.5	Lead-free fpBGA	484	253	I
LC5768MV	LC5768MV-75FN256I	768	3.3	7.5	Lead-free fpBGA	256	193	I
	LC5768MV-75FN484I	768	3.3	7.5	Lead-free fpBGA	484	317	I
LC51024MV	LC51024MV-75FN484I	1024	3.3	7.5	Lead-free fpBGA	484	317	I
	LC51024MV-75FN672I	1024	3.3	7.5	Lead-free fpBGA	672	381	I

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- TN1000 – sysIO Usage Guidelines for Lattice Devices
- TN1003 – sysCLOCK PLL Usage Guide for ispXPGA, ispGDX2, ispXPLD and ispMACH 5000VG Devices
- TN1031 – Power Estimation in ispXPLD 5000MX Devices
- TN1030 – Using Memory in ispXPLD 5000MX Devices
- TN1026 – ispXP Configuration Usage Guidelines

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
December 2003	07	Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers).
		Updated ispXPLD 5000MX timing numbers (version v.1.7).
		Added lead-free package designator.
		Removed ispXPLD 5000MC industrial temperature grade ordering part numbers.
January 2004	08	Lead-free package release for the ispXPLD 5000MC and 5000MV devices.
		Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers).
March 2004	08.1	Updated the MFB Cascade Chain table for the ispXPLD 5256MX device.
May 2004	09	Updated the ispXPLD 5000MX timig numbers (version v.1.8) ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release
		Updated typical supply current data and condition.
		ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14.
August 2004	10	Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ.
		Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free).
October 2004	10.1	Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer)
November 2004	11	Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers.
December 2004	11.1	Pin name RESETB has been updated to RESET.
March 2005	12	208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices.
April 2005	12.1	Page 23, clarification of footnote regarding IDK specification.
March 2006	12.2	Signal description for RESET has been updated.
April 2009	12.3	Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format.
February 2010	12.4	References to "system gates" changed to "functional gates."

SELECT DEVICES DISCONTINUED