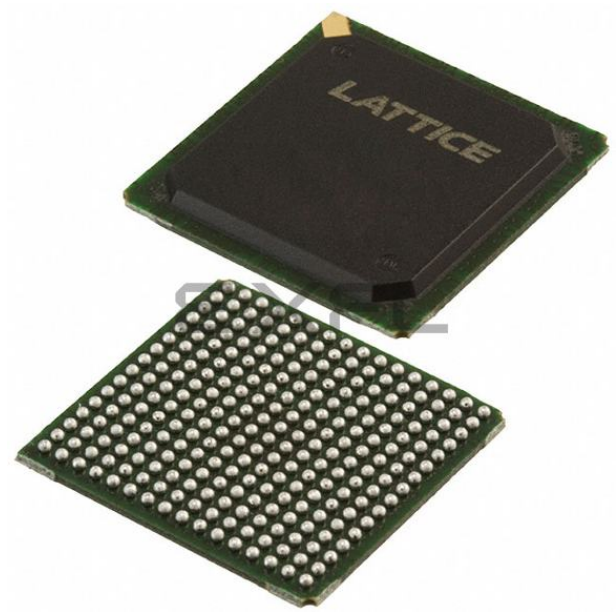
Lattice Semiconductor Corporation - LC5768MV-5FN256C Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	193
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768mv-5fn256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size[1]
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output
The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation
In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width
Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching
All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

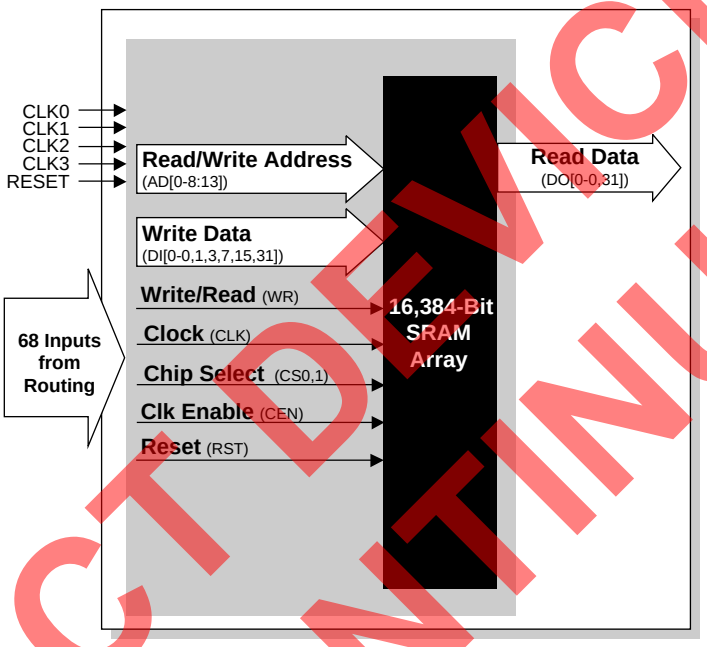


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

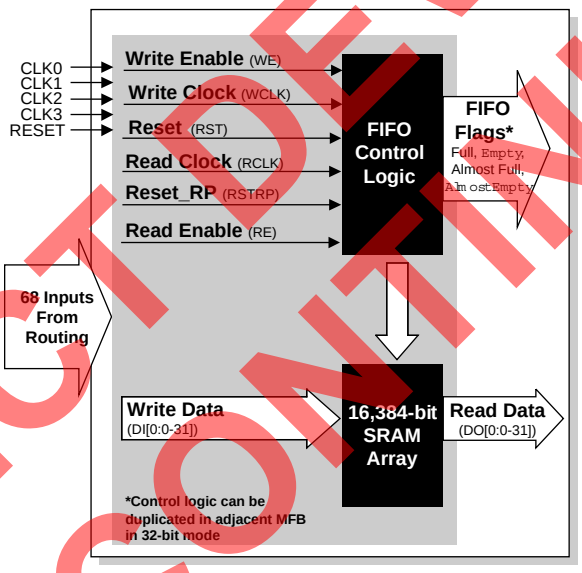


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

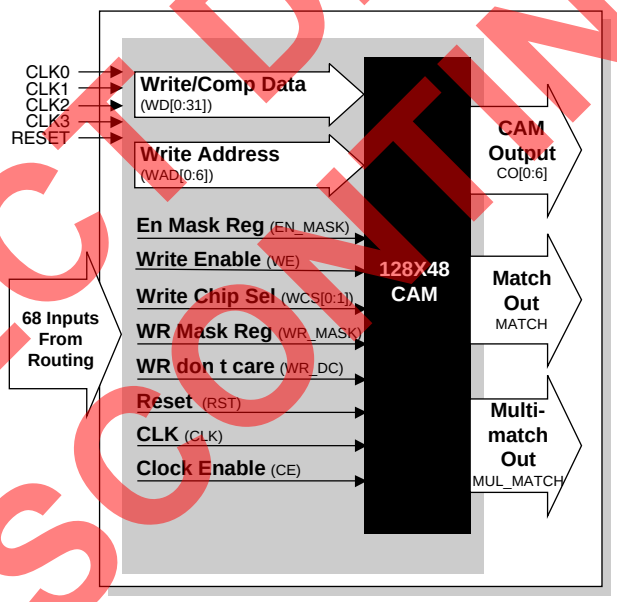


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

Figure 17. I/O Cell

Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 12 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}. For more information on the sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CCP} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CCP} = 1.8V, f = 10MHz	—	3	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—	mA
		V_{CCJ} = 2.5V	—	1	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} and V_{IH} = 0.65 * V_{CC}.
4. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8.

ispXPLD 5000MX Family External Switching Characteristics (Continued)[1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX} (RAM)[5]	Clock Frequency to RAM in:											
	Single Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Dual Port Mode	—	155	—	155	—	155	—	155	—	93	MHz
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—	106	MHz
f_{MAX} (FIFO)[5]	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—	132	MHz
t_{PWR_ON}	Power-on Time	—	200	—	200	—	200	—	200	—	200	µs

Timing v.1.8

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

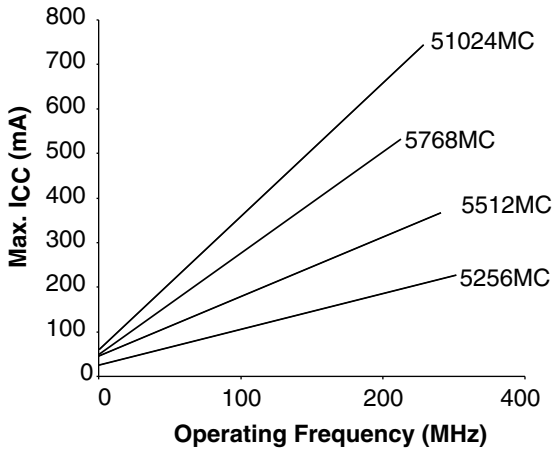
Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
t_{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{SPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21	—	ns
$t_{SPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—	9.86	ns
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—	4.29	ns
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56	—	ns
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19	—	ns
Pseudo Dual Port RAM													
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCES}$	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{PDPRCEH}$	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPWCES}$	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43	—	ns
$t_{PDPWCEH}$	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{PDPRADDS}$	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPRADDH}$	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPWADDS}$	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{PDPWADDH}$	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{PDPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IOI} Input Adjusters													
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t_{IOO} Output Adjusters – Output Signal Modifiers													
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t_{IOO} Output Adjusters – Output Configurations													
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

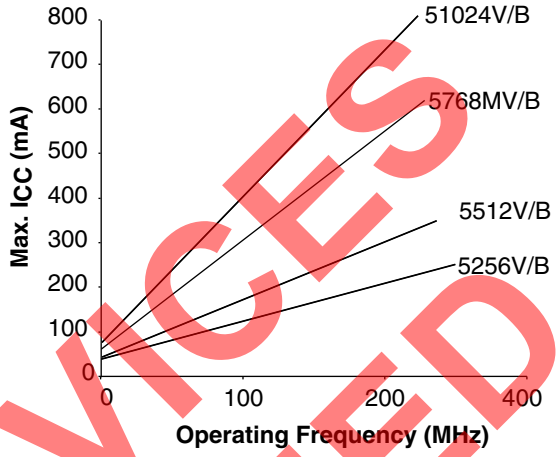
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Signals	208 PQFP[4]	256 fpBGA[3, 5]	484 fpBGA, 5[3]	672 fpBGA[3, 5]
VCC	10, 49, 76, 114, 153, 180	D4, D13, F6, F11, L6, L11, N4, N13	A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4	AA21, AA6, F21, F6, G20, G7, J13, J14, K13, K14, L13, L14, M13, M14, N10, N11, N12, N15, N16, N17, N18, N9, P10, P11, P12, P15, P16, P17, P18, P9, R13, R14, T13, T14, U13, U14, V13, V14, Y20, Y7
VCCO0	5, 17, 189, 204	A1, F7, G6	B9, C3, G8, G9, H7, J2, J7, P4	H10, H11, H8, H9, J8, J9, K8, L8, M8, N8
VCCO1	42, 57, 72	K6, L7, T1	AA9, R7, T3, T8, Y3	P8, R8, T8, U8, V8, V9, W10, W11, W8, W9
VCCO2	85, 100, 107, 121	K11, L10, T16	AA14, R16, T15, T20, Y20	P19, R19, T19, U19, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19
VCCO3	146, 161, 176	A16, F10, G11	B14, C20, G14, G15, H16, J16, J21, P19	H12, H13, H14, H15, H16, H17, H18, H19, J18, J19, K19, L19, M19, N19
VCCP	136	J16	M22	N25
VCCJ	27	J1	M1	N4
GND	15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174	K1, C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3	N1, A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8	A11, A16, A2, A25, AE1, AE2, AE25, AE26, AF11, AF16, AF2, AF25, B1, B2, B25, B26, J10, J11, J12, J15, J16, J17, K10, K11, K12, K15, K16, K17, K18, K9, L1, L10, L11, L12, L15, L16, L17, L18, L26, L9, M10, M11, M12, M15, M16, M17, M18, M9, N13, N14, P13, P14, R10, R11, R12, R15, R16, R17, R18, R9, T1, T10, T11, T12, T15, T16, T17, T18, T26, T9, U10, U11, U12, U15, U16, U17, U18, U9, V10, V11, V12, V15, V16, V17
GNDP	134	K16	N22	P26
NC[2]	—	**5256MX**: A2, A11, A12, A15, B2, B12, B15, B16, C4, C12, C15, C16, D1, D11, D14, D15, D16, E1, E4, E10, E11, E13, E14, F4, F5, F12, F13, L1, L4, M3, M7, M13, N2, N6, P1, P2, P5, P6, P13, P14, P15, P16, R1, R2, R4, R5, R6, R16, T2, T3, T4, T5, T6 **5512MX/5768MX**: L1	**5512MX**: P1, AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6 **5768MX/51024MX**: None	A12, A13, A14, A15, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA7, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AD11, AD12, AD13, AD14, AD15, AD16, AE11, AE12, AE13, AE14, AE15, AE16, AF12, AF13, AF14, AF15, B11, B12, B13, B14, B15, B16, C11, C12, C13, C14, C15, C16, C3, D10, D11, D12, D13, D14, D15, D16, D17, E10, E11, E12, E13, E14, E15, E16, E17, E6, E7, E8, F10, F11, F12, F13, F14, F15, F16, F17, G10, G11, G12, G13, G14, G15, G16, G17, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOX} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. Pin orientation follows the conventional counter-clockwise order from pin 1 marking of the topside view.
5. Internal GNDs and I/O GNDs (Bank 0 - Bank 3)þare connected inside package. V_{CCO} balls connect to four power planes within the package, one each for V_{CCOX}.

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7[1]	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	V19
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	—	—	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	—	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	See Power Supply and NC Connections Table		
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	U8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	15P	C26	D16	-	C27	T4	V6
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	15N	C24	D18	-	C25	T5	V7
-	-	GND	-	-	-	GND	GND
1	16P	C22	D20	-	C23	R4	Y5
-	-	VCC	-	-	-	VCC	VCC
1	16N	C20	D22	-	C21	N6	AA5
1	17P	C18	-	-	C19	R5	Y6
1	17N	C16	-	-	C17	P6	Y7
1	18P	C14	-	-	C15	—	AA6
1	18N	C12	-	-	C13	—	AA7
1	19P	C10	-	-	C11	—	W7
1	19N	C8	-	-	C9	M7	V8
1	20P	C6	-	-	C7	T6	W8
1	20N	C4	-	-	C5	R6	U9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	L8	U10
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	21P	C0	C16	A16	C1	T7	AB7
1	21N	D30	C17	A17	D31	R7	AA8
1	22P	D28	C18	A18	D29	N7	AB8
1	22N	D26	C19	A19	D27	P7	AB9
1	23P	D24	C20	A20	D25	T8	W9
1	23N	D22	C21	A21	D23	R8	Y9
1	24P	D20	C22	A22	D21	M8	AB10
1	24N	D18	C23	A23	D19	P8	AA10
1	-	D16/VREF1	-	-	D17	L9	W10
1	25P	D14	C24	A24	D15	N8	Y10
1	25N	D12	C25	A25	D13	M9	Y11
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	26P	D10	C26	A26	D11	N10	V9
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	26N	D8	C27	A27	D9	T9	V10
1	27P	D6	C28	A28	D7	T10	AA11
-	-	GND	-	-	-	GND	GND
1	27N	D4	C29	A29	D5	R9	AB11
-	-	VCC	-	-	-	VCC	VCC
1	28P	D2	C30	A30	D3	P9	U11
1	28N	D0	C31	A31	D1	N9	V11
2	29P	E0	F0	H0	E1	T11	AB12
-	-	VCC	-	-	-	VCC	VCC

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	29N	E2	F1	H1	E3	T12	AA12
-	-	GND	-	-	-	GND	GND
2	30P	E4	F2	H2	E5	P10	Y12
2	30N	E6	F3	H3	E7	R10	AA13
2	31P	E8	F4	H4	E9	R11	V12
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	31N	E10	F5	H5	E11	M10	U12
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	32P	E12	F6	H6	E13	M11	AB13
2	32N	E14	F7	H7	E15	T13	Y13
2	33P	E16	H0	-	E17	P11	V13
2	33N	E18/VREF2	H1	-	E19	T14	W13
2	34P	E20	F8	H8	E21	R12	V14
2	34N	E22	F9	H9	E23	R13	W14
2	35P	E24	F10	H10	E25	N11	Y14
2	35N	E26	F11	H11	E27	T15	AB14
2	36P	E28	F12	H12	E29	R14	AB15
2	36N	E30	F13	H13	E31	N12	AA15
2	37P	F0	F14	H14	F1	P12	U13
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	37N	F2	F15	H15	F3	R15	U14
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	38P	F4	H2	E0	F5	—	W15
2	38N	F6	H3	E2	F7	—	W16
2	39P	F8	H4	E4	F9	—	Y16
2	39N	F10	H5	E6	F11	—	AA16
2	40P	F12	H6	E8	F13	—	AB16
2	40N	F14	H7	E10	F15	—	AA17
2	41P	F16	H8	E12	F17	—	Y17
2	41N	F18	H9	E16	F19	—	AA18
2	42P	F20	H10	E20	F21	—	W17
-	-	VCC	-	-	-	VCC	VCC
2	42N	F22	H11	E22	F23	—	W18
-	-	GND	-	-	-	GND	GND
2	43P	F24	H12	-	F25	—	V15
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	43N	F26	H13	-	F27	—	U15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	44P	F28	H14	-	F29	P13	Y18
2	44N	F30	H15	-	F31	P15	V17
2	45P	G0	H16	-	G1	M13	V16
2	45N	G2	H17	-	G3	P14	U16
2	46P	G4	H18	-	G5	—	AB18

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	VCC
0	109P	Q28	Q30	S30	Q29	A7	C11
-	-	GND	-	-	-	GND	GND
0	110N	Q26	Q29	S29	Q27	D7	B11
0	110P	Q24	Q28	S28	Q25	C7	A11
0	111N	Q22	Q27	S27	Q23	B6	F11
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	111P	Q20	Q26	S26	Q21	E7	F10
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	112N	Q18	Q25	S25	Q19	E6	E10
0	112P	Q16	Q24	S24	Q17	A6	C10
0	113N	Q14/VREF0	Q3	S3	Q15	A5	D10
0	113P	Q12	Q2	S2	Q13	A4	B10
0	114N	Q10	Q23	S23	Q11	B5	A10
0	114P	Q8	Q22	S22	Q9	A3	A9
0	115N	Q6	Q21	S21	Q7	B4	C9
0	115P	Q4	Q20	S20	Q5	B3	D9
0	116N	Q2	Q19	S19	Q3	C5	F9
0	116P	Q0	Q18	S18	Q1	C6	E9
0	117N	R30	Q1	S1	R31	D5	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	117P	R28	Q0	S0	R29	D6	B8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	118N	R26	S29	-	R27	—	A7
0	118P	R24	S28	-	R25	—	B7
0	119N	R22	S27	-	R23	—	A5
0	119P	R20	S26	-	R21	—	B5
0	120N	R18	S25	-	R19	—	B6
0	120P	R16	S24	-	R17	—	C7
0	121N	R14	S23	-	R15	—	E8
0	121P	R12	S22	-	R13	—	E7
0	122N	R10	S21	-	R11	—	E6
-	-	VCC	-	-	-	VCC	VCC
0	122P	R8	S20	-	R9	—	D6
-	-	GND	-	-	-	GND	GND
0	123N	R6	S19	-	R7	—	D8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	123P	R4	S18	-	R5	—	F8
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	124N	R2	S17	-	R3	—	F7
0	124P	R0	S16	-	R1	—	D7
0	125N	S30	S15	-	S31	A2	C6
0	125P	S28	S14	-	S29	B2	C5

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193	I
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193	C
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193	C
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317	C
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193	I
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I