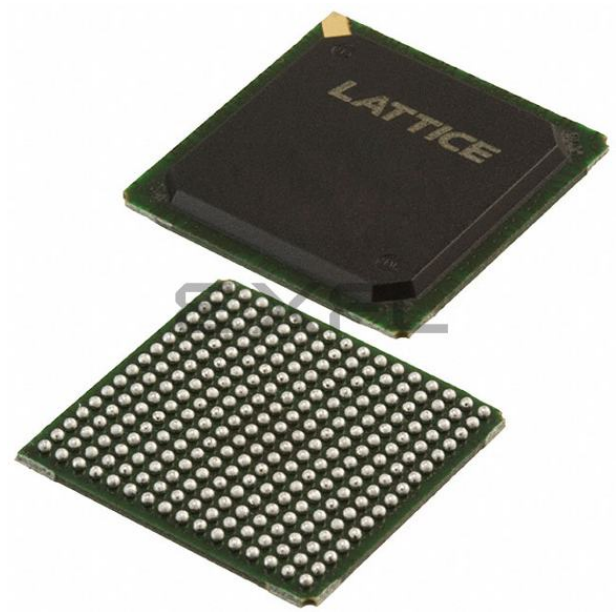
Lattice Semiconductor Corporation - LC5768MV-75F256C Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	193
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768mv-75f256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MV	LC5512MV-45Q208C	Active / Orderable	
	LC5512MV-45QN208C		
	LC5512MV-75Q208C		
	LC5512MV-75QN208C		
	LC5512MV-75Q208I		
	LC5512MV-75QN208I		
	LC5512MV-45F256C		
	LC5512MV-45FN256C		
	LC5512MV-75F256C		
	LC5512MV-75FN256C		
	LC5512MV-75F256I		
	LC5512MV-75FN256I		
	LC5512MV-45F484C		
	LC5512MV-45FN484C		
	LC5512MV-75F484C		
	LC5512MV-75FN484C		
	LC5512MV-75F484I		
	LC5512MV-75FN484I		
LC5512MB	LC5512MB-45Q208C	**Discontinued**	PCN#09-10
	LC5512MB-45QN208C		
	LC5512MB-75Q208C		
	LC5512MB-75QN208C		
	LC5512MB-75Q208I		
	LC5512MB-75QN208I		
	LC5512MB-45F256C	Active / Orderable	
	LC5512MB-45FN256C		
	LC5512MB-75F256C		
	LC5512MB-75FN256C		
	LC5512MB-75F256I		
	LC5512MB-75FN256I		
	LC5512MB-45F484C	**Discontinued**	PCN#09-10
	LC5512MB-45FN484C		
	LC5512MB-75F484C		
	LC5512MB-75FN484C		
	LC5512MB-75F484I		
	LC5512MB-75FN484I		
LC5512MC	LC5512MC-45Q208C	**Discontinued**	PCN#09-10
	LC5512MC-45QN208C		
	LC5512MC-75Q208C		
	LC5512MC-75QN208C		
	LC5512MC-75Q208I		
	LC5512MC-75QN208I		
	LC5512MC-45F256C		
	LC5512MC-45FN256C		
	LC5512MC-75F256C		
	LC5512MC-75FN256C		
	LC5512MC-75F256I		
	LC5512MC-75FN256I		

Product Line	Ordering Part Number	Product Status	Reference PCN
LC5512MC (Cont'd)	LC5512MC-45F484C	**Discontinued**	PCN#09-10
	LC5512MC-45FN484C		
	LC5512MC-75F484C		
	LC5512MC-75FN484C		
	LC5512MC-75F484I		
	LC5512MC-75FN484I		
LC5768MV	LC5768MV-5F256C	Active / Orderable	
	LC5768MV-5FN256C		
	LC5768MV-75F256C		
	LC5768MV-75FN256C		
	LC5768MV-75F256I		
	LC5768MV-75FN256I		
	LC5768MV-5F484C		
	LC5768MV-5FN484C		
	LC5768MV-75F484C		
	LC5768MV-75FN484C		
	LC5768MV-75F484I		
	LC5768MV-75FN484I		
LC5768MB	LC5768MB-5F256C	**Discontinued**	PCN#09-10
	LC5768MB-5FN256C		
	LC5768MB-75F256C		
	LC5768MB-75FN256C		
	LC5768MB-75F256I		
	LC5768MB-75FN256I		
	LC5768MB-5F484C		
	LC5768MB-5FN484C		
	LC5768MB-75F484C		
	LC5768MB-75FN484C		
	LC5768MB-75F484I		
	LC5768MB-75FN484I		
LC5768MC	LC5768MC-5F256C	**Discontinued**	PCN#09-10
	LC5768MC-5FN256C		
	LC5768MC-75F256C		
	LC5768MC-75FN256C		
	LC5768MC-75F256I		
	LC5768MC-75FN256I		
	LC5768MC-5F484C		
	LC5768MC-5FN484C		
	LC5768MC-75F484C		
	LC5768MC-75FN484C		
	LC5768MC-75F484I		
	LC5768MC-75FN484I		

Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width support.

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	H -> G -> F -> E
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

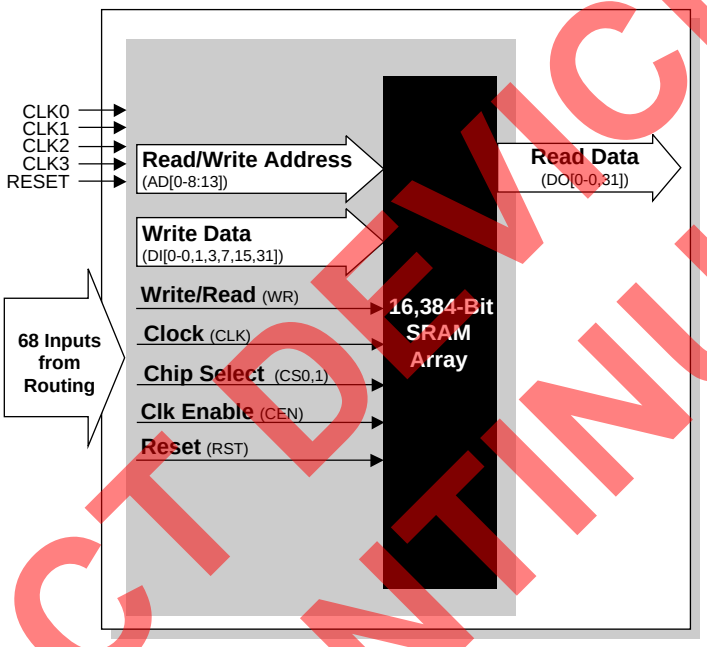


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

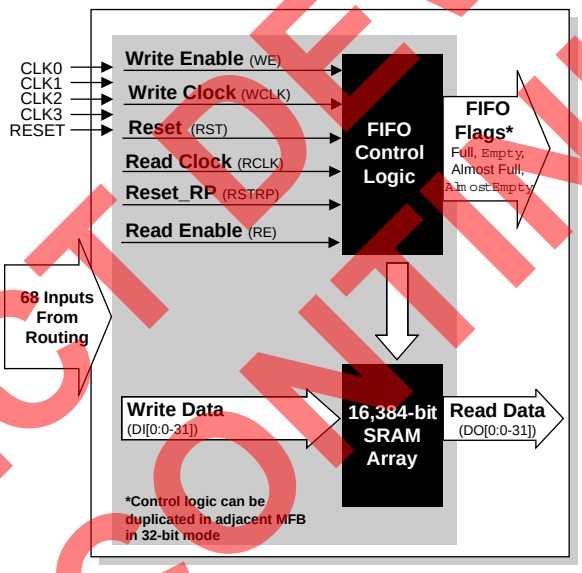


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

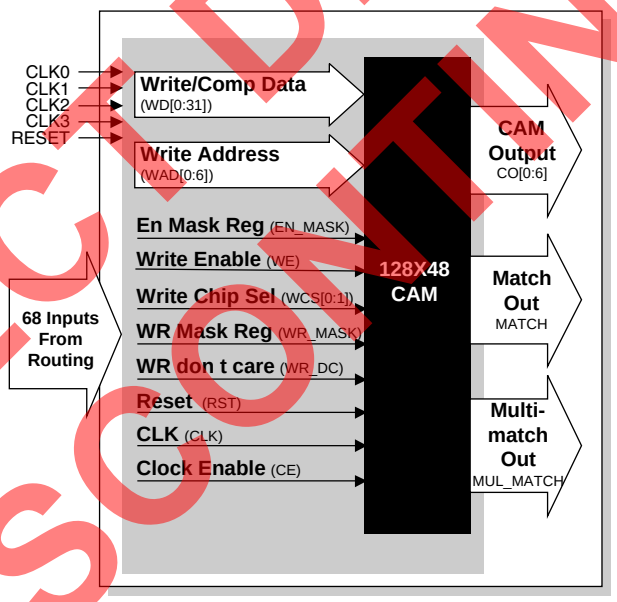


Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	0 ð V_{IN} ð (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) < V_{IN} ð 3.6V	—	—	40	µA
I_{IH}[4]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}[3]	I/O Active Pullup Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points	0 ð V_{IN} ð V_{IH} (MAX)	V_{CCO} * 0.35	—	V_{CCO} * 0.65	µA
C1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz
3. I_{PU} on JTAG pins has a maximum of -175µA for 5512MX devices.
4. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

sysIO Differential DC Electrical Characteristics

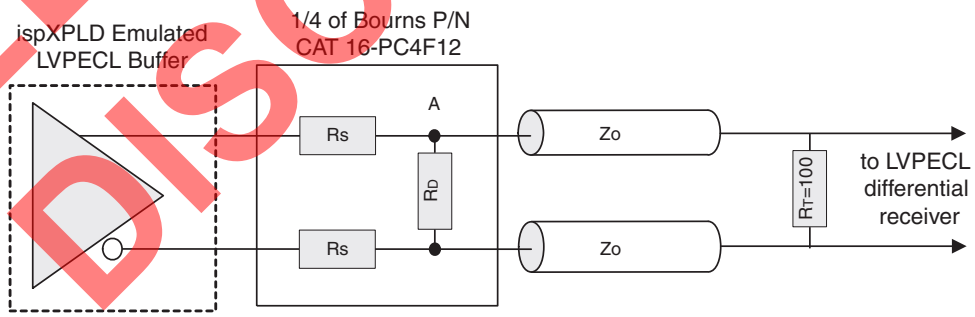
Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS					
V_{INP}	Input Voltage		0V	—	2.4V
V_{THD}	Differential Input Threshold	0.2 ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input Current	Power On	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50mV
V_{OS}	Output Voltage Offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125V	1.20V	1.375V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—	24mA

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input voltage	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 19). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V

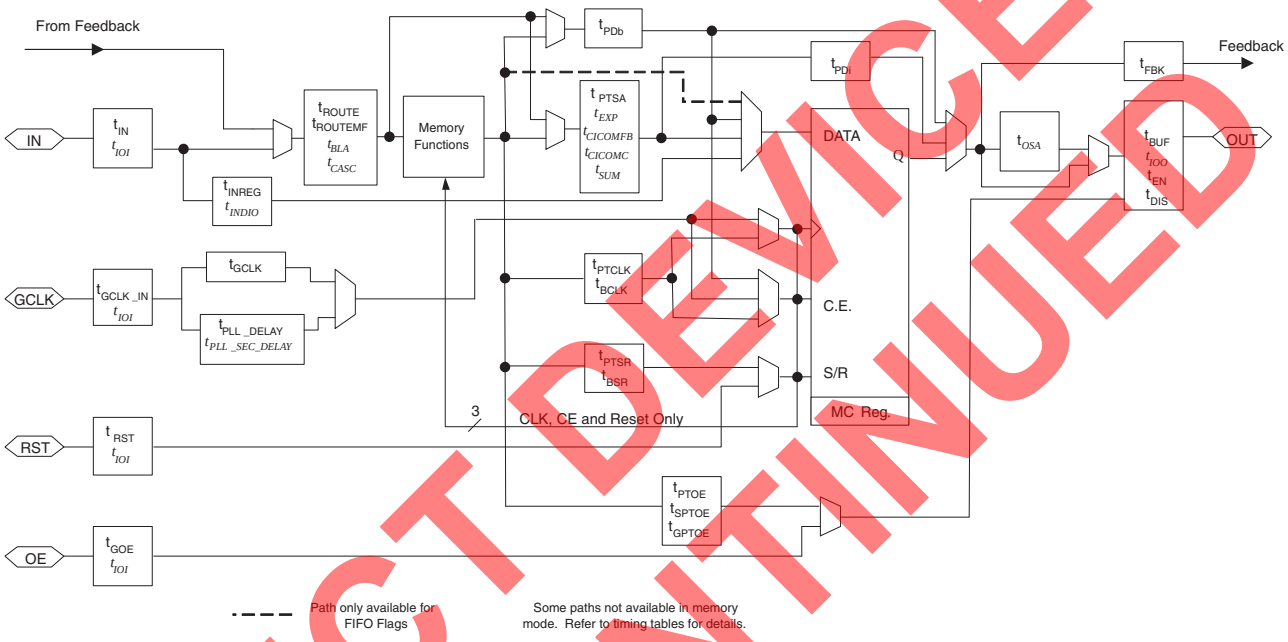
Figure 19. LVPECL Driver with Three Resistor Pack



Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03	—	ns
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14	—	ns
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—	4.29	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—	4.84	ns
CAM – Update Mode													
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44	—	ns
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31	—	ns
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	"Don't Care" Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMDCH}	"Don't Care" Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21	—	ns
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02	—	ns
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27	—	ns

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
2	20P	C14	-	-	C15	P11
2	20N	C16/VREF2	-	-	C17	T14
2	21P	C18	C8	D8	C19	R12
2	21N	C20	C9	D9	-	R13
2	22P	C21	C10	D10	-	N11
2	22N	C22	C11	D11	C23	T15
2	23P	C24	C12	D12	C25	R14
2	23N	C26	C13	D13	C27	N12
2	24P	C28	C14	D14	C29	P12
2	24N	C30	C15	D15	C31	R15
-	-	VCCO2	-	-	-	VCCO2
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	25P	D0	-	-	D1	N15
2	25N	D2	-	-	D3	N14
2	26P	D4	C16	D16	-	N16
2	26N	D5	C17	D17	-	M16
2	27P	D6	C18	D18	D7	M14
2	27N	D8	C19	D19	D9	M15
-	-	VCC	-	-	-	VCC
2	28P	D10	C20	D20	D11	L13
2	28N	D12	C21	D21	D13	L12
2	29P	D14	C22	D22	D15	L15
2	29N	D16	C23	D23	D17	L16
-	-	GND	-	-	-	GND
2	30P	D18	C24	D24	D19	L14
-	-	VCCO2	-	-	-	VCCO2
2	30N	D20	C25	D25	-	K15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	31P	D21	C26	D26	-	K14
2	31N	D22	C27	D27	D23	K12
2	32P	D24	C28	D28	D25	K13
2	32N	D26	C29	D29	D27	J13
2	33P	D28	C30	D30	D29	J14
2	33N	D30	C31	D31	D31	J12
-	-	TOE	-	-	-	J15
-	-	RESET	-	-	-	J11
-	-	GOE0	-	-	-	H11
-	-	GOE1	-	-	-	H13
-	-	GNDP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3N	GCLK2	-	-	-	H15
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table
-	GCLK3P	GCLK3	-	-	-	H16

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	V6
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	—	T5	V7
1	14P	B28	A20	—	B29	—	R4	Y5
1	14N	B30	A22	—	B31	—	N6	AA5
1	15P	C0	—	—	C1	—	R5	Y6
1	15N	C2	—	—	C3	—	P6	Y7
1	16P	C4	—	—	C5	—	—	AA6
1	16N	C8	—	—	C9	—	—	AA7
1	17P	C10	—	—	C11	—	—	W7
1	17N	C12	—	—	C13	—	M7[1]	V8
1	18P	C16	—	—	C17	—	T6	W8
1	18N	C18	—	—	C19	—	R6	U9
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	—	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	76P	L30/PLL_FBK1	L0	J0	L31	F15	E21
3	77N	M0/PLL_RST1	P27	N27	M1	H12	G22
3	77P	M2	P26	N26	M3	G14	F21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	78N	M4	P25	N25	M5	F16	H21
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	78P	M6	P24	N24	-	E16	G21
-	-	GND	-	-	-	GND	GND
3	79N	M8	P23	N23	M9	G13	D22
3	79P	M10	P22	N22	M11	G12	D21
3	80N	M12	P21	N21	M13	F14	J20
3	80P	M14/CLK_OUT1	P20	N20	M15	E15	J19
3	81N	M16	N31	-	M17	F12	E20
-	-	VCC	-	-	-	VCC	VCC
3	81P	M18	N30	M30	M19	F13	F20
3	82N	M20	N29	M28	M21	D16	H17
3	82P	M22	N28	M26	M23	D15	H18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	83N	M24	N27	-	M25	—	J18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	83P	M26	N26	-	M27	—	H19
3	84N	M28	N25	-	M29	—	G20
3	84P	M30	N24	-	M31	—	G19
-	-	GND	-	-	-	GND	GND
3	85N	N0	N23	-	N1	—	C22
-	-	VCC	-	-	-	VCC	VCC
3	85P	N2	N22	-	N3	—	C21
3	86N	N4	N21	-	-	—	D20
3	86P	N6	N20	-	-	—	C19
3	87N	N8	N19	-	N9	C16	F19
3	87P	N10	N18	-	N11	B16	E19
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	88N	N12	N17	-	N13	C15	G18
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	88P	N14	N16	-	N15	B15	F18
3	89N	N16	N15	-	N17	E14	B20
3	89P	N18	N14	-	N19	D14	B19
3	90N	N20	N13	-	N21	E13	A20
3	90P	N22	N12	-	N23	A15	A19
3	91N	N24	P19	N19	N25	D12	D18
3	91P	N26	P18	N18	N27	B14	C18
3	92N	N28	P17	N17	N29	C13	G17
3	92P	N30	P16	N16	N31	A14	F16

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	126N	S26	S13	-	S27	—	C4
0	126P	S24	S12	-	S25	—	D5

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	63P	K8	L20	-	K9	AA19	AA18
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	63N	K10	L21	-	K11	U17	Y18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	64P	K12	L22	-	K13	V18	AD25
2	64N	K14	L23	-	K15	AB21	AD26
2	65P	K16	L24	-	K17	U18	AC23
2	65N	K18	L25	-	K19	T17	AC24
2	66P	K20	L26	-	K21	AB20	AC25
2	66N	K22	L27	-	K23	AA20	AC26
2	67P	K24	L28	-	K25	Y19	AB22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	67N	K26	L29	-	K27	V19	AB23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	68P	K28	J16	L16	K29	T18	AB24
2	68N	K30	J17	L17	K31	R17	AB25
2	69P	L0	J18	L18	L1	U19	AB26
2	69N	L2	J19	L19	L3	T19	AA26
2	70P	L4	L30	I24	L5	V20	AA22
-	-	VCC	-	-	-	VCC	VCC
2	70N	L6	L31	I26	L7	U20	Y21
2	71P	L8	J20	L20	L9	W20	AA23
2	71N	L10	J21	L21	L11	Y21	AA24
2	72P	L12	J22	L22	L13	R18	AA25
2	72N	L14	J23	L23	L15	R19	Y26
-	-	GND	-	-	-	GND	GND
2	73P	L16	J24	L24	L17	W21	Y22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	73N	L18	J25	L25	L19	Y22	Y23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	74P	L20	J26	L26	L21	R20	W20
2	74N	L22	J27	L27	L23	P20	V20
2	75P	L24	J28	L28	L25	T21	W21
2	75N	L26	J29	L29	L27	R21	V21
2	76P	L28	J30	L30	L29	U21	Y24
2	76N	L30	J31	L31	L31	V21	Y25
2	77P	N0	P0	N0	N1	—	W22
2	77N	N2	P1	N1	N3	—	W23
2	78P	N4	P2	N2	N5	—	W24
-	-	VCC	-	-	-	VCC	VCC
2	78N	N6	P3	N3	N7	—	W25
-	-	GND	-	-	-	GND	GND
2	79P	N8	P4	N4	N9	—	W26

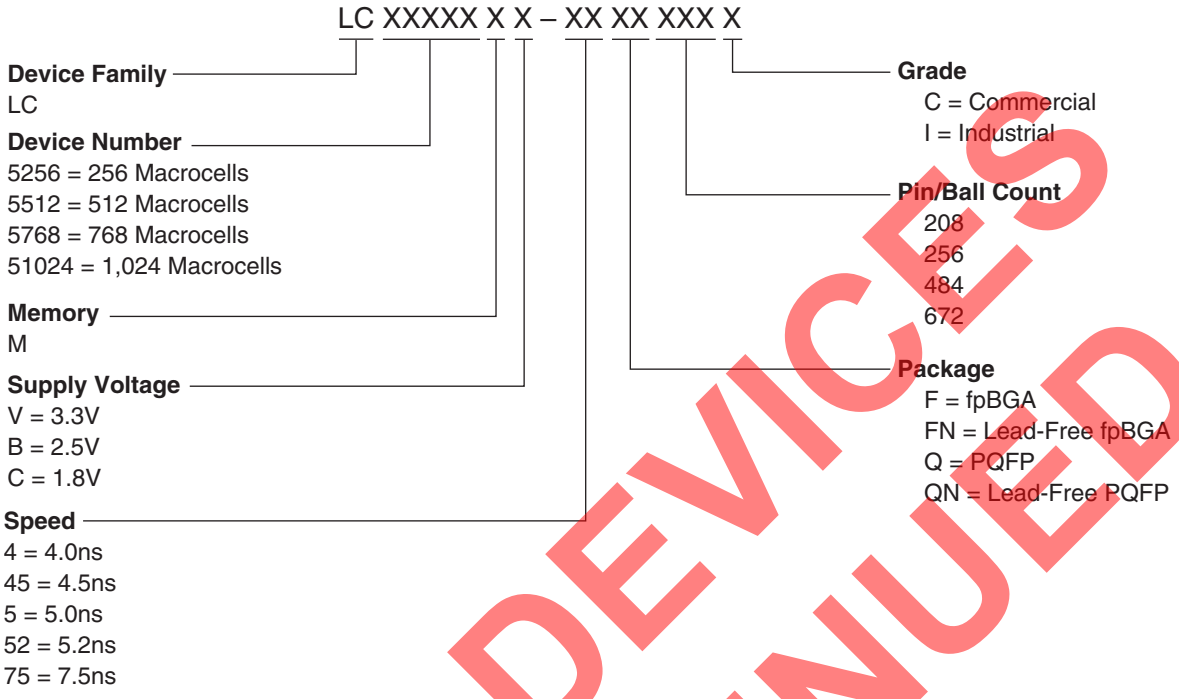
ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3P	GCLK3	-	-	-	N16	N24
3	93N	R0	T31	R31	R1	J22	N23
3	93P	R2	T30	R30	R3	H22	N22
3	94N	R4	T29	R29	R5	N19	M26
3	94P	R6	T28	R28	R7	P15	M25
3	95N	R8	T27	R27	R9	P21	M23
3	95P	R10	T26	R26	R11	N15	M22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	96N	R12	T25	R25	R13	M15	N20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	96P	R14	T24	R24	R15	N20	M20
-	-	GND	-	-	-	GND	GND
3	97N	R16	T23	R23	R17	P22	N21
3	97P	R18	T22	R22	R19	N21	M21
3	98N	R20	T21	R21	R21	N17	M24
3	98P	R22	T20	R20	R23	M20	L24
3	99N	R24	T19	R19	R25	P17	L23
-	-	VCC	-	-	-	VCC	VCC
3	99P	R26	T18	R18	R27	P18	L22
3	100N	R28	T17	R17	R29	M21	L25
3	100P	R30	T16	R16	R31	M17	K26
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	101N	T0	T15	R15	T1	L20	K25
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	101P	T2	T14	R14	T3	N18	K24
3	102N	T4	T13	R13	T5	L21	K23
3	102P	T6	T12	R12	T7	M18	K22
3	103N	T8	T11	R11	T9	L22	J25
3	103P	T10	T10	R10	T11	L17	J24
3	104N	T12	T9	R9	T13	K22	L21
3	104P	T14	T8	R8	T15	L18	K21
3	105N	T16	T7	R7	T17	K21	L20
3	105P	T18	T6	R6	T19	K18	K20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	T20	T5	R5	T21	K20	J23
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	T22	T4	R4	T23	K17	J22
3	107N	T24	T3	R3	T25	K19	J26
3	107P	T26	T2	R2	T27	J17	H26
3	108N	T28	T1	R1	T29	E22	H25
3	108P	T30/PLL_FBK1	T0	R0	T31	E21	H24
3	109N	U0/PLL_RST1	X27	V27	U1	G22	H23
3	109P	U2	X26	V26	U3	F21	H22

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	142N	Y26	Y29	AA29	Y27	B11	A10
0	142P	Y24	Y28	AA28	Y25	A11	A9
0	143N	Y22	Y27	AA27	Y23	F11	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	Y20	Y26	AA26	Y21	F10	A7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	Y18	Y25	AA25	Y19	E10	A6
0	144P	Y16	Y24	AA24	Y17	C10	A5
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	A4
0	145P	Y12	Y2	AA2	Y13	B10	A3
0	146N	Y10	Y23	AA23	Y11	A10	B10
0	146P	Y8	Y22	AA22	Y9	A9	B9
0	147N	Y6	Y21	AA21	Y7	C9	B8
0	147P	Y4	Y20	AA20	Y5	D9	B7
0	148N	Y2	Y19	AA19	Y3	F9	B6
0	148P	Y0	Y18	AA18	Y1	E9	B5
0	149N	Z30	Y1	AA1	Z31	A8	B4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	149P	Z28	Y0	AA0	Z29	B8	B3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	150N	Z26	AA29	-	Z27	A7	C10
0	150P	Z24	AA28	-	Z25	B7	C9
0	151N	Z22	AA27	-	Z23	A5	C8
0	151P	Z20	AA26	-	Z21	B5	C7
0	152N	Z18	AA25	-	Z19	B6	C6
0	152P	Z16	AA24	-	Z17	C7	C5
0	153N	Z14	AA23	-	Z15	E8	C4
0	153P	Z12	AA22	-	Z13	E7	D5
0	154N	Z10	AA21	-	Z11	E6	D9
-	-	VCC	-	-	-	VCC	VCC
0	154P	Z8	AA20	-	Z9	D6	D8
-	-	GND	-	-	-	GND	GND
0	155N	Z6	AA19	-	Z7	D8	D7
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	155P	Z4	AA18	-	Z5	F8	D6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	156N	Z2	AA17	-	Z3	F7	F9
0	156P	Z0	AA16	-	Z1	D7	E9
0	157N	AA30	AA15	-	AA31	C6	F7
0	157P	AA28	AA14	-	AA29	C5	F8
0	158N	AA26	AA13	-	AA27	C4	G8
0	158P	AA24	AA12	-	AA25	D5	G9

Part Number Description



Ordering Information

Note: For voltage families offered in industrial temperature grades and for all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -45XXXXC is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only. In addition, the fastest commercial speed grade (-5) for the LC5768MB/MV devices, at Lattice's discretion, will utilize either a commercial grade only single-mark or a dual-mark format in conjunction with the slower industrial speed grade (-75).

Conventional Packaging

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	141	C
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	141	C
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	141	C
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	149	C
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	149	C
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	193	C
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	193	C
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	253	C
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	253	C