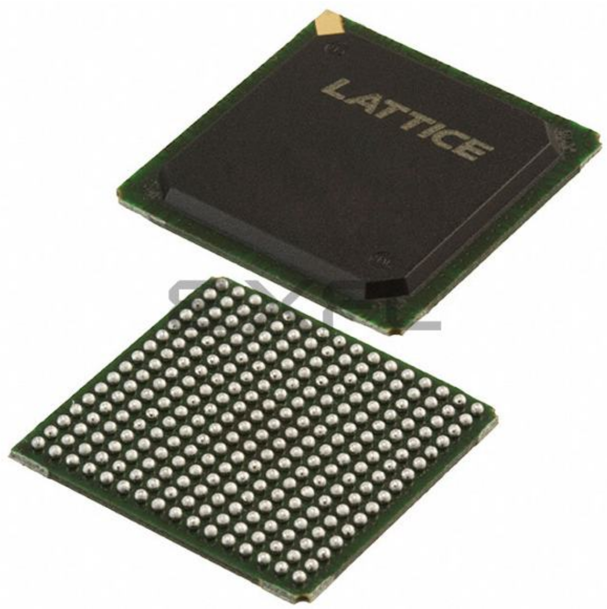


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	193
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768mv-75f256i

ispXPLD™ 5000MX Family

3.3V, 2.5V and 1.8V In-System Programmable
eXpanded Programmable Logic Device XPLD™ Family

February 2010 — Data Sheet

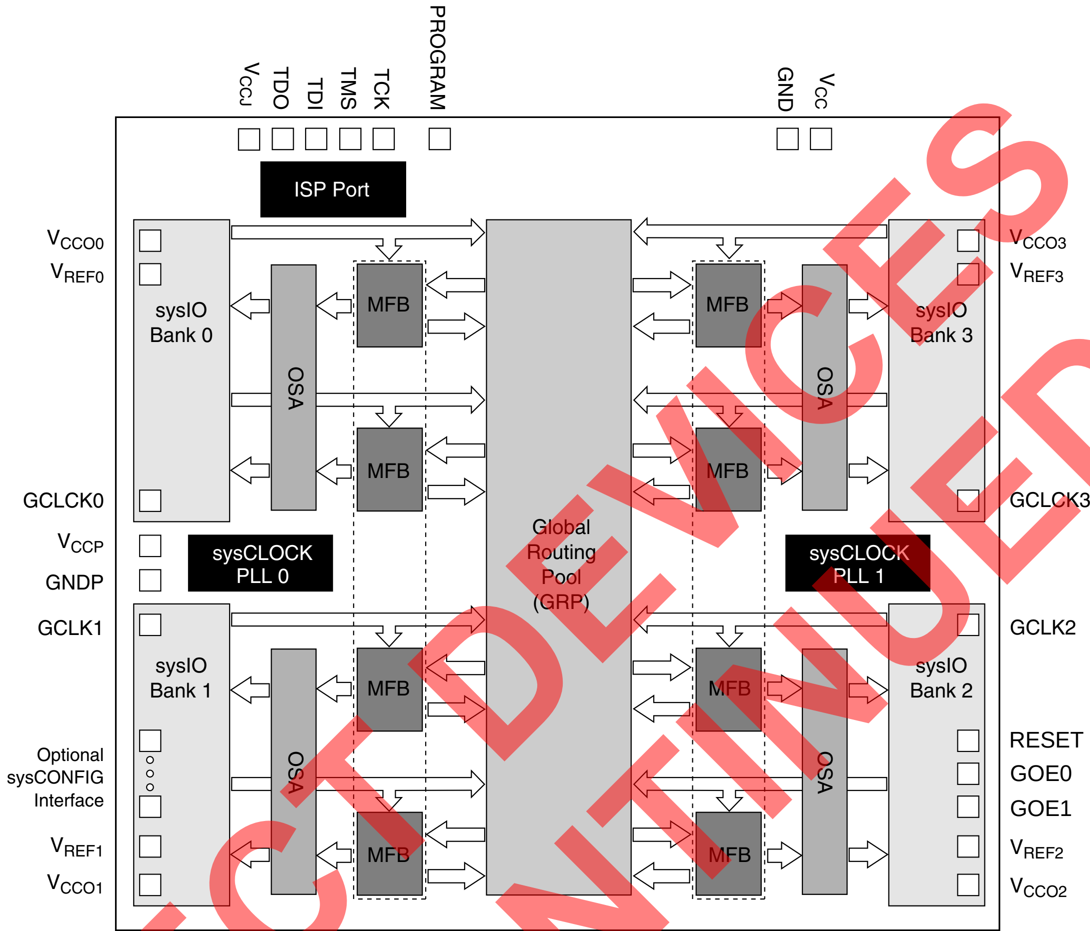
Features

- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
  - LVTTL
- **Expanded In-System Programmability (ispXP™)**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
  - Design security
- **High Speed Operation**
  - 4.0ns pin-to-pin delays, 300MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Typical static power: 20 to 50mA (1.8V), 30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - IEEE 1149.1 interface for boundary scan testing
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging
  - Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	3.7ns
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	250MHz
Functional Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Figure 1. ispXPLD 5000MX Block Diagram



Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

Output Sharing Array (OSA)

A number of I/O pads are available in each sysIO bank to route the selected number of macrocells from the MFB outputs directly to the I/O pads in logic mode. In the ispXPLD 5000MX, the large number of inputs and PTs to the MFB as well as the presence of the PTSA can cover most routing flexibility of signals to I/O cells. The Output Sharing Array gives additional routing capability and I/O access to an MFB when a wide output function takes up the whole MFB and cannot be easily divided across multiple MFBs. By using the OSA, the wide output function, such as 32-bit FIFO, can have all of its output signals from the one MFB routed to I/O cells. In a given I/O block, the wide output functions must share the I/O pads with other logic functions.

The OSA bypass option routes the MFB signal directly to the I/O cell, allowing a direct connection to the I/O cell. The logic functions use the option to provide faster speed to the outputs. The Logic Signal Connection tables list the OSA bypass as the primary macrocell and OSA options as alternate macrocells. Similarly, the Alternate Input listing in the table shows the alternate macrocell input connection for a given I/O pin. Figure 17 shows the alternate macrocell connections in an I/O cell.

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedback line to its associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The MFBs are grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PTOE signal is derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

Figure 17. I/O Cell

Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 12 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}. For more information on the sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to TN1000 – sysIO Usage Guidelines for Lattice Devices.

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. The JTAG TAP pins support only LVCMOS 3.3, 2.5 and 1.8V standards. The voltage is controlled by V_{CCJ}. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

Programmable Slew Rate

The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices support two slew rates. This allows system noise and performance to be balanced in a design.

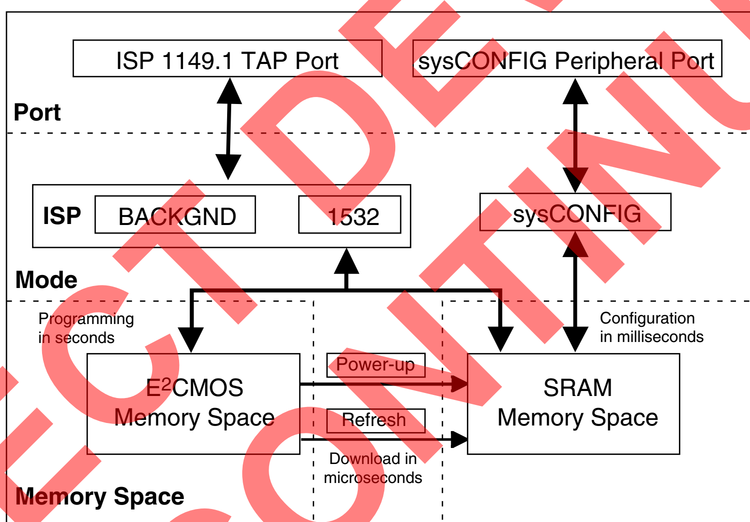
Programmable Bus-Maintenance

All general-purpose inputs have programmable bus maintenance circuitry. These are intended to maintain a valid logic level into a device when driving devices go into the tri-state mode. Four options are available for users: pull-up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides "instant-on" at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device. Figure 18 shows the different ports and modes that are used in the configuration and programming of the ispXPLD 5000MX devices.

Figure 18. ispXP Block Diagram



IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfiguration of the SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during the testing of a circuit board.

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are $V_{IL} = 0.35 * V_{CC}$ and $V_{IH} = 0.65 * V_{CC}$.
4. For 1.8V devices (ispXPLD 5000MC) these specifications are $V_{IL} = 0.3 * V_{CC} * 3.3/1.8$, $V_{IH} = 0.5 * V_{CC} * 3.3/1.8$.

ispXPLD 5000MX Family Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays													
t_{IN}	Input Buffer Delay	—	—	0.70	—	0.91	—	0.96	—	1.11	—	1.30	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.40	—	0.35	—	0.35	—	0.35	—	0.55	ns
t_{RST}	Global RESET Pin Delay	—	—	3.77	—	4.24	—	4.71	—	4.71	—	7.07	ns
t_{GOE}	Global OE Pin Delay	—	—	1.98	—	2.66	—	2.34	—	2.87	—	3.27	ns
t_{BUF}	Delay through Output Buffer	—	—	1.16	—	1.30	—	1.45	—	1.60	—	2.17	ns
t_{EN}	Output Enable Time	—	—	2.52	—	2.84	—	3.16	—	3.63	—	4.23	ns
t_{DIS}	Output Disable Time	—	—	1.92	—	2.40	—	2.40	—	2.40	—	3.60	ns
Routing Delays													
t_{ROUTE}	Delay through SRP	—	—	1.95	—	2.06	—	2.34	—	2.24	—	3.66	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.60	—	0.60	—	0.60	—	0.47	—	1.63	ns
t_{PTSA}	Product Term Sharing Array Delay	—	—	0.50	—	0.50	—	0.53	—	0.83	—	1.34	ns
t_{FBK}	Internal Feedback Delay	—	—	0.19	—	0.02	—	0.39	—	0.03	—	0.60	ns
t_{GCLK}	Global Clock Tree Delay	—	—	0.52	—	0.32	—	0.72	—	0.82	—	0.78	ns
t_{BCLK}	Block PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—	0.23	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.30	—	0.30	—	0.30	—	0.30	ns
t_{BSR}	Block PT Reset Delay	—	—	0.72	—	0.81	—	0.90	—	0.94	—	1.35	ns
t_{PTSR}	Macrocell PT Set/ Reset Delay	—	—	0.60	—	0.75	—	0.75	—	0.75	—	1.13	ns
t_{LPTOE}	Macrocell PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t_{SPTOE}	Segment PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—	1.31	ns
t_{OSA}	Output Sharing Array Delay	—	—	0.80	—	0.90	—	1.00	—	1.00	—	1.50	ns
t_{PTOE}	Global PT OE Delay	—	—	0.83	—	1.04	—	1.04	—	1.04	—	1.56	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	—	0.20	—	0.23	—	0.25	—	0.25	—	0.38	ns
t_{PDI}	Macrocell Propagation Delay	—	—	0.50	—	0.93	—	0.72	—	0.72	—	1.04	ns

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IOI} Input Adjusters													
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
t_{IOO} Output Adjusters – Output Signal Modifiers													
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	ns
t_{IOO} Output Adjusters – Output Configurations													
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns

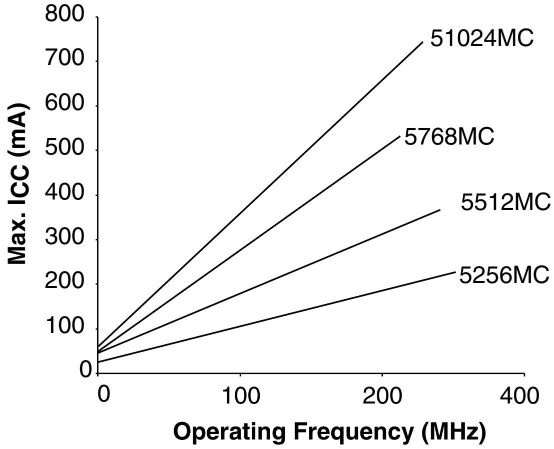
ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_out	Using HSTL 2.5V, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—	0.6	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—	0.3	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	ns

Timing v.1.8

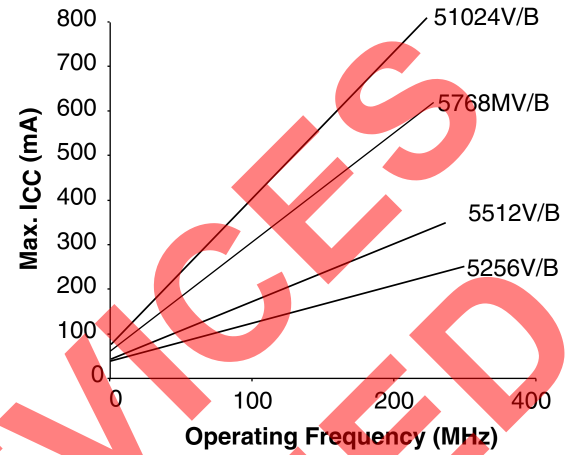
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	36
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to TN1031 – Power Estimation in ispXPLD 5000MX Devices.

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	B4
0	109P	O28	O10	P16	O29	1	E4	A4
0	110N	O26	M17	O17	O27	2	B1	B3
0	110P	O24	M16	O16	O25	3	C1	A3
0	111N	O22	M15	O15	O23	4	D3	F5
—	—	V_{CCO0}	—	—	—	5	V_{CCO0}	V_{CCO0}
0	111P	O20	M14	O14	O21	6	C2	G6
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	GND (Bank 0)
0	112N	O18	M13	O13	O19	8	E3	H6
0	112P	O16	M12	O12	O17	9	D2	G5
0	113N	O14	O9	P14	O15	—	—	D3
0	113P	O12	O8	P12	O13	—	—	D2
0	114N	O10	O7	P10	O11	—	—	E4
0	114P	O8	O6	P8	O9	—	—	E3
0	115N	O6	O5	P6	O7	—	—	F4
0	115P	O4	O4	P4	O5	—	—	G4
0	116N	O2	O3	P2	O3	—	—	C2
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	V_{CCO0}
0	116P	O0	O2	P0	O1	—	—	C1
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	GND (Bank 0)
0	117N	P30	O1	—	P31	—	D1	F3
0	117P	P28	O0	—	P29	—	E1	G3
0	118N	P26	O31	—	P27	—	F4	H4
—	—	V_{CC}	—	—	—	10	V_{CC}	V_{CC}
0	118P	P24	O30	—	P25	—	F5	J4
0	119N	P22	M11	O11	P23	11	E2	H5
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	J5
0	120N	P18	M9	O9	P19	13	F1	E2
0	120P	P16	M8	O8	P17	14	G1	F2
—	—	GND	—	—	—	15	GND	GND
0	121N	P14	M7	O7	P15	16	F3	D1
—	—	V_{CCO0}	—	—	—	17	V_{CCO0}	V_{CCO0}
0	121P	P12	M6	O6	P13	18	G5	E1
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	GND (Bank 0)
0	122N	P10	M5	O5	P11	20	H5	J3
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	H2
0	123N	P6	—	—	P7	22	G3	G2
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	G1
0	124N	P2	—	—	P3	24	G2	H1
0	124P	P0	—	—	P1	25	H1	J1
—	GCLK0P	GCLK0	—	—	—	26	H2	N7
—	—	V_{CCJ}	—	—	—	See Power Supply and NC Connections Table		

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	484 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	P16
-	-	VCCP	-	-	-	See Power Supply and NC Connections Table	
-	GCLK3P	GCLK3	-	-	-	H16	N16
3	61N	J0	L31	J31	-	H14	J22
3	61P	J2	L30	J30	J3	G16	H22
3	62N	J4	L29	J29	J5	—	N19
3	62P	J6	L28	J28	J7	—	P15
3	63N	J8	L27	J27	J9	—	P21
3	63P	J10	L26	J26	J11	—	N15
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	64N	J12	L25	J25	J13	—	M15
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	64P	J14	L24	J24	J15	—	N20
-	-	GND	-	-	-	GND	GND
3	65N	J16	L23	J23	J17	—	P22
3	65P	J18	L22	J22	J19	—	N21
3	66N	J20	L21	J21	J21	—	N17
3	66P	J22	L20	J20	J23	—	M20
3	67N	J24	L19	J19	J25	—	P17
-	-	VCC	-	-	-	VCC	VCC
3	67P	J26	L18	J18	J27	—	P18
3	68N	J28	L17	J17	J29	—	M21
3	68P	J30	L16	J16	J31	—	M17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	69N	L0	L15	J15	-	—	L20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	69P	L2	L14	J14	L3	—	N18
3	70N	L4	L13	J13	L5	—	L21
3	70P	L6	L12	J12	L7	—	M18
3	71N	L8	L11	J11	L9	—	L22
3	71P	L10	L10	J10	L11	—	L17
3	72N	L12	L9	J9	L13	—	K22
3	72P	L14	L8	J8	L15	—	L18
3	73N	L16	L7	J7	L17	—	K21
3	73P	L18	L6	J6	L19	—	K18
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	74N	L20	L5	J5	L21	—	K20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	74P	L22	L4	J4	L23	—	K17
3	75N	L24	L3	J3	L25	—	K19
3	75P	L26	L2	J2	L27	—	J17
3	76N	L28	L1	J1	L29	G15	E22

ispXPLD 51024MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	159N	AA22	AA11	AB18	AA23	B4	C2
0	159P	AA20	AA10	AB16	AA21	A4	C1
0	160N	AA18	Y17	AA17	AA19	B3	D4
0	160P	AA16	Y16	AA16	AA17	A3	D3
0	161N	AA14	Y15	AA15	AA15	F5	D2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	161P	AA12	Y14	AA14	AA13	G6	D1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	162N	AA10	Y13	AA13	AA11	H6	E5
0	162P	AA8	Y12	AA12	AA9	G5	E4
0	163N	AA6	AA9	AB14	AA7	D3	E3
0	163P	AA4	AA8	AB12	AA5	D2	E2
0	164N	AA2	AA7	AB10	AA3	E4	E1
-	-	VCC	-	-	-	VCC	VCC
0	164P	AA0	AA6	AB8	AA1	E3	F2
-	-	GND	-	-	-	GND	GND
0	165N	AB30	AA5	AB6	AB31	F4	F5
0	165P	AB28	AA4	AB4	AB29	G4	G6
0	166N	AB26	AA3	AB2	AB27	C2	F4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	166P	AB24	AA2	AB0	AB25	C1	F3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	167N	AB22	AA1	-	AB23	F3	F1
0	167P	AB20	AA0	-	AB21	G3	G1
0	168N	AB18	AA31	-	AB19	H4	G5
-	-	VCC	-	-		VCC	VCC
0	168P	AB16	AA30	-	AB17	J4	G4
0	169N	AB14	Y11	AA11	AB15	H5	H7
0	169P	AB12/CLK_OUT0	Y10	AA10	AB13	J5	J7
0	170N	AB10	Y9	AA9	AB11	E2	G3
0	170P	AB8	Y8	AA8	AB9	F2	G2
-	-	GND	-	-	-	GND	GND
0	171N	AB6	Y7	AA7	AB7	D1	H6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	171P	AB4	Y6	AA6	AB5	E1	J6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	172N	AB2	Y5	AA5	AB3	J3	H5
0	172P	AB0/PLL_RST0	Y4	AA4	AB1	H2	H4
0	173N	AC30	AC31	AE31	AC31	G2	H3
0	173P	AC28/PLL_FBK0	AC30	AE30	AC29	G1	H2
0	174N	AC26	AC29	AE29	AC27	J6	H1
0	174P	AC24	AC28	AE28	AC25	K4	J1

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	See Power Supply and NC Connections Table	
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	142N	Y26	Y29	AA29	Y27	B11	A10
0	142P	Y24	Y28	AA28	Y25	A11	A9
0	143N	Y22	Y27	AA27	Y23	F11	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	Y20	Y26	AA26	Y21	F10	A7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	Y18	Y25	AA25	Y19	E10	A6
0	144P	Y16	Y24	AA24	Y17	C10	A5
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	A4
0	145P	Y12	Y2	AA2	Y13	B10	A3
0	146N	Y10	Y23	AA23	Y11	A10	B10
0	146P	Y8	Y22	AA22	Y9	A9	B9
0	147N	Y6	Y21	AA21	Y7	C9	B8
0	147P	Y4	Y20	AA20	Y5	D9	B7
0	148N	Y2	Y19	AA19	Y3	F9	B6
0	148P	Y0	Y18	AA18	Y1	E9	B5
0	149N	Z30	Y1	AA1	Z31	A8	B4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	149P	Z28	Y0	AA0	Z29	B8	B3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	150N	Z26	AA29	-	Z27	A7	C10
0	150P	Z24	AA28	-	Z25	B7	C9
0	151N	Z22	AA27	-	Z23	A5	C8
0	151P	Z20	AA26	-	Z21	B5	C7
0	152N	Z18	AA25	-	Z19	B6	C6
0	152P	Z16	AA24	-	Z17	C7	C5
0	153N	Z14	AA23	-	Z15	E8	C4
0	153P	Z12	AA22	-	Z13	E7	D5
0	154N	Z10	AA21	-	Z11	E6	D9
-	-	VCC	-	-	-	VCC	VCC
0	154P	Z8	AA20	-	Z9	D6	D8
-	-	GND	-	-	-	GND	GND
0	155N	Z6	AA19	-	Z7	D8	D7
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	155P	Z4	AA18	-	Z5	F8	D6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	156N	Z2	AA17	-	Z3	F7	F9
0	156P	Z0	AA16	-	Z1	D7	E9
0	157N	AA30	AA15	-	AA31	C6	F7
0	157P	AA28	AA14	-	AA29	C5	F8
0	158N	AA26	AA13	-	AA27	C4	G8
0	158P	AA24	AA12	-	AA25	D5	G9

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193	I
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193	C
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193	C
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317	C
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193	I
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
December 2003	07	Added ispXPLD 5768MX information (supply current, timings, power consumption, power estimation coefficients, memory coefficients, logic signal connections, ordering part numbers).
		Updated ispXPLD 5000MX timing numbers (version v.1.7).
		Added lead-free package designator.
		Removed ispXPLD 5000MC industrial temperature grade ordering part numbers.
January 2004	08	Lead-free package release for the ispXPLD 5000MC and 5000MV devices.
		Timing model parameter tCOi correction - Maximum specification instead of Minimum (no changes in the timing numbers).
March 2004	08.1	Updated the MFB Cascade Chain table for the ispXPLD 5256MX device.
May 2004	09	Updated the ispXPLD 5000MX timig numbers (version v.1.8) ispXPLD 5256MC, 5512MC and 51024MC industrial temperature grade devices release
		Updated typical supply current data and condition.
		ispXPLD 5256MX 256-fpBGA logic signal connection tables: Removed internal signal description for ball H5 and G14.
August 2004	10	Added footnote "1, page 49. These inputs should not toggle during power up for proper power-up configuration." to CCLK and READ.
		Added ispXPLD 5768MC Industrial grade OPNs (Conventional and Lead-Free).
October 2004	10.1	Figure 19, LVPECL Driver with Three Resistor Pack has been updated (ispXPLD LVPECL Buffer changed to ispXPLD Emulated LVPECL Buffer)
November 2004	11	Added ispXPLD 5000MB (2.5V) Lead-Free Ordering Part Numbers.
December 2004	11.1	Pin name RESETB has been updated to RESET.
March 2005	12	208-PQFP Lead-free package release for the ispXPLD 5512MV/B/C devices.
April 2005	12.1	Page 23, clarification of footnote regarding IDK specification.
March 2006	12.2	Signal description for RESET has been updated.
April 2009	12.3	Ordering Information section has been updated to describe alternate LC5768MB/MV top side marking format.
February 2010	12.4	References to "system gates" changed to "functional gates."