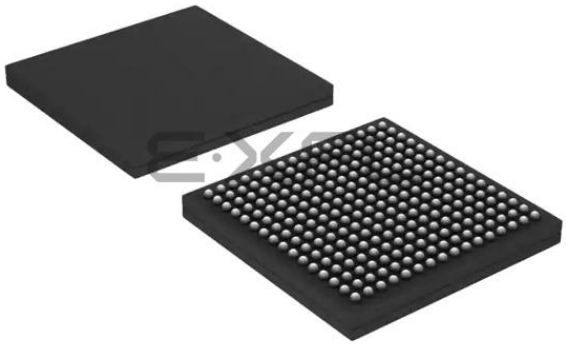

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Peripherals	DMA, PWM, WDT
Number of I/O	87
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf54418cmj250r

Figure 5 shows an example for bypassing the FlexBus power supply for the MPU. This bypass should be applied to as many FB_VDD signals as routing allows. Each one should be placed as close to the ball as possible.

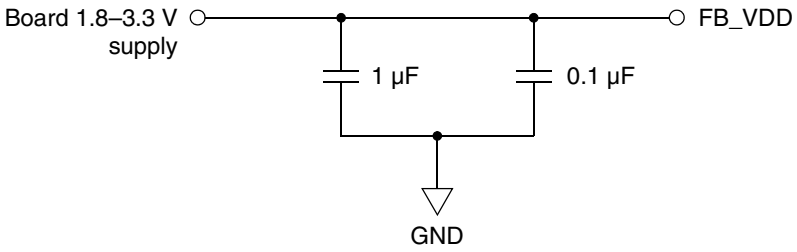
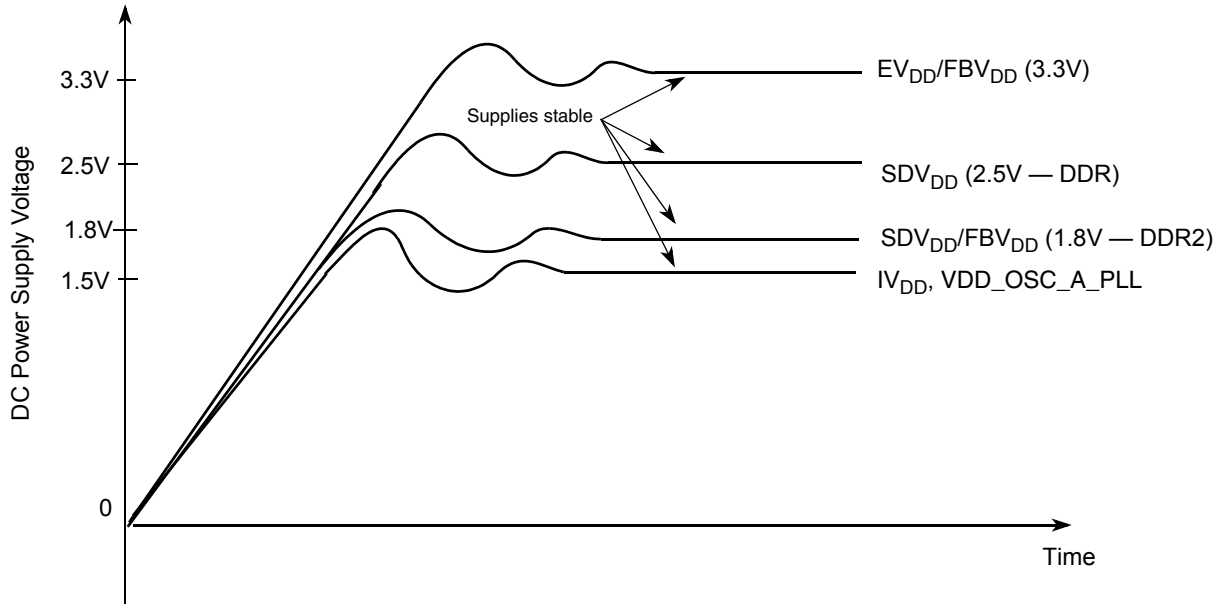


Figure 5. FB_VDD power filter

2.2 Supply voltage sequencing

Figure 6 shows requirements in the sequencing of the I/O V_{DD} (EV_{DD}), FlexBus V_{DD} (FBV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (VDD_OSC_A_PLL), and internal logic/core V_{DD} (IV_{DD}).



Notes:
1. Input voltage must not be greater than the supply voltage (EV_{DD}, FBV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
2. Use 25 V/millisecond or slower rise time for all supplies.

Figure 6. Supply voltage sequencing and separation cautions

The relationships between FBV_{DD}, SDV_{DD} and EV_{DD} are non-critical during power-up and power-down sequences. FBV_{DD} (1.8 – 3.3V), SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.

NOTE

All I/O VDD pins must be powered on when the device is functioning, except when in standby mode.

In standby mode, all I/O VDD pins, except VSTBY_RTC (battery), can be switched off.

Table 3. Estimated power consumption specifications (continued)

Characteristic	Symbol	Typical	Unit
External I/O pad operating supply current (nominal 3.3 V)	EVDD	—[3]	mA
USB operating supply current (nominal 3.3 V)	VDD_USBO, VDD_USBH	30	mA
ADC operating supply current (nominal 3.3 V) Speed mode 00 Speed mode 01	VDDA_ADC	 14 22	mA
DAC operating supply current (nominal 3.3 V)	VDDA_DAC_ADC	11	mA
RTC standby supply current ISTBY	VSTBY_RTC	17	µA

1 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

2 DDR2 interface power is estimated from the Micron DDR2 data sheet. The numbers given in this table do not include the actual power consumption of the memory itself. The current drawn by the memory needs to be added to the values in this table and may be several hundred mA.

3 EVDD values depend on the application, with the restrictions that any single pin cannot exceed 25 mA and that the total power does not exceed the thermal characteristics.

3 Pin assignments and reset states

3.1 Signal multiplexing

The following table lists all the MCF5441*x* pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to the following sections for package diagrams. For a more detailed discussion of the MCF5441*x* signals, consult the *MCF5441x Reference Manual* (MCF54418RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_AD23), while designations for multiple signals within a group use brackets (i.e., FB_AD[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO default to their GPIO functionality. See the following table for a list of the exceptions.

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
FlexCAN 1									
CAN1_TX	PB0	UART9_TXD	I2C1_SCL	—	I/O	EVDD	ssr	—	D14
CAN1_RX	PC7	UART9_RXD	I2C1_SDA	—	I/O	EVDD	ssr	—	D15
SDRAM controller									
SD_A14	—	—	—	—	O	SDVDD	st_dec ap	—	P6
SD_A[13:0]	—	—	—	—	O	SDVDD	st_dec ap	P3, M1, M3, L2, L1, N4, M2, P2, L3, L4, N1, N2, K1, N3	R4, R1, R3, N4, P3, T4, R2, T2, N3, P5, P4, N5, P2, T3
SD_BA[2:0]	—	—	—	—	O	SDVDD	st_dec ap	M6, J4, P4	P7, N6, R5
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	st_dec ap	K4	N8
SD_CKE	—	—	—	—	O	SDVDD	st_dec ap	N6	R7
SD_CLK	—	—	—	—	O	SDVDD	st_ck	P6	T5
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	st_ck	P7	T6
$\overline{\text{SD\_CS}}$	—	—	—	—	O	SDVDD	st_dec ap	M5	N7
SD_D[7:0]	—	—	—	—	I/O	SDVDD	st_odt	P11, M10, N10, M9, P10, M8, N8, M7	T12, R11, T11, R10, N9, T10, P9, R9
SD_DM	—	—	—	—	O	SDVDD	st_odt	N7	T7
SD_DQS	—	—	—	—	I/O	SDVDD	st_dqs	P8	T8
$\overline{\text{SD\_DQS}}$	—	—	—	—	I/O	SDVDD	st_dqs	P9	T9
SD_ODT	—	—	—	—	O	SDVDD	st_dec ap	P5	P8
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	st_dec ap	M4	R6
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	st_dec ap	N5	R8
SD_VREF	—	—	—	—	—	SDVDD	st_vref	N9	P10
SD_VTT	—	—	—	—	—	SDVDD	st_vtt	L8	N10

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
External interrupts port									
$\overline{\text{IRQ7}}$	PC6	—	—	—	I	EVDD	ssr	G10	F12
$\overline{\text{IRQ6}}$	PC5	—	USB_CLKIN[11]	—	I	EVDD	ssr	—	N1
$\overline{\text{IRQ4}}$	PC4	$\overline{\text{DREQ0}}$	—	—	I	EVDD	ssr	E11	F14
$\overline{\text{IRQ3}}$	PC3	DSPI0_PCS3	USBH_VBUS_EN	—	I	EVDD	ssr	—	M1
$\overline{\text{IRQ2}}$	PC2	DSPI0_PCS2	USBH_VBUS_OC	—[12]	I	EVDD	ssr	—	M2
$\overline{\text{IRQ1}}$	PC1	—	—	—	I	EVDD	ssr	E13	F13
USB On-the-Go									
USBO_DM	—	—	—	—	I/O	VDD_USB0	ae	B13	A14
USBO_DP	—	—	—	—	I/O	VDD_USB0	ae	A13	B14
USB host									
USBH_DM	—	—	—	—	I/O	VDD_USBH	ae	—	A15
USBH_DP	—	—	—	—	I/O	VDD_USBH	ae	—	B15
ADC									
ADC_IN7/ DAC1_OUT	—	—	—	—	I	VDDA_DAC_ADC	ae	—	K3
ADC_IN[6:4]	—	—	—	—	I	VDDA_ADC	ae	—	H2, J3, G4
ADC_IN3/ DAC0_OUT	—	—	—	—	I	VDDA_DAC_ADC	ae	—	K4
ADC_IN[2:0]	—	—	—	—	I	VDDA_ADC	ae	—	J2, J1, H1
Real time clock									
RTC_EXTAL	—	—	—	—	I[4]	VSTBY	ae	B14	B16
RTC_XTAL	—	—	—	—	O	VSTBY	ae	C14	C16
DSPI0/SBF[13]									
DSPI0_PCS1/ $\overline{\text{SBF\_CS}}$	PC0	—	—	—	I/O	EVDD	msr	K3	L1

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
Enhanced secure digital host controller									
SDHC_DAT3	PF2	PWM_A1	DSPI1_PCS0	—	I/O	EVDD	msr	—	B13
SDHC_DAT2	PF1	PWM_B1	DSPI1_PCS2	—	I/O	EVDD	msr	—	E14
SDHC_DAT1	PF0	PWM_A2	DSPI1_PCS1	—	I/O	EVDD	msr	—	D12
SDHC_DAT0	PG7	PWM_B2	DSPI1_SOUT	—	I/O	EVDD	msr	—	B12
SDHC_CMD	PG6	PWM_B0	DSPI1_SIN	—	I/O	EVDD	msr	—	C11
SDHC_CLK	PG5	PWM_A0	DSPI1_SCK	—	O	EVDD	msr	—	A10
Smart card interface 0									
SIM0_DATA	RGPIO13/PG4	PWM_FAULT2	SDHC_DAT7	—	I/O	EVDD	msr	—	E12
SIM0_VEN	RGPIO12/PG3	PWM_FAULT0	—	—	O	EVDD	msr	—	D13
SIM0_RST	RGPIO11/PG2	PWM_FORCE	SDHC_DAT6	—	O	EVDD	msr	—	C15
SIM0_PD	RGPIO10/PG1	PWM_SYNC	SDHC_DAT5	—	I	EVDD	msr	—	C14
SIM0_CLK	RGPIO9/PG0	PWM_FAULT1	SDHC_DAT4	—	O	EVDD	msr	—	A11
Synchronous serial interface 0[19]									
SSI0_RXD	PH7	I2C2_SDA	SIM1_VEN	—	I	EVDD	msr	B12	C12
SSI0_TXD	PH6	I2C2_SCL	SIM1_DATA	—	O	EVDD	msr	A11	C13
SSI0_FS	PH5	UART7_TXD	SIM1_RST	—	I/O	EVDD	msr	C13	E15
SSI0_MCLK	PH4	SSI_CLKIN	SIM1_CLK	—	O	EVDD	msr	A12	A12
SSI0_BCLK	PH3	UART7_RXD	SIM1_PD	—	I/O	EVDD	msr	D13	A13
Ethernet subsystem									
MII0_MDC	PI1	RMII0_MDC[20]	—	—	O	EVDD	fsr	N14	P16
MII0_MDIO	PI0	RMII0_MDIO[20]	—	—	I/O	EVDD	fsr	M14	N16
MII0_RXDV	PJ7	RMII0_CRS_DV[20]	—	—	I	EVDD	fsr	M13	P14
MII0_RXD[1:0]	PJ[6:5]	RMII0_RXD[1:0][20]	—	—	I	EVDD	fsr	P13, N13	R15, T15
MII0_RXER	PJ4	RMII0_RXER[20]	—	—	I	EVDD	fsr	M12	N14
MII0_TXD[1:0]	PJ[3:2]	RMII0_TXD[1:0][20]	—	—	O	EVDD	fsr	L12, L11	R13, P13
MII0_TXEN	PJ1	RMII0_TXEN[20]	—	D[21]	O	EVDD	fsr	N12	P12
MII0_COL	PJ0	RMII1_MDC	ULPI_STP	—	I	EVDD	fsr	—	R12
MII0_TXER	PK7	RMII1_MDIO	ULPI_DATA4	—	O	EVDD	fsr	—	R14
MII0_CRS	PK6	RMII1_CRS_DV	ULPI_DATA5	—	I	EVDD	fsr	—	P11
MII0_RXD[3:2]	PK[5:4]	RMII1_RXD[1:0]	ULPI_DATA[1:0]	—	I	EVDD	fsr	—	P15, N13

Table 5. MCF5441*x* Signal information and muxing (continued)

Signal name	GPIO	Alternate 1	Alternate 2	Pullup (U)[1] Pulldown (D)	Direction[2]	Voltage domain	Pad type[3]	196 MAPBGA	256 MAPBGA
MII0_RXCLK	PK3	RMII1_RXER	ULPI_DATA6	—	I	EVDD	fsr	—	M14
MII0_TXD[3:2]	PK[2:1]	RMII1_TXD[1:0]	ULPI_DATA[3:2]	—	O	EVDD	fsr	—	T13, N12
MII0_TXCLK	PK0	RMII1_TXEN	ULPI_DATA7	D[21]	I	EVDD	fsr	—	T14
BDM/JTAG									
ALLPST[22]	PH2	—	—	—	O	EVDD	fsr	K12	—
DDATA[3:2]	PH[1:0]	—	—	—	O	EVDD	fsr	—	L15, M13
DDATA[1:0]	PI[7:6]	—	—	—	O	EVDD	fsr	—	M15, L14
PST[3:0]	PI[5:2]	—	—	—	O	EVDD	fsr	—	J13, J16, J15, J14
JTAG_EN	—	—	—	D	I	EVDD	msr	N11	N15
PSTCLK	—	TCLK[23]	—	—	I	EVDD	fsr	L14	M16
DSI	—	TDI[23]	—	U	I	EVDD	msr	L10	L13
DSO	—	TDO[23]	—	—	O	EVDD	msr	L13	K14
$\overline{\text{BKPT}}$	—	TMS[23]	—	U	I	EVDD	msr	K13	K16
DSCLK	—	$\overline{\text{TRST}}$[23]	—	U	I	EVDD	msr	L9	K13
Test (this signal must be grounded)									
TEST	—	—	—	D	I	EVDD	ssr	K10	R16
Power supplies									
IVDD	—	—	—	—	—	—	—	D9, D10, E9, E10, F9, F10, F12	E9–E11, F9–F11
EVDD	—	—	—	—	—	—	—	F4–F7, G6, G7, H6, H7, J5, J6	H8, J7–J10, K6–K11, L6
FB_VDD	—	—	—	—	—	—	—	D5–D7, E4–E7	E5–E7, F5, F6, G5
SD_VDD	—	—	—	—	—	—	—	K7–K9, L5–L7	M7–M12
VDD_OSC_A_PLL	—	—	—	—	—	—	vddint	F14	F15
VSS_OSC_A_PLL	—	—	—	—	—	—	vddint	F13	F16
VDD_USBO	—	—	—	—	—	—	vdde	F11	G12
VDD_USBH	—	—	—	—	—	—	vdde	—	H12
VDDA_ADC	—	—	—	—	—	—	—	—	H4

3.2 Pinout—196 MAPBGA

The pinout for the MCF54410 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	GND	FB_AD10	FB_AD14	FB_AD16	FB_AD18	FB_AD19	FB_AD24	FB_AD27	FB_AD30	FB_AD31	SSI0_TXD	SSI0_MCLK	USB_DPLS	GND	A
B	FB_AD6	FB_AD9	FB_AD11	FB_AD13	FB_AD17	FB_AD20	FB_AD23	FB_AD26	FB_AD29	U1_RXD	U0_TXD	SSI0_RXD	USB_DMNS	RTC_EXTAL	B
C	FB_AD3	FB_AD5	FB_AD8	FB_AD12	FB_AD15	FB_AD21	FB_AD22	FB_AD25	FB_AD28	U1_TXD	U0_RXD	U0RTS_B	SSI0_FS	RTC_XTAL	C
D	FB_AD0	FB_AD2	FB_AD4	FB_AD7	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	U1RTS_B	U1CTS_B	SSI0_BCLK	GND	D
E	FB_BE2_B	FB_ALE	FB_AD1	FBVDD	FBVDD	FBVDD	FBVDD	GND	CVDD	CVDD	IRQ4_B	U0CTS_B	IRQ1_B	VSTBY	E
F	FB_BE0_B	FB_BE1_B	FB_BE3_B	EVDD	EVDD	EVDD	EVDD	GND	CVDD	CVDD	VDD_USBO	CVDD	VSS_OSC_A_PLL	VDD_OSC_A_PLL	F
G	FB_CLK	FB_CS0_B	FB_CS1_B	GND	BOOTMOD1	EVDD	EVDD	GND	GND	IRQ7_B	GND	I2C0_SDA	T3IN	EXTAL	G
H	FB_OE_B	FB_RW_B	FB_TA_B	GND	BOOTMOD0	EVDD	EVDD	GND	GND	GND	GND	I2C0_SCL	T1IN	XTAL	H
J	DSPI0_PCS0	DSPI0_SOUT	DSPI0_SCK	SD_BA1	EVDD	EVDD	GND	GND	GND	GND	GND	T2IN	T0IN	GND	J
K	SD_A1	DSPI0_SIN	DSPI0_PCS1	SD_CAS_B	GND	GND	SDVDD	SDVDD	SDVDD	TEST	GND	ALLPST	TMS	RSTIN_B	K
L	SD_A9	SD_A10	SD_A5	SD_A4	SDVDD	SDVDD	SDVDD	SD_VTT	TRST_B	TDI	RM110_TXD0	RM110_TXD1	TDO	TCLK	L
M	SD_A12	SD_A7	SD_A11	SD_RAS_B	SD_CS_B	SD_BA2	SD_D0	SD_D2	SD_D4	SD_D6	OWIO	RMII0_RXER	RMII0_CRS_DV	RMII0_MDIO	M
N	SD_A3	SD_A2	SD_A0	SD_A8	SD_WE_B	SD_CKE	SD_DQM	SD_D1	SD_VREF	SD_D5	JTAG_EN	RMII0_TXEN	RMII0_RXD0	RMII0_MDC	N
P	GND	SD_A6	SD_A13	SD_BA0	SD_ODT	SD_CLK	SD_CLK_B	SD_DQS	SD_DQS_B	SD_D3	SD_D7	RSTOUT_B	RMII0_RXD1	GND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 7. MCF54410 Pinout (196 MAPBGA)

4 Electrical characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5441*x* microprocessor. This section contains detailed information on AC/DC electrical characteristics and AC timing specifications.

NOTE

The specifications for this device in any other document are superseded by the specifications in this document.

4.1 Absolute maximum ratings

Table 6. Absolute maximum ratings[1, 2]

Rating	Symbol	Pin name	Value	Units
External I/O pad supply voltage	EV_{DD}	EVDD	–0.3 to +4.0	V
Internal logic supply voltage	IV_{DD}	IVDD	–0.5 to +2.0	V
FlexBus I/O pad supply voltage	FBV_{DD}	FB_VDD	–0.3 to +4.0	V
SDRAM I/O pad supply voltage	SDV_{DD}	SD_VDD	–0.3 to +4.0	V
PLL supply voltage	PV_{DD}	VDD_OSC_A_PLL	–0.3 to +4.0	V
USB OTG supply voltage	$USBV_{DD}$	VDD_USBO	–0.3 to +4.0	V
USB host supply voltage	$USBV_{DD}$	VDD_USBH	–0.3 to +4.0	V
ADC supply voltage	AV_{DD}	VDDA_ADC	–0.3 to +4.0	V
DAC and ADC supply voltage	—	VDDA_DAC_ADC	–0.3 to +4.0	V
RTC standby supply voltage	$RTCV_{STBY}$	VSTBY_RTC	–0.3 to +4.0	V
Digital input voltage[3]	V_{IN}	—	–0.3 to +3.6	V
Instantaneous maximum current Single pin limit (applies to all pins) [3, 4, 5]	I_{DD}	—	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	—	–40 to +85	°C
Storage temperature range	T_{stg}	—	–55 to +150	°C

1 Functional operating conditions are given in Table 11. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Immunity to static and electrical fields is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD} .

5 Power supply must maintain regulation within operating EV_{DD}, FBV_{DD}, and SDV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$, FBV_{DD}, or SDV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD}, FBV_{DD}, or SDV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD}, FBV_{DD}, or SDV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (for example, no clock).

Table 10. Power supply specifications (continued)

Characteristic	Symbol	Pin Name	Min	Max	Units
External I/O pad supply voltage, nominal 3.3 V	EV_{DD}	EVDD	3.135	3.63	V
USB supply voltage, nominal 3.3 V	$USBV_{DD}$	VDD_USBO VDD_USBH	3.135	3.63	V
ADC supply voltage	AV_{DD}	VDDA_ADC	3.135	3.63	V
DAC supply voltage	—	VDDA_DAC_ ADC	3.135	3.63	V
RTC standby supply voltage	$RTCV_{STBY}$	VSTBY_RTC	1.6	EV_{DD} – 0.2V	V

Table 11. I/O electrical specifications

Characteristic	Symbol	Min	Max	Units
CMOS input high voltage	EV_{IH}	0.65 × EV_{DD}	EV_{DD} + 0.3	V
CMOS input low voltage	EV_{IL}	V_{SS} – 0.3	0.35 × EV_{DD}	V
CMOS output high voltage I_{OH} = –2.0 mA	EV_{OH}	0.8 × EV_{DD}	—	V
CMOS output low voltage I_{OL} = 2.0 mA	EV_{OL}	—	0.2 × EV_{DD}	V
SDRAM input high voltage DDR2 @ 1.8V	SDV_{IH}	SDV_{REF} + 0.125	SDV_{DD} + 0.3	V
SDRAM input low voltage DDR2 @ 1.8V	SDV_{IL}	–0.3	SDV_{REF} – 0.125	V
SDRAM output high voltage DDR2@ 1.8V I_{OH} = –13.4 mA	SDV_{OH}	SDV_{DD} × 0.9	—	V
SDRAM output low voltage DDR2@ 1.8V I_{OH} = 13.4 mA	SDV_{OL}	—	SDV_{DD} × 0.1	V
FlexBus input high voltage @ 1.8V–3.3V	FBV_{IH}	0.51 × FBV_{DD}	FBV_{DD} + 0.3	V
FlexBus input low voltage @ 1.8V–3.3V	FBV_{IL}	V_{SS} – 0.3	0.42 × FBV_{DD}	V
FlexBus output high voltage @ 1.8V–3.3V I_{OH} = –5.0 mA for all modes	FBV_{OH}	0.8 × FBV_{DD}	—	V
FlexBus output low voltage @ 1.8V–3.3V I_{OL} = 5.0 mA for all modes	FBV_{OL}	—	0.2 × FBV_{DD}	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA

4.8 Oscillator and PLL electrical characteristics

Reference Figure 9 for crystal circuits.

Table 14. PLL electrical characteristics

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[1] Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 14[1] 14[1]	 50[1] 50[1]	 MHz MHz
2	Core frequency FB_CLK frequency[2] (MISCCR2[FBHALF] = 0)	f_{sys} $f_{sys/2}$	120 60	250 100	MHz MHz
3	VCO frequency	f_{vco}	240	500	MHz
4	DCC frequency[3]	f_{DCC}	300	500	MHz
5	Crystal start-up time[4, 5]	t_{cst}	—	10	ms
6	EXTAL input high voltage External and limp modes	V_{IHEXT}	EV_{IH}	EVDD	V
7	EXTAL input low voltage External and limp modes	V_{ILEXT}	0	EV_{IL}	V
8	PLL lock time [4, 6]	t_{lpll}	—	50	ms
9	Duty cycle of reference [4]	t_{dc}	–45%	+45%	%
10	Crystal capacitive load	C_L	—	From crystal spec	pF
11	Feedback resistor	R_F	10	—	MΩ
12	Series resistor	R_S	0	200	Ω
13	Discrete load capacitance for XTAL	C_{L_XTAL}	—	$2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}	—	$2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[7]	pF
15	FB_CLK period jitter, [4, 5, 7, 8,] Measured at f_{SYS} Max Peak-to-peak jitter (clock edge to clock edge) Long term jitter	C_{jitter}	 — —	 10 0.1	 % $f_{sys/3}$ % $f_{sys/3}$

1 These reference value ranges are for after a PLL predivider (PREDIV), which can be programmed to 1, 2, 4, 8, or 16. The PREDIV value can be set while booting from serial flash. In parallel reset configuration, the PREDIV value is set to one. In this mode, if the input frequency results in an out of range reference frequency, boot the processor in limp mode, set the proper PREDIV and multiplier settings, and switch to PLL mode.

2 All internal registers retain data at 0 Hz.

3 Required only for DDR2 memory.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification is the PLL lock time only and does not include oscillator start-up time.

7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

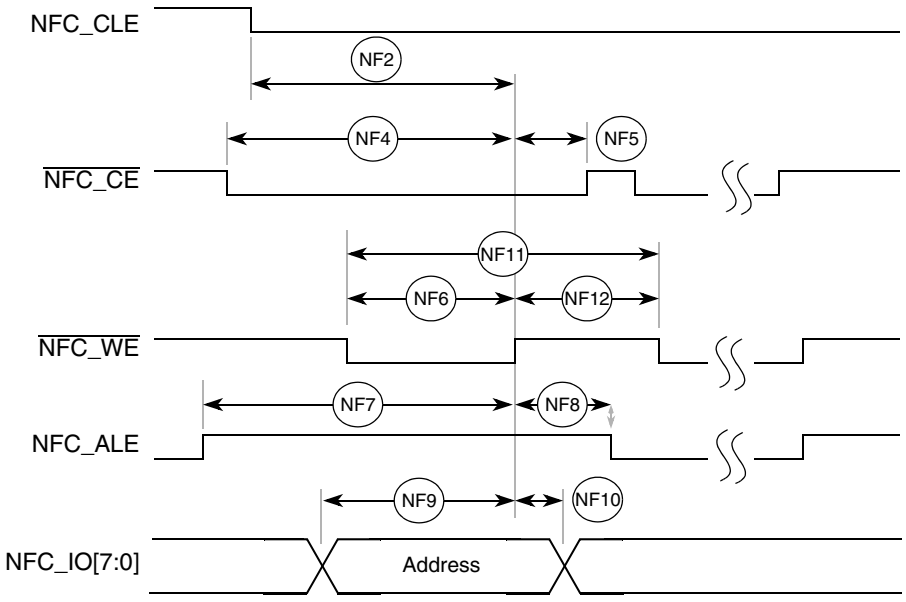


Figure 14. Address latch cycle timing

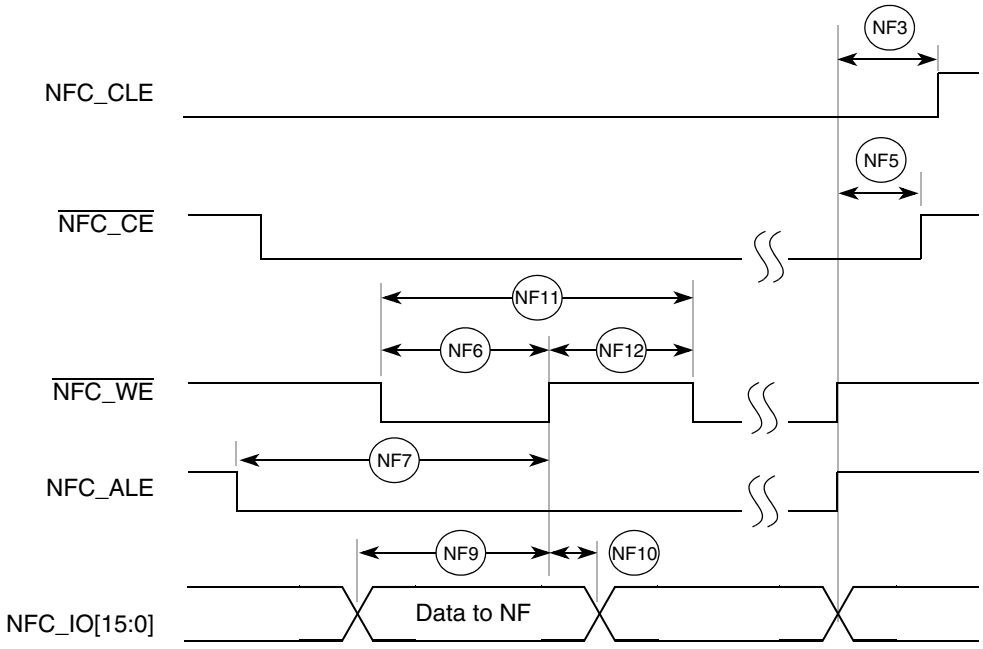


Figure 15. Write data latch timing

3 This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

4 The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

5 This specification relates to the required hold time of DDR memories. SD_D[31:24] is relative to SD_DQS[3]; SD_D[23:16] is relative to SD_DQS[2]

6 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

7 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

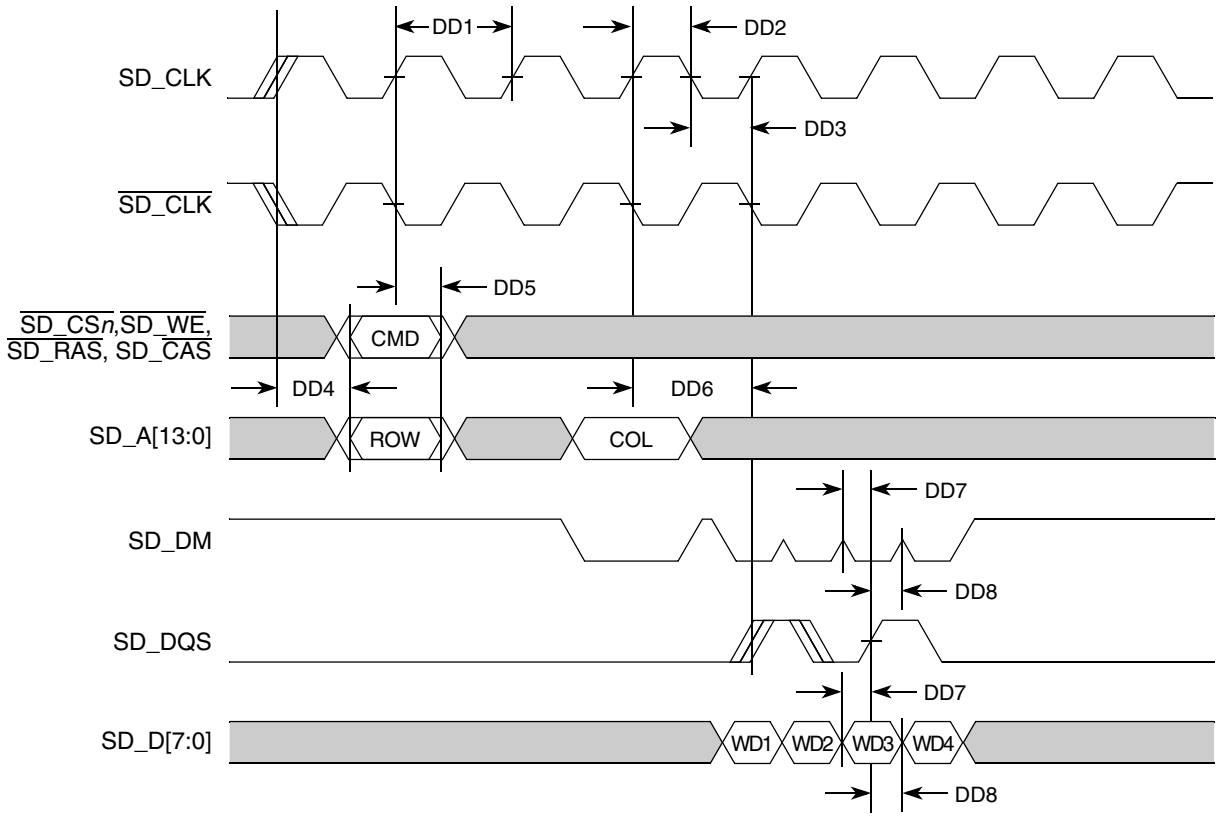


Figure 17. DDR write timing

4.15.2 eSDHC electrical DC characteristics

Table 21 lists the eSDHC electrical DC characteristics.

Table 21. MMC/SD interface electrical specifications

Num	Parameter	Design value	Min	Max	Unit	Condition/remark
Bus signal line load						
7	Pull-up resistance	47	10	100	kΩ	Internal PU
8	Open drain resistance	NA	NA	NA	kΩ	For MMC cards only
Open drain signal level						For MMC cards only
9	Output high voltage		V_{DD} – 0.2		V	I_{OH} = –100 µA
10	Output low voltage			0.3	V	I_{OL} = 2 mA
Bus signal levels						
11	Output high voltage		0.75 x V_{DD}		V	I_{OH} = –100 µA @V_{DD} min
12	Output low voltage			0.125 x V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
13	Input high voltage		0.625 x V_{DD}	V_{DD} + 3	V	
14	Input low voltage		V_{SS} – 0.3	0.25 x V_{DD}	V	

4.16 SIM timing specifications

Each SIM card interface consist of a total of 12 pins (two separate ports of six pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data, like a standard UART. All six (or five when a bidirectional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other. There are no required timing relationships between the signals in normal mode. However, there are some in reset and power down sequences.

All SIM signals use pad type pad_msr. SIM timing is fairly relaxed compared to other interfaces and can be met at 50 pF loading with any slew rate setting other than 00.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

4.16.2.2 Cards with active-low reset

The sequence of reset for this kind of card is as follows (see Figure 23):

1. After powerup, the clock signal is enabled on SIM_CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. SIM_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
4. SIM_RST is set high (time T1)
5. SIM_RST must remain high for at least 40,000 clock cycles after T1 and a response must be received on RX between 400 and 40,000 clock cycles after T1.

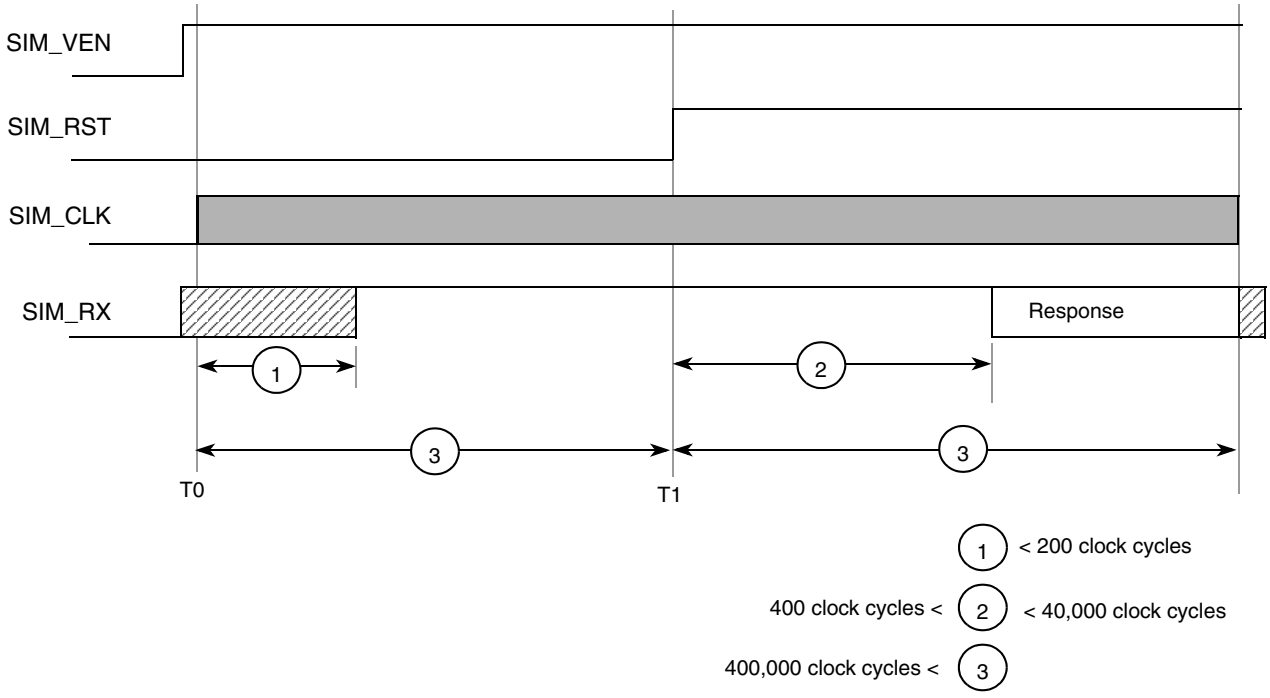


Figure 23. Active-low-reset card reset sequence

4.16.3 Power-down sequence

Power down sequence for SIM interface is as follows:

1. SIM_PD port detects the removal of the SIM card
2. SIM_RST goes low
3. SIM_CLK goes low
4. SIM_TX goes low
5. SIM_VEN goes low

Each of these steps is completed in one CKIL period (usually 32 kHz). Power-down may be started in response to a card-removal detection or launched by the processor. Figure 24 and Table 23 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

Table 23. Timing requirements for power-down sequence

Num	Description	Symbol	Min	Max	Unit
1	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 ÷ f_{CKIL}	0.8	µs
2	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8 ÷ f_{CKIL}	1.2	µs
3	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 ÷ f_{CKIL}	1.8	µs
4	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 ÷ f_{CKIL}	25	ns

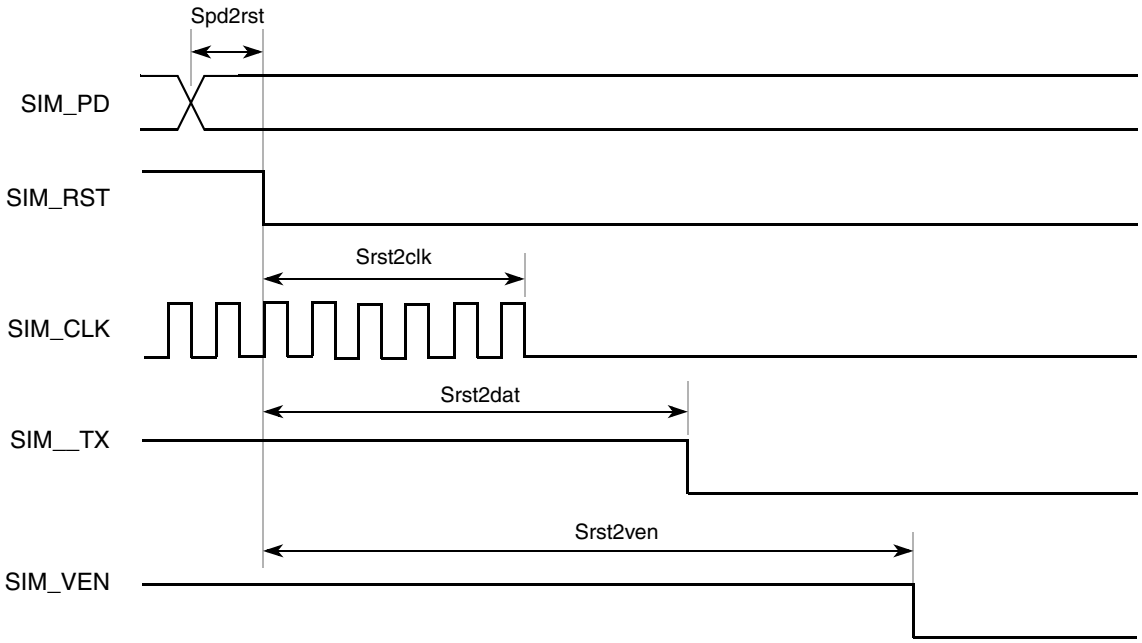


Figure 24. SmartCard interface power-down AC timing

4.17 SSI timing specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

All SSI signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF. When the SSI_MCLK output is not used, the maximum SSI bit clock (SSI_BCLK) frequency is such that timing can also be met at slew rate settings 10 and 01.[1]

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

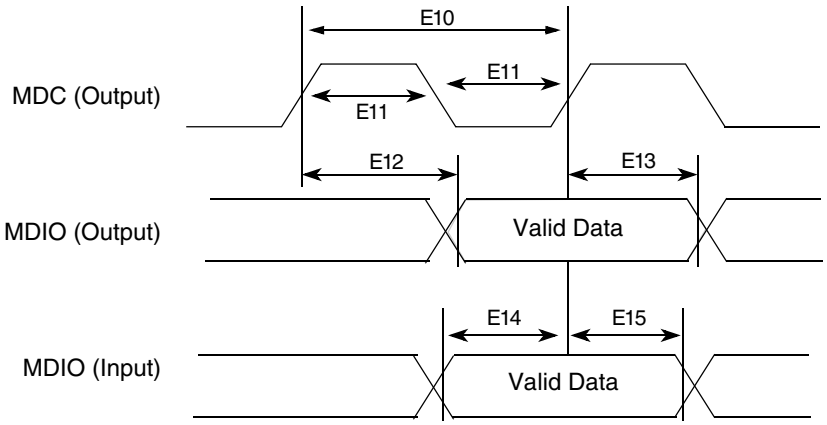


Figure 31. MDIO serial management channel timing diagram

4.23 32-bit timer module timing specifications

Table 35 lists timer module AC timings.

Table 35. Timer module AC timing specifications

Name	Characteristic	Min	Max	Unit
T1	DT*n*IN cycle time (*n* = 0:3)	3	—	$1/f_{SYS/2}$
T2	DT*n*IN pulse width (*n* = 0:3)	1	—	$1/f_{SYS/2}$

4.24 DSPI timing specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. Table 36 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF54418 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

All DSPI signals use pad type pad_msr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 36. DSPI module AC timing specifications[1]

Name	Characteristic	Symbol	Min	Max	Unit	Notes
Master Mode						
—	DSPI_SCK frequency	f_{SCK}	—	50	MHz	
DS1	DSPI_SCK cycle time	t_{SCK}	20	—	ns	2
DS2	DSPI_SCK duty cycle	—	$(t_{sck} \div 2) - 2.0$	$(t_{sck} \div 2) + 2.0$	ns	3
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	$(t_{sck} \div 2) - 2.0$	—	ns	4
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	$(t_{sck} \div 2) - 3.0$	—	ns	5
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

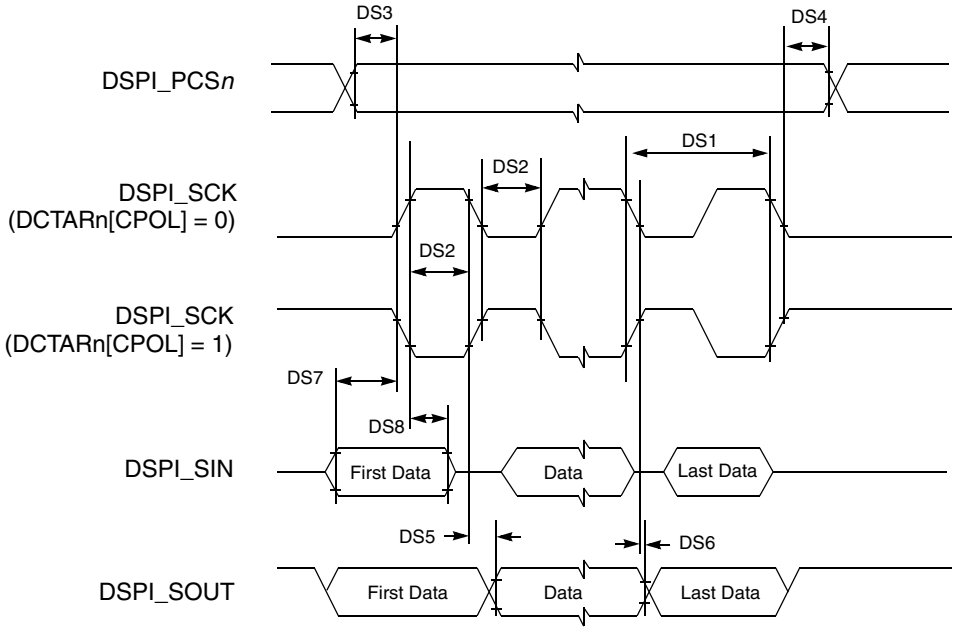


Figure 32. DSPI Classic SPI timing — master Mode

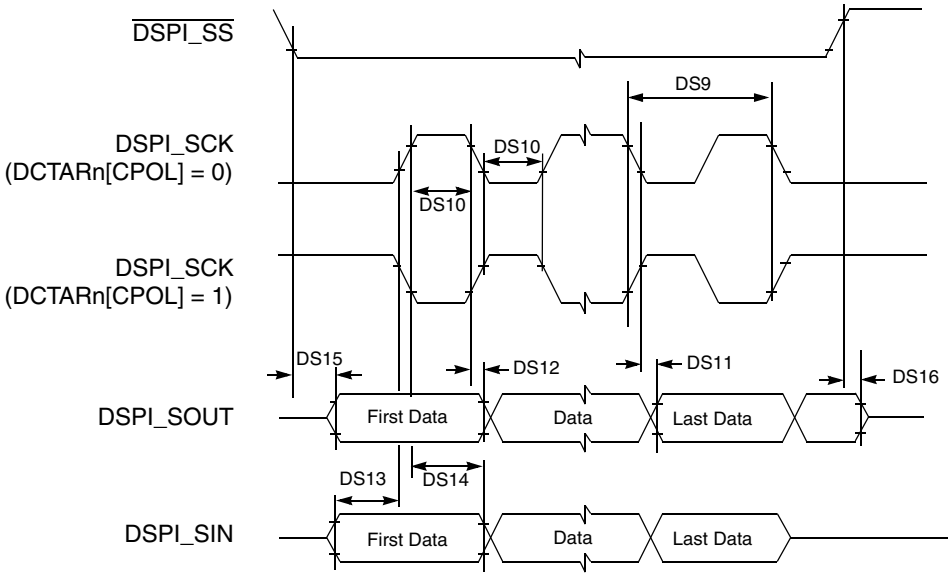


Figure 33. DSPI Classic SPI timing — slave mode

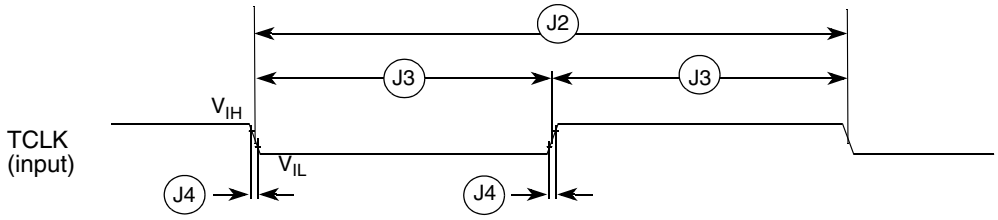


Figure 37. Test clock input timing

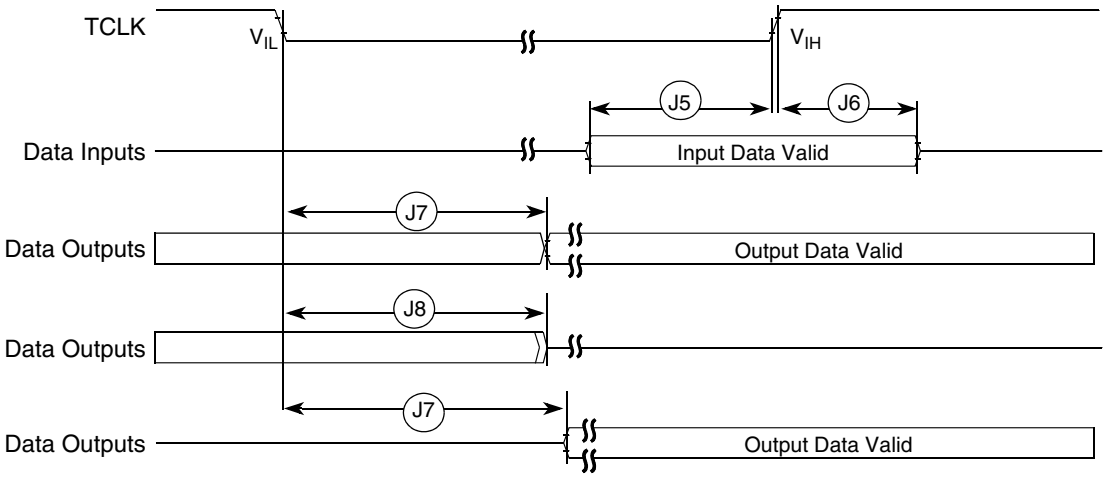


Figure 38. Boundary scan (JTAG) timing

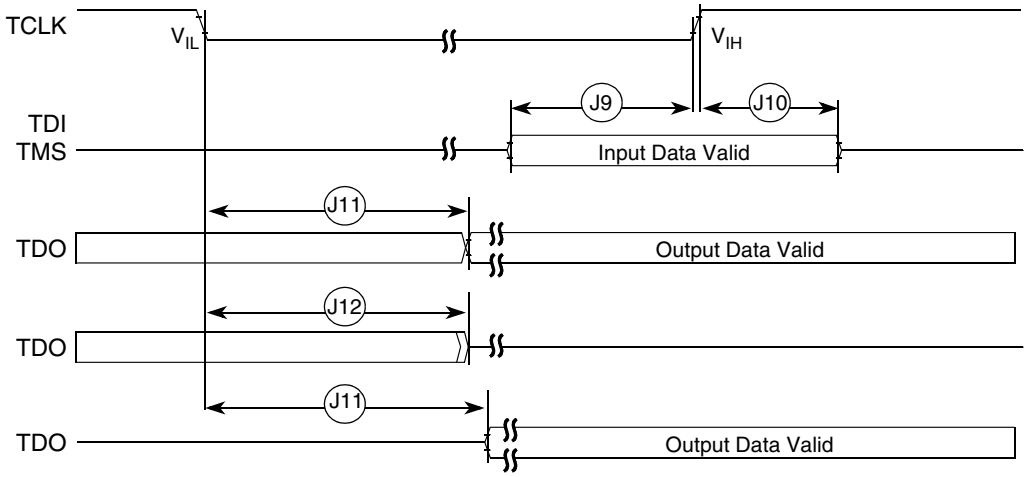


Figure 39. Test access port timing

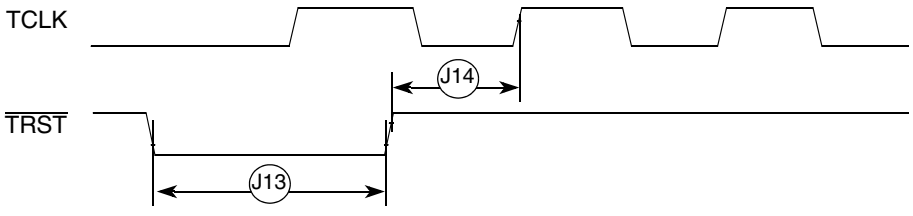


Figure 40. $\overline{\text{TRST}}$ timing

4.30 Debug AC timing specifications

Table 41 lists specifications for the debug AC timing parameters shown in Figure 41 and Table 42.

All debug signals use pad type pad_msr except for PSTCLK which use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF.[1]

Table 41. Debug AC timing specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	0.5	0.5	$1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	0.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

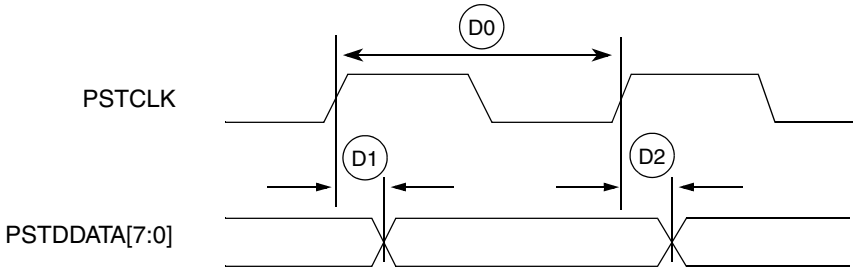


Figure 41. Real-time trace AC timing

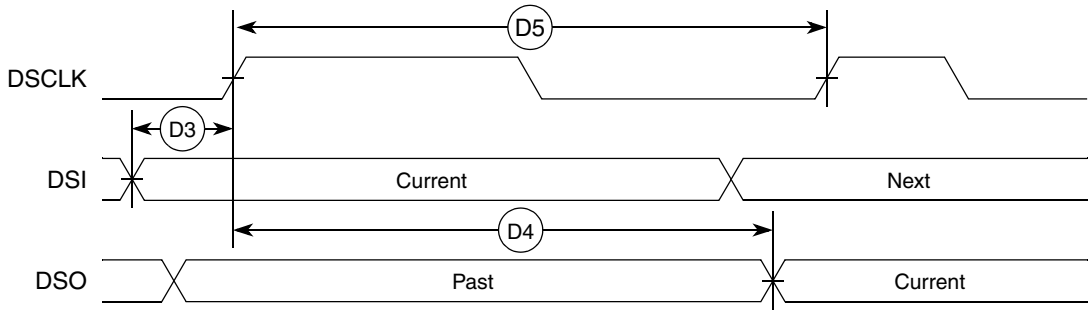


Figure 42. BDM serial port AC timing

1.These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 43. Revision history (continued)

Rev. No.	Date	Summary of changes
3	31 July 2009	Changed 169MAPBGA package to 196MAPBGA throughout. MCF54410 device now supports a single SSI module and one Ethernet controller with IEEE 1588 support
4	17 Aug 2009	Updated MCF5441*x* Signal Information and Muxing table with 196MAPBGA pin locations Changed SD_D*n* pin locations on 256 MAPBGA package Added note to Section 4.6, "Output pad loading and slew rate"
5	29 Jan 2010	Added orderable part numbers
6		Swapped locations of RTC_EXTAL and RTC_XTAL pins in Table 5, Figure 7, and Figure 8 Corrected instances of MCF5445*x* to MCF5441*x* Added thermal characteristic s to Table 7 Added case outline numbers to Table 42 Changed PLL supply voltage from "–0.5 to +2.0" to "–0.3 to +4.0" in Table 6 Miscellaneous corrections based on information from shared review comments by team members
7	October 2011	• Updated the pinouts in Table 5, "MCF5441x Signal information and muxing". • Updated the Figure 7, "MCF54410 Pinout (196 MAPBGA)". • Removed the symbol ADC_IN7/DAC1_OUT from Table 9, "Latch-up results". • Updated Table 11, "I/O electrical specifications". • Updated Table 13, "DDR pad drive strengths".
8	June 2012	• In Table 7, added the thermal characteristics for the 196 MAPBGA package. • In Table 42, updated the case outline number for the 196 MAPBGA package from "98ARH98217" to "98ASA00321D".