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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	31
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.5K × 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-XFQFN Exposed Pad
Supplier Device Package	40-HXQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213j4tnnp-w4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Item	Function	Specification			
Serial	UART0	Clock synchronous serial I/O/UART			
Interface	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), SSU mode, multiprocessor communication function			
LIN Module	•	Hardware LIN: 1 (timer RA, UART0)			
A/D Converter		10-bit resolution \times 12 channels, includes sample and hold function, with sweep mode			
Sensor Contro	l Unit	System CH x 3, electrostatic capacitive touch detection x 22			
Flash Memory		 Programming and erasure voltage: VCC = 2.7 V to 5.5 V Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) Program security: ROM code protect, ID code check Debug functions: On-chip debug, on-board flash rewrite function Background operation (BGO) function 			
Operating Free Voltage	quency/Supply	f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)			
Current Consu	mption	Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μ A (VCC = 3.0 V, wait mode) Typ. 2.0 μ A (VCC = 3.0 V, stop mode)			
Operating Amb	pient Temperature	-20 to 85°C (N version)			
Package		40-pin HXQFN Package code: PXQN0040LA-A			

Table 1.2 Specifications for R8C/3JT Group (2)



1.3 **Block Diagram**

Figure 1.2 shows a Block Diagram.

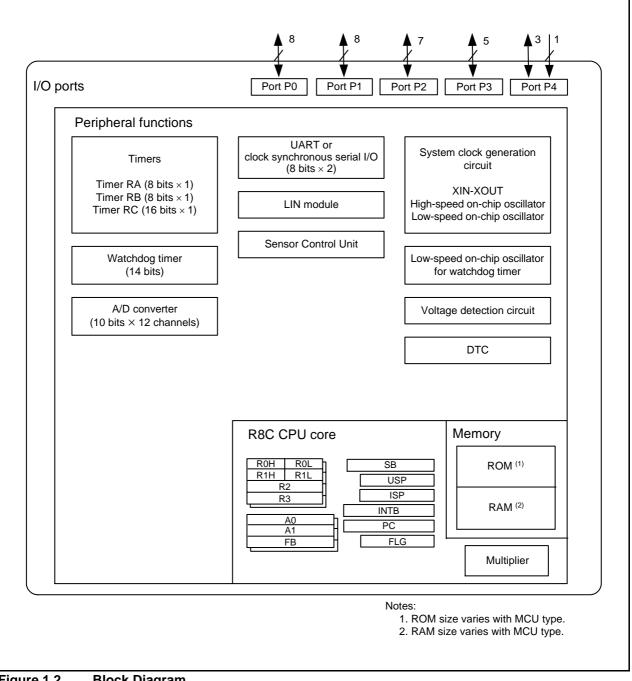


Figure 1.2 **Block Diagram**



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1	SFR Information (1) (1)		
Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	0010000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb ⁽²⁾
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h		l l l l l l l l l l l l l l l l l l l	1
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
			1000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾
			0010000b ⁽⁵⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h		l l l l l l l l l l l l l l l l l l l	1
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4)
	- v		1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
V: Undefined			100010100

Table 4.1SFR Information (1) (1)

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, Software reset, or watchdog timer reset does not affect this bit.

3. The CSPROINI bit in the OFS register is set to 0.

4. The LVDAS bit in the OFS register is set to 1.

5. The LVDAS bit in the OFS register is set to 0.

0038h Volage Monitor 2 Circuit Control Register V2C 10000010B 0038h 0038h 0038h 0038h 0038h	Address	Register	Symbol	After Reset
0032h				
0030h	003Bh			
0038h	003Ch			
0039h	003Dh			
0040h Flash Memory Ready Interrupt Control Register FMRDYIC XXXXX000b 0041h Flash Memory Ready Interrupt Control Register FMRDYIC XXXXX000b 0044h				
0041h Flish Memory Ready Interrupt Control Register PMEDYIC XXXXX000b 0043h -				
0042h				
0044h Image: Second Secon		Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0044h 0044h 0044h 0047h Tmer RC Interrupt Control Register 1RCIC XXXXX000b 0048h 0048h 0048h 0048h 0048h 0048h UART2 Transmit Interrupt Control Register S2TIC XXXXX00b 0040h UART2 Transmit Interrupt Control Register ADIC XXXXX00b 0040h UART0 Transmit Interrupt Control Register ADIC XXXXX00b 0050h 0051h UART0 Receive Interrupt Control Register S0RIC XXXXX00b 0058h Imer R4 Interrupt Control Register TRAIC XXXXX00b 0058h Imer R4 Interrupt Control Register TREIC XXXXX00b 0058h Imer R4 Interrupt Control Register TREIC XXXXX000b 0058h I				
0046h FCIC XXXXX000b 0047h Timer RC Interrupt Control Register TRCIC XXXXX000b 0048h FCIC XXXXX000b 0048h FCIC XXXXX000b 0048h S2TIC XXXXX000b 0048h VART2 Receive Interrupt Control Register S2TIC XXXXX000b 0046h VART2 Receive Interrupt Control Register ADIC XXXXX000b 0046h VART2 Receive Interrupt Control Register ADIC XXXXX00b 0046h VARTO Conversion Interrupt Control Register S0TIC XXXXX00b 0055h VARTO Receive Interrupt Control Register S0TIC XXXXX00b 0055h VARTO Receive Interrupt Control Register S0TIC XXXXX00b 0055h INT2 Interrupt Control Register TRAIC XXXXX00b 0055h INT2 Interrupt Control Register TRAIC XXXXX00b 0055h INT1 Interrupt Control Register INTIC XXXXX00b 0055h INT1 Interrupt Control Register INTIC XXXXX00b 0055h INT3 Interrupt Control Register </td <td></td> <td></td> <td></td> <td></td>				
0044h Imer RC Interrupt Control Register TRGIC XXXXX000b 0044h Imer RC Interrupt Control Register IRGIC XXXXX000b 0044h Imer RC Interrupt Control Register SZTIC XXXXX000b 0044h Imer RC Interrupt Control Register SZTIC XXXXX000b 0044h Imer RC Interrupt Control Register SZTIC XXXXX000b 0044h ADI Conversion Interrupt Control Register SZTIC XXXXX000b 0044h ADI Conversion Interrupt Control Register SOTIC XXXXX00b 0055h UARTO Transmit Interrupt Control Register SOTIC XXXXX00b 0055h UARTO Receive Interrupt Control Register SOTIC XXXXX00b 0055h ITTE Interrupt Control Register INT2IC XX00X00b 0055h ITTE Interrupt Control Register INT3IC XX00X00b <t< td=""><td></td><td></td><td></td><td></td></t<>				
0044h TRCIC XXXX000b 0044h 0044h 0044h 0044h S2TIC XXXX000b 0044h S2TIC XXXX000b 0046h LART2 Receive Interrupt Control Register S2TIC XXXX000b 0046h KUPIC XXXX000b XXXX000b 0046h KupitC XXXX000b XXXX000b 0046h KupitC XXXX000b XXXX000b 0046h ADIC XXXX000b XXXX00b 0046h LART0 Transmit Interrupt Control Register SOTIC XXXX000b 0055h UART0 Transmit Interrupt Control Register SOTIC XXXX000b 0055h INT2 Interrupt Control Register SOTIC XXXX000b 0055h INTE Interrupt Control Register TRAIC XXXX000b 0055h INTE R Interrupt Control Register INTIC XX00X000b 0055h INTI Interrupt Control Register INTIC XX00X000b 0055h INTO Interru				
0049h		Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0040h				70000000
004Ah S2TIC XXXXX000b 004Bi UART2 Transmit Interrupt Control Register S2TIC XXXXX000b 004Db Kkp Input Interrupt Control Register KUPIC XXXXX000b 004Db Kkp Input Interrupt Control Register ADIC XXXXX000b 004DF AD Conversion Interrupt Control Register ADIC XXXXX000b 004Fh ADIC XXXXX000b XXXXX000b 004Fh ADIC XXXXX000b XXXXX000b 005h UART0 Transmit Interrupt Control Register SOFIC XXXXX000b 005h UART0 Teseive Interrupt Control Register SOFIC XXXXX000b 005h IMT2 Interrupt Control Register INT2IC XX00X00b 005h Immer R8 Interrupt Control Register TRAIC XXXXX000b 005h Immer R8 Interrupt Control Register INT11C XX00X00bb 005h INT1 Interrupt Control Register INT11C XX00X00bb 005h INT1 Interrupt Control Register INT0IC XX00X00bb 005h INT1 Interrupt Control Register INT0IC <td< td=""><td></td><td></td><td></td><td></td></td<>				
0044h UART2 Transmit Interrupt Control Register \$211C XXXXX000b 004Ch UART2 Receive Interrupt Control Register KUPIC XXXXX000b 004Dh Key Input Interrupt Control Register ADIC XXXXX000b 004Fh AD Conversion Interrupt Control Register ADIC XXXXX000b 0051h UART0 Transmit Interrupt Control Register SOTIC XXXXX000b 0055h UART0 Receive Interrupt Control Register SOTIC XXXXX000b 0055h IVART0 Transmit Interrupt Control Register SOTIC XXXXX000b 0055h IVT2 Interrupt Control Register TRAIC XXXXX000b 0055h IVT2 Interrupt Control Register TRAIC XXXXX000b 0055h IVT2 Interrupt Control Register TRAIC XX0XX000b 0055h IVT1 Interrupt Control Register TRAIC XX0XX000b 0055h IVT1 Interrupt Control Register IVT1 XX0XX000b 0055h IVT1 Interrupt Control Register IVT1 XX0XX000b 0055h IVT1 Interrupt Control Register IVT1 XX0XX000b				
004Ch UART2 Receive Interrupt Control Register SRIC XXXXX000b 004Dh Key Iput Interrupt Control Register ADIC XXXXX000b 004Eh AD Conversion Interrupt Control Register ADIC XXXXX000b 004Fh ADIC XXXXX000b XXXXX000b 004Fh ADIC XXXXX000b XXXXX000b 005h UART0 Transmit Interrupt Control Register SOFIC XXXXX000b 0055h UART0 Receive Interrupt Control Register SOFIC XXXX000b 0055h INT2 Interrupt Control Register INT2IC XX00X00b 0055h INT2 Interrupt Control Register TRAIC XXXXX00Db 0055h Immer R8 Interrupt Control Register IRTIC XXXXX00Db 0055h INT1 Interrupt Control Register INTIC XX0XX00Db 0055h INT3 Interrupt Control Register INTIC XX0XX00Db 0056h INT0 Interrupt Control Register INTIC XX0XX00Db 0055h INT3 Interrupt Control Register INTIC XX0XX00Db 0055h INT0 Interrupt Control Register<		UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Eh AD Conversion Interrupt Control Register ADIC XXXXX000b 004Fh ADIC XXXXX00b ADIC XXXXX00b 0050h IMRT0 Receive Interrupt Control Register SORIC XXXXX000b 0053h IMRT0 Receive Interrupt Control Register SORIC XXXXX000b 0053h Imer RA Interrupt Control Register INT2IC XXXX000b 0055h INT2 Interrupt Control Register TRAIC XXXXX000b 0055h Imer RA Interrupt Control Register TRAIC XXXXX000b 0055h IINT1 Interrupt Control Register INT1IC XXXX000b 0055h IINT3 Interrupt Control Register INT1IC XX0X000b 0055h IINT3 Interrupt Control Register INT3IC XX0X000b 0055h UART2 Bus Collision Detection Interrupt Control Register UBCNIC XXXXX000b 0055h UART2 Bus Collision Detection Interrupt Control Register UBCNIC XXXXX000b 0055h UART2 Bus Collision Detection Interrupt Control Register UBCNIC XXXXX000b 0065h Imerupt Control Register Imerupt Control	004Ch		S2RIC	XXXXX000b
004Fh 0050h UART0 Transmit Interrupt Control Register SOTIC XXXXX000b 0051h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0053h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0053h INT2 Interrupt Control Register INT2IC XX0000b 0055h Timer RA Interrupt Control Register TRAIC XXXXX000b 0055h Timer RB Interrupt Control Register TRBIC XXXX000b 0055h Timer RB Interrupt Control Register INT3IC XX00000b 0055h Timer RB Interrupt Control Register INT3IC XX00000b 0055h INT1 Interrupt Control Register INT3IC XX00000b 0055h INT0 Interrupt Control Register INT0IC XX0000b 0065h INT0 Interrupt Control Register INT0IC	004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
0050h	004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
0051h UARTO Transmit Interrupt Control Register SOTIC XXXX000b 0052h UARTO Receive Interrupt Control Register SORIC XXXX000b 0053h				
0052h UART0 Receive Interrupt Control Register SORIC XXXX000b 0053h INT2 Interrupt Control Register INT2IC XX0000b 0055h INT2 Interrupt Control Register INT2IC XX0000b 0055h Timer RA Interrupt Control Register TRAIC XXXX000b 0055h Timer RA Interrupt Control Register TRBIC XXXX000b 0055h INT1 Interrupt Control Register TRBIC XXXX000b 0055h INT3 Interrupt Control Register INT3IC XX00X000b 0055h INT0 Interrupt Control Register INT0IC XX00X00b 0055h INT0 Interrupt Control Register U2BCNIC XXXX000b 0055h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXX000b 0055h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXX000b 0065h Int1 Int1 Int2 Int2 Int2 0065h Int2 Int2 Int2 Int2 Int2 0065h Interrupt Control Register U2BCNIC XXXXX000b </td <td></td> <td></td> <td></td> <td></td>				
0063h interrupt Control Register INT2i C XX0000b 0056h Timer RA Interrupt Control Register TRAIC XX0000b 0057h Timer RA Interrupt Control Register TRAIC XX0000b 0058h Timer RA Interrupt Control Register TRAIC XX0000b 0057h Timer RA Interrupt Control Register TRBIC XX0000b 0058h INT3 Interrupt Control Register INT3iC XX0000b 0058h INT3 Interrupt Control Register INT3iC XX0000b 0058h INT3 Interrupt Control Register INT3iC XX0000b 0058h UART2 Bus Collision Detection Interrupt Control Register U28CNIC XXXXX000b 0058h 0061h				
0055h INT2 Interrupt Control Register INT2IC XX00X000b 0055h Timer RA Interrupt Control Register TRAIC XXXXX000b 0057h Timer RB Interrupt Control Register TRBIC XXXXX000b 0058h Timer RB Interrupt Control Register TRBIC XXXXX000b 0059h INT3 Interrupt Control Register INT3IC XX00X000b 0055h INT1 Interrupt Control Register INT3IC XX00X00b 0055h INT0 Interrupt Control Register INT0IC XX00X00b 0055h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXX000b 0056h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXX000b 0066h		UART0 Receive Interrupt Control Register	SORIC	XXXXX000b
0055h INT2 Interrupt Control Register INT2IC XX0X000b 0055h Timer RA Interrupt Control Register TRAIC XXXXX00b 0057h Timer RB Interrupt Control Register INT1IC XX0X00b 0058h Timer RB Interrupt Control Register INT1IC XX000b 0058h INT3 Interrupt Control Register INT3IC XX000b 0058h INT3 Interrupt Control Register INT3IC XX00x00b 0058h INT0 Interrupt Control Register INT0IC XX00x00b 0055h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXx000b 0065h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXX00b 0065h INT0 Interrupt Control Register U2BCNIC XXXX00b 0065h INT0 Interrupt Control Register U2BCNIC XXXX00b 0065h INT0 INT0 Interrupt Control Register Interrupt Control Register 0066h INT0 Interrupt Control Register XXXXX00b Interrupt Control Register 0066h Interrupt Control Register				
0056h Timer RA Interrupt Control Register TRAIC XXXX000b 0057h				
0057h Tmer R Interrupt Control Register TRBIC XXXX000b 0058h INT1 Interrupt Control Register INT3IC XX00X00b 0058h INT3 Interrupt Control Register INT3IC XX00X00b 0056h INT3 Interrupt Control Register INT3IC XX00X00b 0056h INT0 Interrupt Control Register INT0IC XX00X00b 0057h U2RCNIC XXXX000b XXXX00b 0057h U2RCNIC XXXX000b XXX00b 0057h U2RCNIC XXXX00b XXXX00b 0057h U2RCNIC XXXX00b XXXX00b 0057h U2RCNIC XXXX00b XXXX00b 0066h INT0 INT0 INT0 0066h INT0 INT0 INT0 </td <td></td> <td></td> <td>_</td> <td></td>			_	
0058h Timer RB Interrupt Control Register TRBIC XXXXX000b 0059h INT1 Interrupt Control Register INT1IC XX0000b 0058h INT3 Interrupt Control Register INT3IC XX0000b 0058h INT3 Interrupt Control Register INT3IC XX0000b 0058h INT0 Interrupt Control Register INT0IC XX0000b 0058h INT0 Interrupt Control Register INT0IC XX0000b 0058h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXX000b 0058h INT0 INT0IC XX000b INT0 0066h INT0 INT0IC XX000b INT0 0063h INT0 INT0 INT0 INT0 INT0 0066h INT0		Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0059h INT1 Interrupt Control Register INT1IC XX00X00b 005Ah INT3 Interrupt Control Register INT3IC XX00X00b 005Ch 005Ch 005Ch 005Ch 005Ch </td <td></td> <td></td> <td>TRNO</td> <td>XXXXXXX000h</td>			TRNO	XXXXXXX000h
005Ah INT3 Interrupt Control Register INT3IC XX00X000b 005Bh				
005Bh		INTT Interrupt Control Register		
006Ch INTO Interrupt Control Register INTOIC XX00X000b 005Eh UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXX000b 0066h u2BCNIC XXXXX000b 0060h 0061h u2BCNIC XXXXX00b 0062h u2BCNIC XXXXX00b 0063h u2BCNIC XXXXX00b 0064h u2BCNIC XXXXX00b 0065h u2BCNIC XXXXX00b 0066h u2BCNIC XXXX00b 0066h u2BCNIC XXXX00b 0066h u2BCNIC XXXX00b 0066h u2BCNIC XXXXX00b 0066h u2BCNIC XXXXX00b 0066h u2BCNIC XXXXX00b 0066h u2BCNIC XXXXX00b 0066h u2BCNIC XXXXX000b 0066h			INTSIC	XX00X000b
005Dh INT0 Interrupt Control Register INT0IC XX00X000b 005Eh UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXX000b 0067h				
006Eh UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXX000b 0067h		INTO Interrupt Control Register	INTOIC	XX00X000b
006Fh				
0060h Image: Constraint of the second s		Over 12 Das Completing Delection interrupt Control Register	02801110	
0061h				
0062h				
0063h				
0065h				
0065h				
0067h				
0068hImage: control with a	0066h			
0069hSensor Control Unit Interrupt Control RegisterSCUICXXXXX00bb006BhScuicXXXXX00bb006ChScuicScuic006DhScienceScience006EhScienceScience006FhScienceScience006FhScienceScience0070hScienceScience0077hScienceScience0072hVoltage Monitor 1 Interrupt Control RegisterVCMP1IC0073hVoltage Monitor 2 Interrupt Control RegisterVCMP2IC0075hScienceScience0076hScienceScience0077hScienceScien	0067h			
006AhSensor Control Unit Interrupt Control RegisterSCUICXXXX000b006Bh </td <td>0068h</td> <td></td> <td></td> <td></td>	0068h			
006Bh	0069h			
006Ch		Sensor Control Unit Interrupt Control Register	SCUIC	XXXXX000b
006DhImage: constraint of the second sec				
006Eh				
006Fh Image: Constraint of the second se				
0070h				
0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC 0074h 0075h 0076h 0077h 0078h 0079h 0077h				
0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXX000b 0074h 0075h 0076h 0077h 0077h 0077h 0077h 0078h 0079h 007Ah				
0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXX000b 0074h		Valle as Manifes & Intermet Original D	Venera	
0074h				
0075h			VCIVIPZIC	
0076h				
0077h		<u> </u>		
0078h		<u> </u>		
0079h 007Ah		<u> </u>		
007Ah				
007Ch				
007Dh				
007Eh				
007Fh				

SFR Information (2) ⁽¹⁾ Table 4.2

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.



Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h		DTOFNO	
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0091h 0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	UOCO	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UARTO Receive Buffer Register	UORB	XXh
00A01		OOKB	
			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh	1		XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
	UADTO Special Made Desister 5	LIDOMDE	0.01
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
0 0 D C .	UART2 Special Mode Register 4	U2SMR4	00h
00BCh			
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
	UART2 Special Mode Register 3 UART2 Special Mode Register 2 UART2 Special Mode Register	U2SMR3 U2SMR2 U2SMR	000X0X0Xb X000000b X000000b

Table 4.3SFR Information (3) (1)

X: Undefined

Note:



Address Register Symbol ADR Register 00Cinh ADR Register 1 ADD 00000XAb 00Cinh ADR Register 1 ADD 00000XAb 00Cinh ADR Register 2 ADD 00000XAb 00Cinh ADR Register 3 00000XAb 00000XAb 00Cinh ADR Register 3 ADD 00000XAb 00Cinh ADR Register 3 ADD 00000XAb 00Cinh ADR Register 3 ADD 00000XAb 00Cinh ADR Register 5 ADS Xh 00Cinh ADR Register 6 ADF Xh 00Cinh ADR Register 7 AD7 00000XAb 00Cinh ADR Register 7 AD7 <td< th=""><th>Address</th><th>Bogistor</th><th>Symbol</th><th>After Reset</th></td<>	Address	Bogistor	Symbol	After Reset
00C1h AD Register 1 AD1 XNh 00C3h AD Register 2 AD2 XNh 00C3h AD Register 2 AD2 00000Xb 00C3h AD Register 3 AD3 XNh 00C3h AD Register 3 AD3 XNh 00C3h AD Register 4 AD4 XNh 00C3h AD Register 5 AD5 XNh 00C3h AD Register 6 000000Xb 00000Xb 00C5h AD Register 7 AD7 XNh 00C6h AD Register 7 00000Xb 00000Xb 00C5h AD Register 7 AD7 XNh 000000 - - - 000000 - - - 000000 - - - 000000 - - - 000000 - - - 000000 - - - 000000 - - - 000000 -				
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00CAT AD Register 2 ODOCOMA 20000XXb 00CEh AD Register 3 AD3 XNn 00CEh AD Register 3 AD3 XNn 00CEh AD Register 4 AD4 XNn 00CEh AD Register 4 AD4 XNn 00CEh AD Register 5 AD5 XNn 00CEh AD Register 5 AD5 XNn 00CEh AD Register 6 AD6 COD000XXb 00CEh AD Register 7 AD7 COD00XXb 00CEh AD Register 7 AD7 COD000XXb 00CEh AD Register 7 AD7 COD00XXb 00CEh AD Register 7 AD7 COD00XXb 00CEh AD Register 1 AD7 COD00XB 00DFh AD Control Register 1 AD100D COD1 00DFh AD Control Register 1 ADC0N1 COD1 00DFh AD Control Register 1 ADC0N1 COD1 00DFh AD Control Register 1 ADC0N1 COD1 <				
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00CAR AD Register 5 ADS XXh 00CCR AD Register 6 ADG 00000Xb 00CCR AD Register 7 AD7 000000Xb 00CCR AD Register 7 000000Xb 000000Xb 00CDn - 000000Xb 000000Xb 00D0n - 000000Xb 000000Xb 00D01 - - 000000Xb 00D3R - - 000000Xb 00D3R - - - 00D3R - - - 00D3R - - - 00D3R AD Control Register ADICON1 00h 00D3R - - - 00D5R - - - 00D5R - - -	00C9h			000000XXb
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00CCh AD Register 6 AD6 XXh 00CCh AD7 XXh 00000Xb 00CFh AD7 XXh 00000Xb 00CFh AD7 00000Xb 00000Xb 00D7h - - 00000Xb 00D7h - - 000000Xb 00D7h - - 000000Xb 00D7h - - 000000Xb 00D7h AD Mode Register ADMOD 00h 00D7h AD Control Register 1 ADCONU 00h 00D7h - - - 00D7h		A/D Register 5	ADS	
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0002h 00000k 0000 0001h 0001h 0000 0002h 0001 0000 0002h 0000 000 0002h 000 000 0002h AD Mode Register ADMOD 0005h AD Control Register 0 ADCON0 00h 0002h AD Control Register 0 ADCON1 00h 0002h AD Control Register 1 ADCON1 00h 0002h AD Control Register 1 ADCON1 00h 0002h 000 00 0000 00h 0002h 000 00 000 00h 0002h 00 00 000 00h 0002h 00 00 00h 00h 0002h 00 00 00h 00h 0002h 00 00 00h 00h 0002h 00 00h 00h 00h 002Eh 001 P0 P0 Register P1 Xh	00CDh			00000XXb
0002h 00000k 0000 0001h 0001h 0000 0002h 0001 0000 0002h 0000 000 0002h 000 000 0002h AD Mode Register ADMOD 0005h AD Control Register 0 ADCON0 00h 0002h AD Control Register 0 ADCON1 00h 0002h AD Control Register 1 ADCON1 00h 0002h AD Control Register 1 ADCON1 00h 0002h 000 00 0000 00h 0002h 000 00 000 00h 0002h 00 00 000 00h 0002h 00 00 00h 00h 0002h 00 00 00h 00h 0002h 00 00 00h 00h 0002h 00 00h 00h 00h 002Eh 001 P0 P0 Register P1 Xh	00CEh	A/D Register 7	AD7	XXh
0000h		······································		
0001h				0000000000
0002h 000 0003h AD Mode Register ADMOD 00h 0005h AD Input Select Register ADINSEL 1100000b 0005h AD Control Register 0 ADCON0 00h 0005h AD Control Register 1 ADCON1 00h 0005h Port PR Register P1 AD ADCON1 0005h Port PD Register P1 PO XXh 005Eh Port P1 Register P1 PO1 00h 005Eh Port P2 Register P2 Xh Xh 005Eh Port P3 Direction Register P3 P3 Xh 005Eh Port P3 Register P4 P4 Xh <td></td> <td></td> <td></td> <td></td>				
0003h AD Mode Register ADMOD Ooh 0005h AD Input Salect Register ADINSEL 11000000b 0015h AD Control Register 0 ADCON Ooh 0015h AD Control Register 1 ADCON1 Ooh 00107h AD Control Register 1 ADCON1 Ooh 0005h Image: ADD Control Register 1 Image: ADD Control Register 1 Image: ADD Control Register 1 0005h Port PD Register P1 XXh Image: ADD Control Register 1 0005h Port P0 Register P1 XXh Image: ADD Control Register 1 P1 XXh 0055h Port P1 Register P2 XXh Image: ADD Control Register 1 P2 Xh 0055h Port P2 Register P3 XXh Image: ADD Control Register 1 P2 Xh 0055h Port P3 Register				
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00D4h AD Input Select Register ADIOD 00h 00D5h AD Control Register 0 ADCON0 00h 00D5h AD Control Register 0 ADCON1 00h 00D5h AD Control Register 1 ADCON1 00h 00D5h	00D3h			
0005h A/D Iontril Register A/D Control Register 0 A/D Control Register 1 00h 0005h A/D Control Register 1 A/D Control Register 1 00h 00h 0005h		A/D Mode Register	ADMOD	00h
0006h A/D Control Register 0 ADCON 00h 0007h A/D Control Register 1 ADCON1 00h 0008h		A/D Input Select Register		
0007h A/D Control Register 1 00h 0008h				
0008h				
0009h		A/D Control Register 1	ADCON1	00h
000Ah	00D8h			
000Ah	00D9h			
000Bh			1	
00DCh				
00DDh				
00DEh 000Eh Port P0 Register P0 XXh 00E1h Port P1 Register P1 XXh 00E2h Port P0 Direction Register PD0 00h 00E3h Port P1 Direction Register PD1 00h 00E3h Port P2 Register P2 XXh 00E5h Port P2 Register P3 XXh 00E6h Port P2 Register P3 XXh 00E6h Port P2 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P4 Register P3 00h 00E8h Port P4 Register P4 XXh 00E9h 00E6h 00E6h 00E6h 00E6h </td <td></td> <td></td> <td></td> <td></td>				
00DFh Pott P1 Register P0 XXh 00E1h Pott P1 Register P1 XXh 00E2h Pott P0 Direction Register PD0 00h 00E3h Pott P1 Direction Register PD1 00h 00E3h Pott P2 Register P2 XXh 00E5h Pott P3 Register P2 XXh 00E5h Pott P3 Register P2 00h 00E5h Pott P4 Register PD2 00h 00E5h Pott P4 Register P4 XXh 00E6h P0t P4 Direction Register PD4 00h 00E5h P0t P4 Direction Register PD4 00h 00E6h P0t P4 Direction Register PD4 00h 00E6h P0t P4 Direction Register PD4 0h 00E6h P00E6h P01 P01	00DDh			
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ODE2h Port PD Direction Register PD0 O0h ODE3h Port P1 Direction Register PD1 O0h ODE4h Port P2 Register P2 XXh ODE5h Port P3 Register P3 XXh ODE6h Port P2 Direction Register PD2 O0h ODE7h Port P3 Direction Register PD3 00h ODE8h Port P4 Register PD3 00h ODE8h Port P4 Register PD3 00h ODE8h Port P4 Register PD4 XXh ODE8h Port P4 Direction Register PD4 00h ODE6h O0E2h O0E7h O0E7h O0F1h				
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O0E4h Port P2 Register P2 XXh 00E5h Port P3 Register P3 XXh 00E6h Port P3 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E8h Port P4 Register P4 XXh 00E8h Port P4 Direction Register PD4 00h 00E8h Port P4 Direction Register PD4 00F 00F7h				
00E4h Port P2 Register P2 XXh 00E5h Port P3 Register P3 XXh 00E6h Port P3 Direction Register PD2 00h 00E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h 00E6h Port P4 Direction Register PD4 00h 00E8h Port P4 Direction Register PD4 00h 00E6h 00E7h 00E7h <td>00E3h</td> <td>Port P1 Direction Register</td> <td>PD1</td> <td>00h</td>	00E3h	Port P1 Direction Register	PD1	00h
00E5h Port P3 Register P3 XXh 00E6h Port P2 Direction Register PD2 00h 00E7h Port P4 Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h PD4 00h 00h 00E8h Port P4 Direction Register P4 00h 00E8h PD4 00h 00h 00E6h PD4 00h 00h 00E6h PD4 00h 00E 00E6h PD4 PD4 00h 00E7h PD4 PD4 PD4 00E7h PD4 PD4 PD4 00E7h PD4 PD4 PD4 00F7h PD4 PD4 PD4 00F7h PD4 PD4 PD4 00F7h PD4 PD4 PD4 00F6h PD4 PD4 PD4 00F7h PD4 PD4 PD4 00F7h PD4 PD4 <td>00E4h</td> <td></td> <td>P2</td> <td>XXh</td>	00E4h		P2	XXh
ODE6h Port P2 Direction Register PD2 O0h 00E7h Port P3 Direction Register PD3 O0h 00E8h Port P4 Register P4 XXh 00E9h				
O0E7h Port P3 Direction Register PD3 00h 00E8h Port P4 Register P4 XXh 00E9h		Port D2 Direction Degister		
O0E8h Port P4 Register P4 XXh O0E9h				
O0E9h				00h
00E9h 00EAh Port P4 Direction Register PD4 00h 00EBh 00ECh 00EFh 00EFh 00EFh	00E8h	Port P4 Register	P4	XXh
O0EAh Port P4 Direction Register PD4 00h 00EBh	00E9h			
00EBh		Port P4 Direction Register	PD4	00h
00ECh				
00EDh				ļ
O0Eh Image: constraint of the second se				
O0EFh Image: Constraint of the system Image: Consthe system I				
O0EFh Image: Constraint of the system Image: Consthe system I	00EEh			
00F0h			1	
00F1h 00F2h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F0h 00F1h				+
00F2h 00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00F8h 00FBh 00FCh 00FDh 00FFh				<u> </u>
00F3h 00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00F8h 00F8h 00F8h 00FBh 00FCh 00FDh 00FFh				
00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00F8h 00F9h 00F8h 00FBh 00FCh 00FDh 00FFh	00F2h			
00F4h 00F5h 00F6h 00F7h 00F8h 00F9h 00F8h 00F9h 00F8h 00FBh 00FCh 00FDh 00FFh	00F3h			
00F5h Image: mail of the second				1
00F6h 00F7h 00F8h 00F9h 00F9h 00FAh 00FBh 00FCh 00FDh 00FEh 00FFh			1	+
00F7h			+	
00F8h				
00F9h				
00F9h	00F8h			
00FAh			1	1
00FBh				+
00FCh			+	<u> </u>
00FDh				
00FEh 00FFh 00FFh				
00FEh 00FFh 00FFh	00FDh			
00FFh				1
				+
				1

Table 4.4SFR Information (4) (1)

X: Undefined

Note:

Address	Pogiator	Symbol	After Reset
02C0h	Register SCU Control Register 0	SCUCRO	00h
02C0h	SCU Mode Register	SCUMR	00h
02C2h	SCU Timing Control Register 0	SCTCR0	00000011b
			0000001b
02C3h	SCU Timing Control Register 1	SCTCR1	
02C4h	SCU Timing Control Register 2	SCTCR2	00010000b
02C5h	SCU Timing Control Register 3	SCTCR3	00h
02C6h	SCU Channel Control Register	SCHCR	00h
02C7h	SCU Channel Control Counter	SCUCHC	00h
02C8h	SCU Flag Register	SCUFR	00h
02C9h	SCU Status Counter	SCUSTC	00h
02CAh	SCU Secondary Counter Set Register	SCSCSR	00000111b
02CBh	SCU Secondary Counter	SCUSCC	00000111b
02CCh			
02CDh			
02CEh	SCU Destination Address Register	SCUDAR	00h
02CEh	SCO Destiliation Address Register	SCODAR	
		0011000	00001100b
02D0h	SCU Data Buffer Register	SCUDBR	00h
02D1h			00h
02D2h	SCU Primary Counter	SCUPRC	00h
02D3h			00h
02D4h			
02D5h			
02D6h			
02D7h			
02D7h 02D8h			
02D8h			
02DAh			
02DBh			
02DCh	Touch Sensor Input Enable Register 0	TSIER0	00h
02DDh	Touch Sensor Input Enable Register 1	TSIER1	00h
02DEh	Touch Sensor Input Enable Register 2	TSIER2	00h
02DFh			
:			
2C00h	DTC Transfer Vector Area		XXh
2C00h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area	1	XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C3111 2C40h	DTC Control Data 0	DTCD0	XXh
		01000	
2C41h	4		XXh
2C42h	4		XXh
2C43h	1		XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h	1		XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h		2.001	XXh
2C490 2C4Ah	4		
	4		XXh
			XXh
2C4Bh			XXh
2C4Bh 2C4Ch			
2C4Bh 2C4Ch 2C4Dh			XXh
2C4Bh 2C4Ch			

Table 4.9SFR Information (9) (1)

Note:

Address	Desister	Ourseland	After Deset
Address	Register	Symbol	After Reset
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h	-		XXh
2C98h	DTC Control Data 11	DTCD11	XXh
		DICDII	
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h	-		XXh
2CA3h	-		XXh
	-		
2CA4h	4		XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh	1		XXh
2CABh	-		XXh
2CACh	-		XXh
2CADh	-		XXh
2CADh 2CAEh	-		XXh
2CAFh			XXh
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h	1		XXh
2CB6h			XXh
2CB7h	-		XXh
	DTO Ocustual Data 45	DTOD45	
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh	4		XXh
2CBBh			XXh
2CBCh			XXh
2CBDh]		XXh
2CBEh	1		XXh
2CBFh	1		XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2000h		510510	XXh
2CC2h	4		XXh
2CC2h 2CC3h	4		
	4		XXh
2CC4h	4		XXh
2CC5h	1		XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh	1		XXh
2CCAn 2CCBh	4		XXh
	4		
2CCCh	4		XXh
2CCDh	4		XXh
2CCEh	1		XXh
2CCFh			XXh
Y: Undofined			

Table 4.11SFR Information (11) (1)

X: Undefined Note:



Symbol	Parameter	Conditions	Standard			Unit
Symbol	Farameter	Conditions	Min.	Тур.	Max.	Unit
_	Program/erase endurance (2)		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μS
—	Block erase time		—	0.3	—	S
td(SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μS
_	Time from suspend until erase restart		_	—	30 + CPU clock × 1 cycle	μS
td(CMDRST -READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	μS
	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0		60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	_	—	year

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Notes:

1. Vcc = 2.7 V to 5.5 V at Topr = 0° C to 60° C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.



Symbol		Parameter	Condition		Standard		Unit	
Symbol		Falameter			Min.	Тур.	Max.	Unit
Vон	Output "H"	Other than XOUT	Drive capacity High Vcc = $5 V$	Іон = -20 mA	Vcc - 2.0	—	Vcc	V
	voltage		Drive capacity Low Vcc = $5 V$	Iон = -5 mA	Vcc - 2.0	_	Vcc	V
		XOUT	Vcc = 5 V	Іон = -200 μА	1.0	—	Vcc	V
Vol	Output "L"	Other than XOUT	Drive capacity High Vcc = $5 V$	IoL = 20 mA	_	_	2.0	V
	voltage		Drive capacity Low Vcc = 5 V	IoL = 5 mA	—	—	2.0	V
		XOUT	Vcc = 5 V	IoL = 200 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2			0.1	1.2		>
		RESET			0.1	1.2	—	V
Ін	Input "H" cu	rrent	VI = 5 V, Vcc = 5.0 V				5.0	μA
lı∟	Input "L" cu	rrent	VI = 0 V, Vcc = 5.0 V		_	_	-5.0	μA
Rpullup	Pull-up resis	stance	VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
Rfxin	Feedback resistance	XIN			—	0.3	_	MΩ
Vram	RAM hold v	oltage	During stop mode		1.8	—	—	V

Table 5.13 Electrical Characteristics (1) [4.2 V \leq Vcc \leq 5.5 V]

Note:

1. 4.2 V \leq Vcc \leq 5.5 V at Topr = -20°C to 85°C (N version), f(XIN) = 20 MHz, unless otherwise specified.



Table 5.17Serial Interface

Symbol	Parameter	Standard		Link
Symbol	Parameter	Min.	Max.	Unit
tc(CK)	CLKi input cycle time	200	—	ns
tW(CKH)	CLKi input "H" width	100	—	ns
tW(CKL)	CLKi input "L" width	100	—	ns
td(C-Q)	TXDi output delay time	—	50	ns
th(C-Q)	TXDi hold time	0	—	ns
tsu(D-C)	RXDi input setup time	50	—	ns
th(C-D)	RXDi input hold time	90	_	ns

i = 0, 2

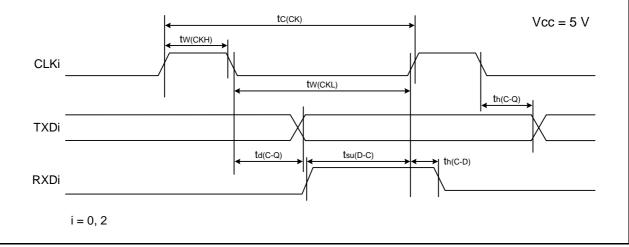


Figure 5.6 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18 External Interrupt INTi (i = 0 to 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol Parameter		Standard		Unit
Symbol	Falameter	Min.	Max.	Unit
tw(INH)	INTi input "H" width, Kli input "H" width	250 ⁽¹⁾	_	ns
tw(INL)	INTi input "L" width, Kli input "L" width	250 ⁽²⁾		ns

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.



Figure 5.7 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 5 V

Table 5		Characteristics (4) [2.7 V \leq Vcc $<$ 3.3 V] $^{\circ}$ C to 85 $^{\circ}$ C (N version), unless otherwise specified.)

0		Ì	0		Standar	d	
Symbol	Parameter		Condition	Min.	Тур.	Max.	Uni
сс	Power supply current (Vcc = 2.7 V to 3.3 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.5	10	mA
	other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	3		mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4		mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRD = MSTTRC = 1	_	1		mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	3.5		μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2	5.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	5	_	μA



Table 5.23Serial Interface

Symbol	Parameter	Stan	L Locit	
Symbol	Parameter	Min.	Max.	Unit
tc(CK)	CLKi input cycle time	300	—	ns
tW(CKH)	CLKi input "H" width	150	—	ns
tW(CKL)	CLKi Input "L" width	150	—	ns
td(C-Q)	TXDi output delay time - 80			
th(C-Q)	TXDi hold time 0 —			
tsu(D-C)	RXDi input setup time		—	ns
th(C-D)	RXDi input hold time 90 —			

i = 0, 2

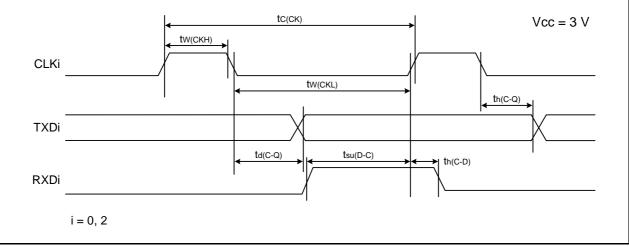


Figure 5.10 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.24 External Interrupt INTi (i = 0 to 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard		
Symbol	Falameter	Min.	Max.	Unit	
tw(INH)	INTi input "H" width, Kli input "H" width	380 (1)	_	ns	
tw(INL)	INTi input "L" width, Kli input "L" width	380 (2)	1	ns	

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

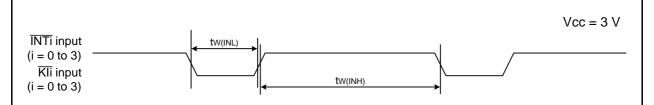


Figure 5.11 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 3 V

Symbol	Parameter		Condition			Standard		Unit
Symbol		Falameter	Min.		Min.	Тур.	Max.	Unit
Vон	Output "H"	Other than XOUT	Drive capacity High	Іон = –2 mA	Vcc - 0.5	_	Vcc	V
	voltage		Drive capacity Low	Iон = -1 mA	Vcc - 0.5	_	Vcc	V
		XOUT		Іон = –200 μА	1.0	_	Vcc	V
Vol	Output "L"	Other than XOUT	Drive capacity High	IOL = 2 mA	_	_	0.5	V
	voltage		Drive capacity Low	IoL = 1 mA	—	_	0.5	V
		XOUT		IoL = 200 μA	—	_	0.5	V
VT+-VT-	Hysteresis INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2		0.05	0.20		V		
		RESET			0.05	0.20	—	V
Ін	Input "H" current		VI = 2.2 V, Vcc = 2.2 V		—		4.0	μA
l∟	Input "L" current		VI = 0 V, Vcc = 2.2 V		_	_	-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 V		70	140	300	kΩ
Rfxin	Feedback resistance	XIN			—	0.3	_	MΩ
VRAM	RAM hold v	oltage	During stop mode		1.8	_	—	V

Table 5.25	Electrical Characteristics (5) [1.8 V \leq Vcc $<$ 2.7 V]
------------	---

Note:

1. 1.8 V \leq Vcc < 2.7 V at Topr = -20°C to 85°C (N version), f(XIN) = 5 MHz, unless otherwise specified.



Timing requirements (Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.27 External Clock Input (XOUT)

Symbol	Parameter		Standard		
Symbol	Falanielei	Min.	Max.	Unit	
tc(XOUT)	XOUT input cycle time	200	_	ns	
twh(xout)	XOUT input "H" width	90	—	ns	
twl(xout)	XOUT input "L" width	90	_	ns	

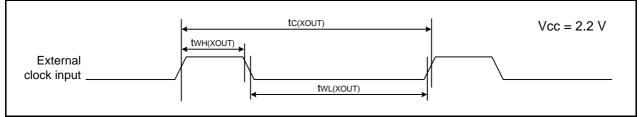


Figure 5.12 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.28 TRAIO Input

Symbol	Parameter	Stan	Unit	
Symbol		Min.	Max.	Unit
tc(TRAIO)	TRAIO input cycle time	500	_	ns
twh(traio)	TRAIO input "H" width	200	_	ns
twl(traio)	TRAIO input "L" width	200	_	ns

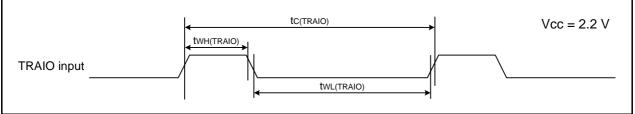


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 2.2 V



Table 5.29Serial Interface

Symbol	Parameter	Stan	Link	
Symbol	Parameter	Min.	Max.	Unit
tc(CK)	CLKi input cycle time	800	—	ns
tW(CKH)	CLKi input "H" width	400	—	ns
tW(CKL)	CLKi input "L" width	400	—	ns
td(C-Q)	TXDi output delay time	200	ns	
th(C-Q)	TXDi hold time	0	—	ns
tsu(D-C)	RXDi input setup time		—	ns
th(C-D)	RXDi input hold time 90 —			

i = 0, 2

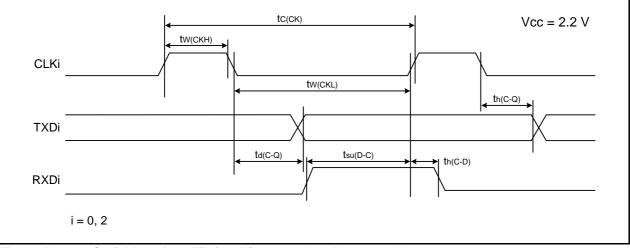


Figure 5.14 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.30 External Interrupt \overline{INTi} (i = 0 to 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)

Symbol	Parameter		Standard		
Symbol	Falameter	Min.	Max.	Unit	
tw(INH)	INTi input "H" width, Kli input "H" width	1000 (1)	_	ns	
tw(INL)	NTi input "L" width, Kli input "L" width 1000 ⁽²⁾			ns	

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

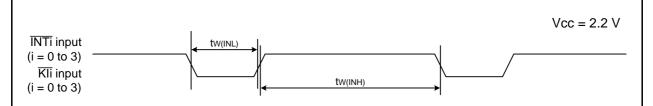


Figure 5.15 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 2.2 V

REVISION HISTORY

R8C/3JT Group Datasheet

Rev.	Date		Description
Nev.	Dale	Page	Summary
0.10	Jul 12, 2010	_	First Edition issued
1.00	Apr 26, 2011	All pages	"Preliminary", "Under development", and "D version" deleted
		3	Table 1.2 revised, Note 1 deleted
		4	Table 1.3 and Figure 1.1 revised
		12	3.1 "The internal ROM with address 0FFFFh." deleted
		26	Table 5.1 revised
		27	Note 1 revised
		29	Note 1 revised
		31	Table 5.5, Note 1, Note 7 revised, and Note 8 added
		32	Note 1 of Table 5.6 and Table 5.7 revised
		33	Note 1 of Table 5.8 and Table 5.9 revised
		34	Table 5.10, Note 1 of Table 5.10 and Table 5.11 revised
		35	Note 1 revised
		36	Table 5.14 revised
		39	Note 1 revised
		40	Table 5.20 revised
		43	Note 1 revised
		44	Table 5.26 revised

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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