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What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	31
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-XFQFN Exposed Pad
Supplier Device Package	40-HXQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213j5tnnp-w4

1.2 Product List

Table 1.3 lists Product List for R8C/3JT Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3JT Group.

Table 1.3   Product List for R8C/3JT Group   **Current of Apr 2011**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213J4TNNP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PXQN0040LA-A	N version
R5F213J5TNNP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PXQN0040LA-A	
R5F213J6TNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PXQN0040LA-A	

Part No. R 5 F 21 3J 6 T N NP

Package type:
    NP: PXQN0040LA-A (0.4 mm pin-pitch, 5 mm square body)

Classification
    N: Operating ambient temperature −20°C to 85°C

ROM capacity
    4: 16 KB
    5: 24 KB
    6: 32 KB

R8C/3JT Group

R8C/3x Series

Memory type
    F: Flash memory

Renesas MCU
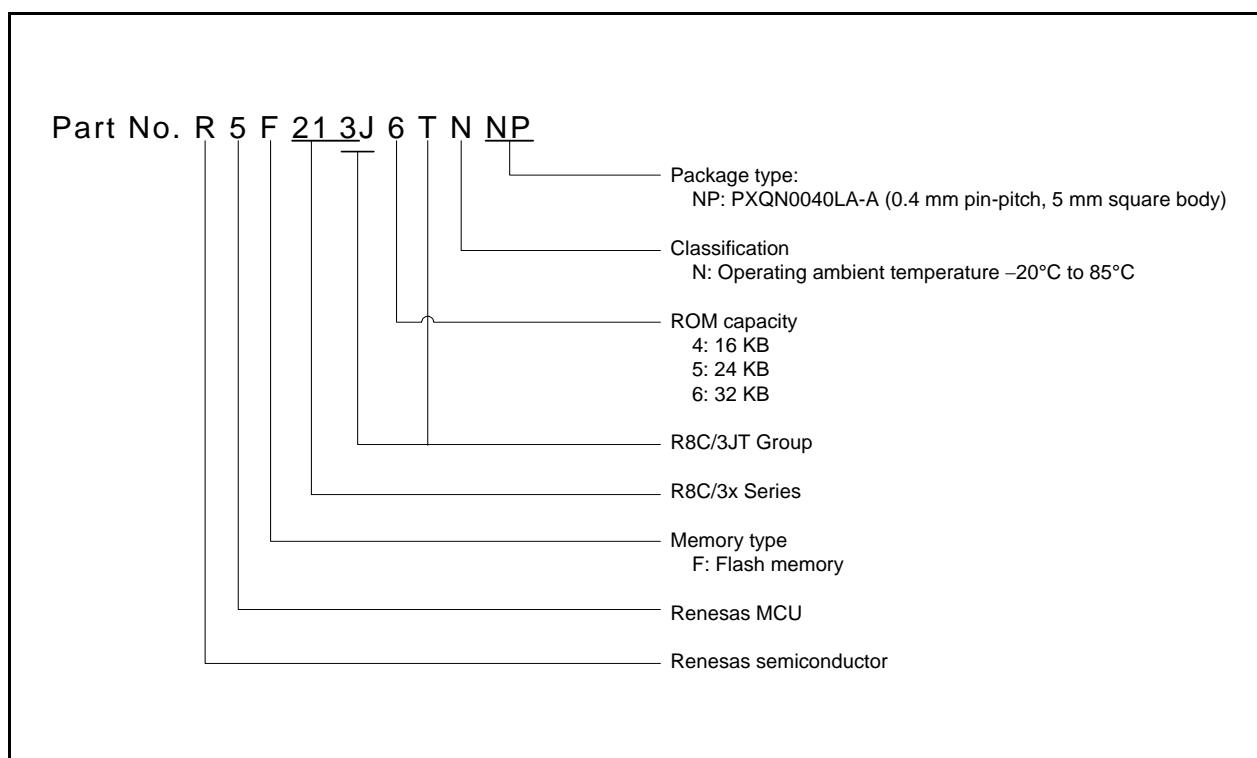
Renesas semiconductor

Figure 1.1   Part Number, Memory Size, and Package of R8C/3JT Group

Table 1.4   Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules				
			Interrupt	Timer	Serial Interface	A/D Converter	Sensor Control Unit
1		P4_2				VREF	
2	MODE						
3	$\overline{\text{RESET}}$						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC/AVCC						
8		P3_7	$(\overline{\text{INT3}})$	TRAO/ (TRCCLK)	(RXD2/SCL2/ TXD2/SDA2)		
9		P3_5	$(\overline{\text{INT1}})$	TRAIO/ (TRCIOD)	(CLK2)		
11		P3_4	$\overline{\text{INT2}}$	(TRCIOC)	(RXD2/SCL2/ TXD2/SDA2)		
12		P3_3	$\overline{\text{INT3}}$	TRBO/ (TRCCLK)	$(\overline{\text{CTS2}}/\overline{\text{RTS2}})$		$\overline{\text{SCUTRG}}$
13		P2_6					CH21
14		P2_5					CH20
15		P2_4					CH19
16		P2_3					CH18
17		P2_2		(TRCIOD)	(RXD2/TXD2/ SCL2/SDA2)		CH17
18		P2_1		(TRCIOC)	(CLK2)		CH16
19		P2_0	$(\overline{\text{INT1}})$	(TRCIOB)	(RXD2/TXD2/ SCL2/SDA2)		CH15
21		P3_1		TRBO/ (TRCTRG/ TRCIOA)	$(\overline{\text{CTS2}}/\overline{\text{RTS2}})$		CH14
22		P4_5	$\overline{\text{INT0}}$		(RXD2/SCL2)	$\overline{\text{ADTRG}}$	CH13
23		P1_7	$\overline{\text{INT1}}$	(TRAIO)			CH12
24		P1_6			(CLK0)		CH11
25		P1_5	$(\overline{\text{INT1}})$	(TRAIO)	(RXD0)		CH10
26		P1_4		(TRCCLK)	(TXD0)		CH9
27		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOC)		AN11	CH8
28		P1_2	$\overline{\text{KI2}}$	(TRCIOB)		AN10	CH7
29		P1_1	$\overline{\text{KI1}}$	(TRCIOA/ TRCTRG)		AN9	CH6
30		P1_0	$\overline{\text{KI0}}$	(TRCIOD)		AN8	CH5
32		P0_7		(TRCIOC)		AN0	CH4
33		P0_6		(TRCIOD)		AN1	CH3
34		P0_5		(TRCIOB)		AN2	CH2
35		P0_4		(TRCIOB)		AN3	CH1
36		P0_3		(TRCIOB)		AN4	CH0
37		P0_2		(TRCIOA/ TRCTRG)		AN5	CHxA
38		P0_1		(TRCIOA/ TRCTRG)		AN6	CHxB
39		P0_0		(TRCIOA/ TRCTRG)		AN7	CHxC

Note:
   1. Can be assigned to the pin in parentheses by a program.

2.1   Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2   Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3   Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4   Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5   Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6   User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7   Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8   Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1   Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2   Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3   Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4   Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5   Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6   Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

Table 4.11   SFR Information (11) [1]

Address	Register	Symbol	After Reset
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.12   SFR Information (12) [1]

Address	Register	Symbol	After Reset
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined

Note:
1. The blank areas are reserved and cannot be accessed by users.

5.   Electrical Characteristics

Table 5.1   Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		−0.3 to 6.5	V
V_I	Input voltage		−0.3 to Vcc + 0.3	V
V_O	Output voltage		−0.3 to Vcc + 0.3	V
P_d	Power dissipation	$-20°C \leq Topr \leq 85°C$	500	mW
T_{opr}	Operating ambient temperature		−20 to 85 (N version)	°C
T_{stg}	Storage temperature		−65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	—	5.5	V
Vss/AVss	Supply voltage					—	0	—	V
VIH	Input "H" voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
		External clock input (XOUT)				1.2	—	Vcc	V
VIL	Input "L" voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
		External clock input (XOUT)				0	—	0.4 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)				—	—	−160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)				—	—	−80	mA
IOH(peak)	Peak output "H" current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
IOH(avg)	Average output "H" current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
IOL(sum)	Peak sum output "L" current	Sum of all pins IOL(peak)				—	—	160	mA
IOL(sum)	Average sum output "L" current	Sum of all pins IOL(avg)				—	—	80	mA
IOL(peak)	Peak output "L" current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
IOL(avg)	Average output "L" current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
fOCO40M	When used as the count source for timer RC [3]				2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V at Topr = −20°C to 85°C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of Vcc = 2.7 V to 5.5 V.

Table 5.3   A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±3	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVcc = 5.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.3 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 3.0 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
			Vref = AVcc = 2.2 V	AN0 to AN7 input AN8 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V $\leq$ Vref = AVcc $\leq$ 5.5 V [2]		2	—	20	MHz
			3.2 V $\leq$ Vref = AVcc $\leq$ 5.5 V [2]		2	—	16	MHz
			2.7 V $\leq$ Vref = AVcc $\leq$ 5.5 V [2]		2	—	10	MHz
			2.2 V $\leq$ Vref = AVcc $\leq$ 5.5 V [2]		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
t_{CONV}	Conversion time	10-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	ms
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.75	—	—	μs
I_{Vref}	Vref current		Vcc = 5.0 V, XIN = f1 = ϕAD = 20 MHz		—	45	—	μA
V_{ref}	Reference voltage				2.2	—	AVcc	V
V_{IA}	Analog input voltage [3]				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz $\leq$ ϕAD $\leq$ 4 MHz		1.19	1.34	1.49	V

Notes:
1. Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V at Topr = −20°C to 85°C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 [2]		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 [2]		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 [2]		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 [2]		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time [4]	At the falling of Vcc from 5 V to (Vdet0_0 − 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
td(E-A)	Waiting time until voltage detection circuit operation starts [3]		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = −20°C to 85°C (N version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 [2]	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 [2]	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 [2]	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 [2]	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 [2]	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 [2]	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 [2]	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 [2]	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 [2]	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 [2]	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A [2]	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B [2]	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C [2]	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D [2]	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E [2]	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F [2]	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time [3]	At the falling of Vcc from 5 V to (Vdet1_0 − 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
td(E-A)	Waiting time until voltage detection circuit operation starts [4]		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = −20°C to 85°C (N version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.8   Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time [2]	At the falling of Vcc from 5 V to (Vdet2_0 − 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	µA
td(E-A)	Waiting time until voltage detection circuit operation starts [3]		—	—	100	µs

Notes:
  1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = −20°C to 85°C (N version).
  2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
  3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.9   Power-on Reset Circuit [2]

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	(Note 1)	0	—	50000	mV/msec

Notes:
  1. The measurement condition is Topr = −20°C to 85°C (N version), unless otherwise specified.
  2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.
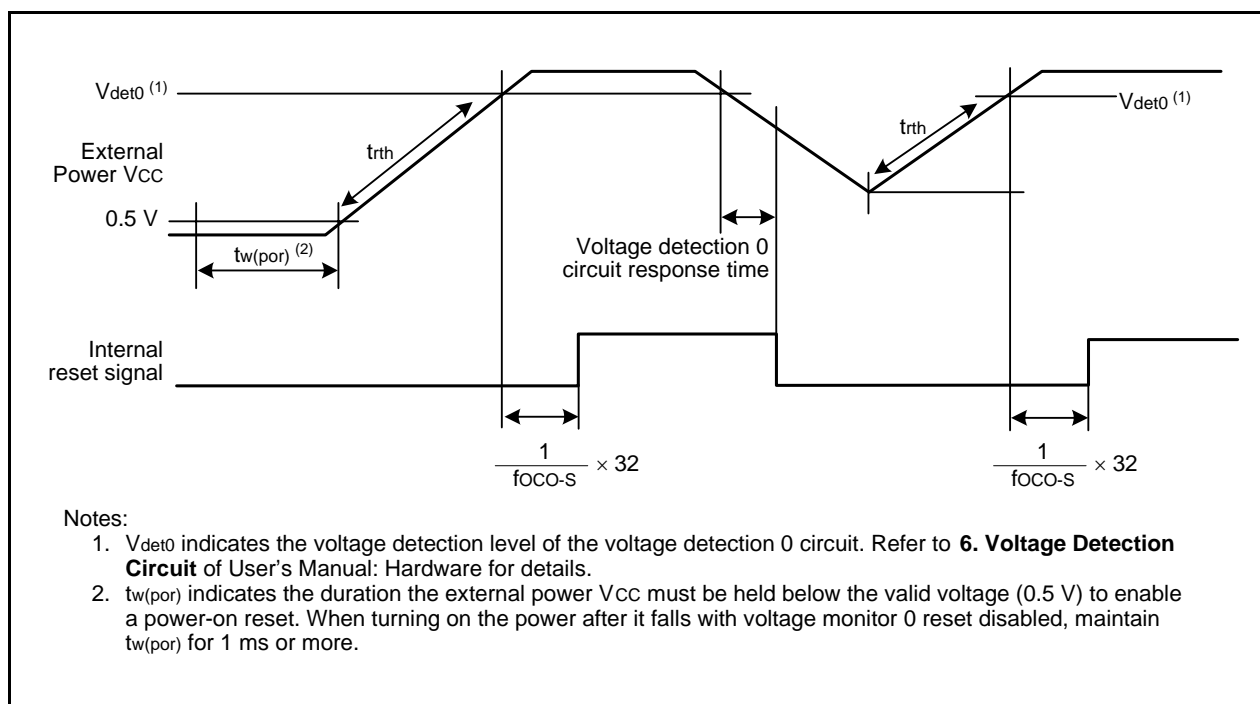
Figure 5.3   Power-on Reset Circuit Electrical Characteristics

Table 5.10   High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	37.8	40	42.6	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register [2]	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	34.836	36.864	39.261	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	30.24	32	34.08	MHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	0.5	3	ms
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	400	—	μA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = −20°C to 85°C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.11   Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	μs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	2	—	μA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = −20°C to 85°C (N version), unless otherwise specified.

Table 5.12   Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on [2]		—	—	2000	μs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.13   Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard Min.	Standard Typ.	Standard Max.	Unit
VOH	Output "H" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOH = −20 mA	Vcc − 2.0	—	Vcc	V
			Drive capacity Low Vcc = 5 V	IOH = −5 mA	Vcc − 2.0	—	Vcc	V
		XOUT	Vcc = 5 V	IOH = −200 µA	1.0	—	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High Vcc = 5 V	IOL = 20 mA	—	—	2.0	V
			Drive capacity Low Vcc = 5 V	IOL = 5 mA	—	—	2.0	V
		XOUT	Vcc = 5 V	IOL = 200 µA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2			0.1	1.2	—	V
		RESET			0.1	1.2	—	V
IIH	Input "H" current		VI = 5 V, Vcc = 5.0 V		—	—	5.0	µA
IIL	Input "L" current		VI = 0 V, Vcc = 5.0 V		—	—	−5.0	µA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			—	0.3	—	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
   1. 4.2 V ≤ Vcc ≤ 5.5 V at Topr = −20°C to 85°C (N version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C)

Table 5.15   External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	—	ns
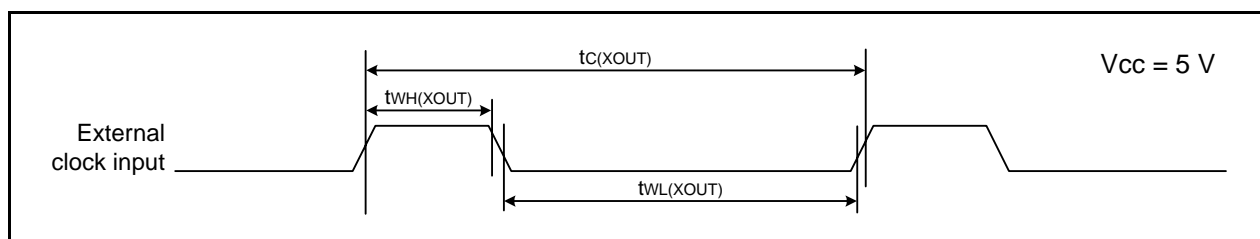
Figure 5.4   External Clock Input Timing Diagram when Vcc = 5 V

Table 5.16   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	—	ns
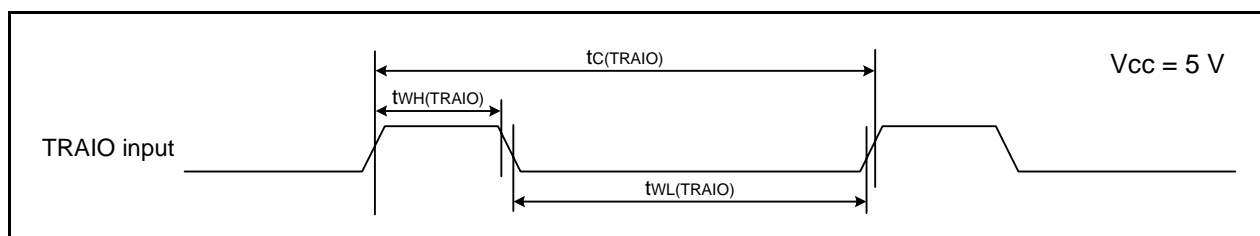
Figure 5.5   TRAIO Input Timing Diagram when Vcc = 5 V

Timing requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C)

Table 5.21   External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input "H" width	24	—	ns
$t_{WL(XOUT)}$	XOUT input "L" width	24	—	ns
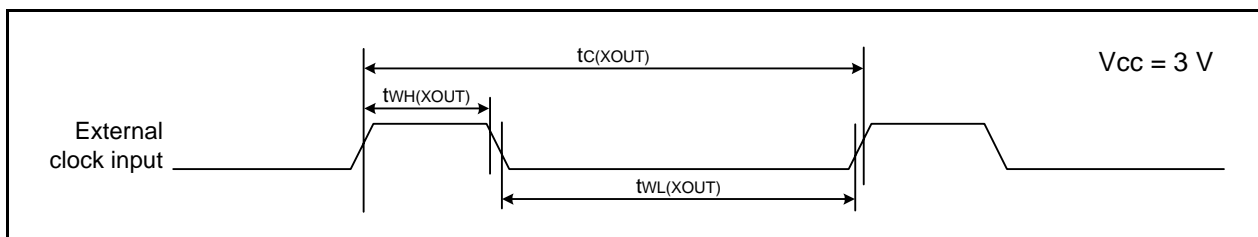
Figure 5.8   External Clock Input Timing Diagram when Vcc = 3 V

Table 5.22   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	120	—	ns
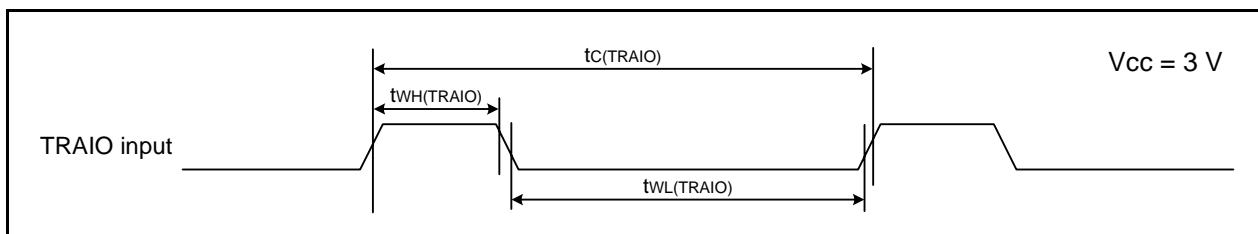
Figure 5.9   TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.23   Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input "H" width	150	—	ns
$t_{W(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0, 2
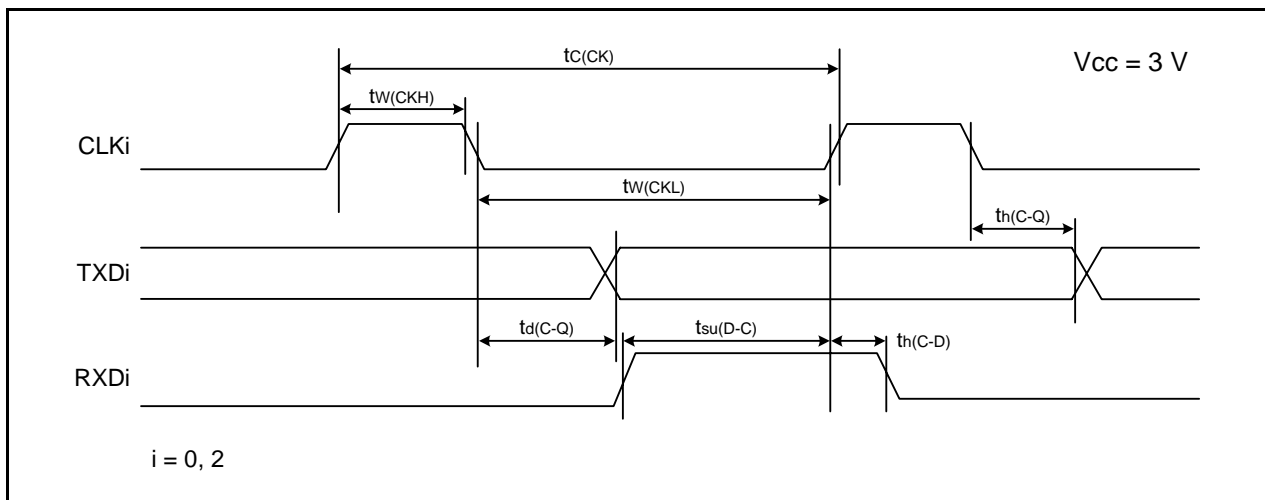
Figure 5.10   Serial Interface Timing Diagram when Vcc = 3 V

Table 5.24   External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input "H" width, $\overline{\text{KIi}}$ input "H" width	380 [1]	—	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input "L" width, $\overline{\text{KIi}}$ input "L" width	380 [2]	—	ns

Notes:
1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
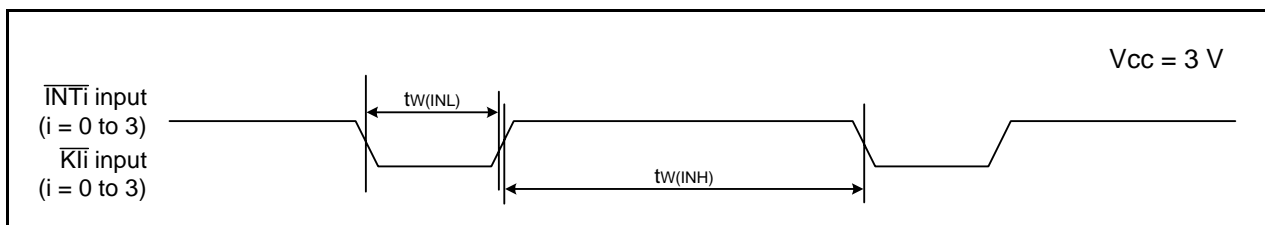
Figure 5.11   Input Timing for External Interrupt $\overline{\text{INTi}}$ and Key Input Interrupt $\overline{\text{KIi}}$ when Vcc = 3 V

Table 5.25   Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage	Other than XOUT	Drive capacity High	IOH = −2 mA	Vcc − 0.5	—	Vcc	V
			Drive capacity Low	IOH = −1 mA	Vcc − 0.5	—	Vcc	V
		XOUT		IOH = −200 μA	1.0	—	Vcc	V
VOL	Output "L" voltage	Other than XOUT	Drive capacity High	IOL = 2 mA	—	—	0.5	V
			Drive capacity Low	IOL = 1 mA	—	—	0.5	V
		XOUT		IOL = 200 μA	—	—	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2			0.05	0.20	—	V
		RESET			0.05	0.20	—	V
IIH	Input "H" current		VI = 2.2 V, Vcc = 2.2 V		—	—	4.0	μA
IIL	Input "L" current		VI = 0 V, Vcc = 2.2 V		—	—	−4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 V		70	140	300	kΩ
RfXIN	Feedback resistance	XIN			—	0.3	—	MΩ
VRAM	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 1.8 V ≤ Vcc < 2.7 V at Topr = −20°C to 85°C (N version), f(XIN) = 5 MHz, unless otherwise specified.

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.27   External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{C(XOUT)}$	XOUT input cycle time	200	—	ns
t$_{WH(XOUT)}$	XOUT input "H" width	90	—	ns
t$_{WL(XOUT)}$	XOUT input "L" width	90	—	ns
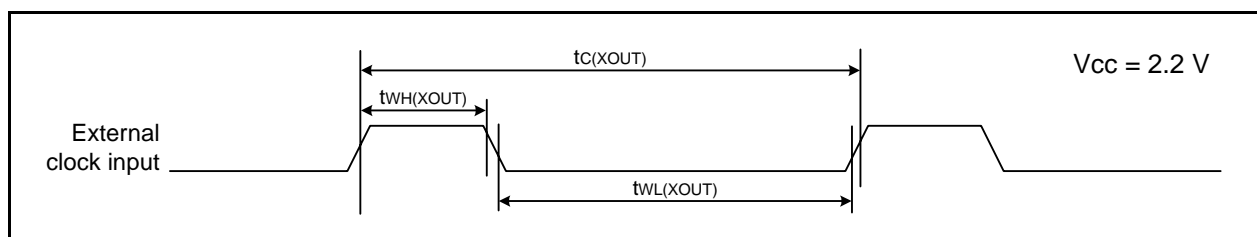
Figure 5.12   External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.28   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{C(TRAIO)}$	TRAIO input cycle time	500	—	ns
t$_{WH(TRAIO)}$	TRAIO input "H" width	200	—	ns
t$_{WL(TRAIO)}$	TRAIO input "L" width	200	—	ns
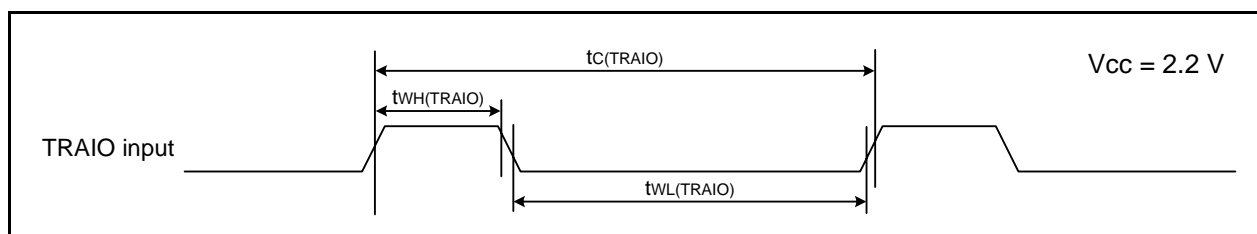
Figure 5.13   TRAIO Input Timing Diagram when Vcc = 2.2 V

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141