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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-XFQFN Exposed Pad
Supplier Device Package	40-HXQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213j6tnnp-yc

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R8C/3JT Group 1. Overview

Table 1.2 Specifications for R8C/3JT Group (2)

Item	Function	Specification		
Serial	UART0	Clock synchronous serial I/O/UART		
Interface	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), SSU mode, multiprocessor communication function		
LIN Module		Hardware LIN: 1 (timer RA, UART0)		
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode		
Sensor Control Unit		System CH x 3, electrostatic capacitive touch detection x 22		
Flash Memory		 Programming and erasure voltage: VCC = 2.7 V to 5.5 V Programming and erasure endurance: 10,000 times (data flash)		
Operating Free Voltage	quency/Supply	f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)		
Current Consu	mption	Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μ A (VCC = 3.0 V, wait mode) Typ. 2.0 μ A (VCC = 3.0 V, stop mode)		
Operating Amb	pient Temperature	-20 to 85°C (N version)		
Package		40-pin HXQFN Package code: PXQN0040LA-A		

R8C/3JT Group 1. Overview

1.2 Product List

Table 1.3 lists Product List for R8C/3JT Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3JT Group.

Table 1.3 Product List for R8C/3JT Group

Current of Apr 2011

Part No.	ROM C	apacity	RAM	Package Type	Remarks
rait NO.	Program ROM	Data flash	Capacity	Fackage Type	Remarks
R5F213J4TNNP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PXQN0040LA-A	N version
R5F213J5TNNP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PXQN0040LA-A	
R5F213J6TNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PXQN0040LA-A	

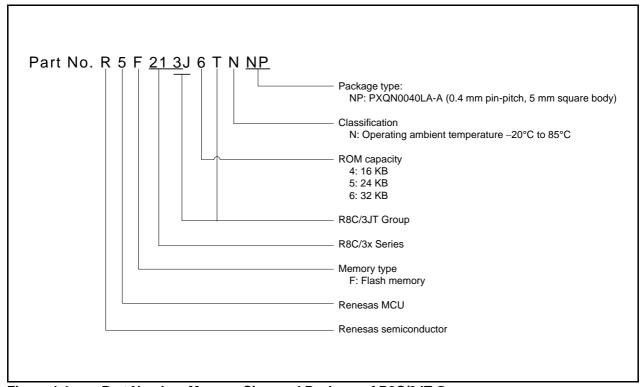


Figure 1.1 Part Number, Memory Size, and Package of R8C/3JT Group

R8C/3JT Group 1. Overview

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.

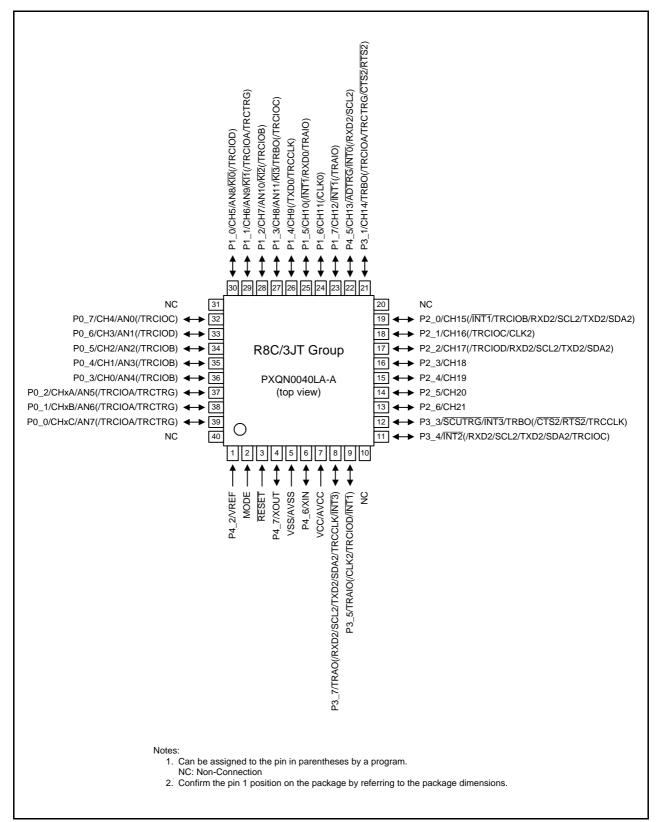


Figure 1.3 Pin Assignment (Top View)

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



R8C/3JT Group 3. Memory

3. Memory

3.1 **R8C/3JT Group**

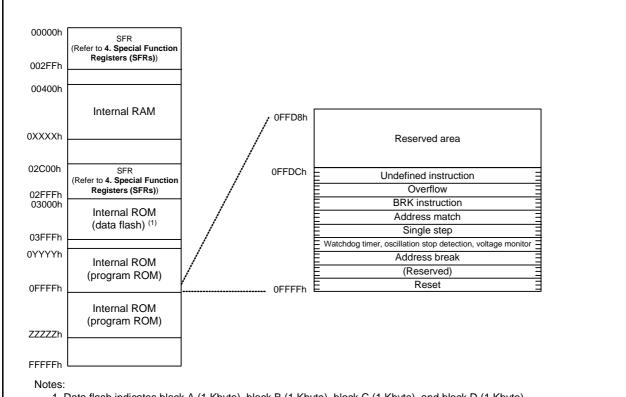
Figure 3.1 is a Memory Map of R8C/3JT Group. The R8C/3JT Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



- 1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
- 2. The blank areas are reserved and cannot be accessed by users.

Part Number		Internal ROM		Internal RAM		
Fait Number	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	
R5F213J4TNNP, R5F213J4TDNP	16 Kbytes	0C000h	-	1.5 Kbytes	009FFh	
R5F213J5TNNP, R5F213J5TDNP	24 Kbytes	0A000h	=	2 Kbytes	00BFFh	
R5F213J6TNNP, R5F213J6TDNP	32 Kbytes	08000h	_	2.5 Kbytes	00DFFh	

Figure 3.1 Memory Map of R8C/3JT Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h	Negistei	Symbol	Alter Neset
1			<u> </u>
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
		OCD	00000100b
000Ch	Oscillation Stop Detection Register		
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h	<u> </u>	†	
0017h		+	1
0018h			+
0019h			
0019II			
001Bh		0000	
001Ch	Count Source Protection Mode Register	CSPR	00h
			10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			1
0021h			+
0022h		+	+
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0023h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
	High-Speed On-Chip Oscillator Control Register 2	FRA2	•
0025h	High-Speed On-Only Oscillator Control Register 2		00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h		00005	
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh		1	1
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0030h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
003111 0032h	Voltago Monitor Orrodit Edgo Octob Nogister	¥ 0/ 10	0011
	Voltage Detact Register 1	V/CA1	00001000b
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾
			00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h	, , , , , , , , , , , , , , , , , , ,	1	
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4)
000011	- Stage methor of onotine control regions		
			4400V044h (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	1100X011b ⁽⁵⁾ 10001010b

X: Undefined

Notes:

- 1. The blank areas are reserved and cannot be accessed by users.
- 2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, Software reset, or watchdog timer reset does not affect this bit.
- 3. The CSPROINI bit in the OFS register is set to 0.
- 4. The LVDAS bit in the OFS register is set to 1.
- 5. The LVDAS bit in the OFS register is set to 0.



SFR Information (2) (1) Table 4.2

0038h Voltage Monitor 2 Circuit Control Register VYZC 100009169 0030h 0030h 1 100009169 0030h 0030h 1 1 0040h 0040h 1 1 0041h 1 1 1 1 0041h 1 1 1 1 0041h 1 1 1 1 1 0041h 1	Address	Register	Symbol	After Reset
003Ch 003Ch 003Ch 003Ph 003Ph 004Ph 004Ph Flash Memory Resdy Interrupt Control Register 004Ph 004Ph 005Ph 004Ph 005Ph 005Ph	003Ah			
0035b 0035h 0037h 0037h 0037h 004h 004h 004h 004b 004h 004b 004h 004h 004h 005h 004h 004h 004h 005h 005h 004h 004h 005h 005h 005h 005h 005h 005h 005h 005h 00				
0038th 0004th 005th 007th 007th	003Ch			
0037h 0040h 0041h Flash Memory Ready Interrupt Control Register FMRDYIC XXXXXX000b 0043h 0043h 0040h 0040h 0044h 0040h 0040h 0040h 0040h UART2 Transmit Interrupt Control Register SZRIC XXXXX000b 0040h Vall Transmit Interrupt Control Register ADIC XXXXX000b 0040h ADIC Convencio Interrupt Control Register SCRIC XXXXX000b 0055h ADIC Convencio Interrupt Control Register Intriol Control Register				
004th 0	003Eh			
004th Flash Memory Ready Interrupt Control Register FMRDVIC XXXXXX000b 004ah 004ah 004ah 004ah 004ah 005ah 005ah 005ah 004bh 004ah 004ah 005ah 004ah 004ah 004ah 004ah 004bh 004bh 004bh 004bh 004bh 004bh 004bh 004bh 004bh 004bh 004bh 004bh 005bh 005bh 005bh 005bh 005bh 005bh 005bh 005bh				
0042h 004h 004sh 004sh 005sh 005sh 005sh <td>0040h</td> <td></td> <td>EMBB///O</td> <td>N/////</td>	0040h		EMBB///O	N/////
0034sh 004sh 004sh 005sh 004sh 005sh 005sh 1872 interrupt Control Register 005sh 1873 interrupt Control		Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0044h 0046h 0046h 0046h 0047h Timer RC Interrupt Control Register 0048h 0048h 0048h 0048h 0048h 0048h 0048h UART2 Transmit Interrupt Control Register SZRIC XXXXXX00b 0046h UART2 Receive Interrupt Control Register SZRIC XXXXXX00b 0046h AD Corversion Interrupt Control Register ROPIC XXXXXX00b 0046h AD Corversion Interrupt Control Register ADIC XXXXXX00b 0046h AD Corversion Interrupt Control Register SORIC XXXXXX00b 0057h UARTO Transmit Interrupt Control Register SORIC XXXXXX00b 0053h INT2 Interrupt Control Register INT2IC XXXXXX00b 0055h INT2 Interrupt Control Register TRAIC XXXXXX00b 0057h Timer RA Interrupt Control Register TRAIC XXXXXX00b 0058h INT3 Interrupt Control Register INT3IC XXXXXX00b 0058h INT3 Interrupt Control Register INT3IC XXXXXX00b	0042h			
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004Dh Key Input Interrupt Control Register XUPIC XXXXX000b 004En 40 Conversion Interrupt Control Register ADIC XXXXX000b 005Ph 005Ph 005Ph 005Ph 005Ph 0052h 0052h 007Dh 005Ph 005Ph </td <td>004Bh</td> <td></td> <td>S2TIC</td> <td>XXXXX000b</td>	004Bh		S2TIC	XXXXX000b
004Eh 005Ph 005Ph 005Ph 0052h ADIC XXXXX000b 005Ph 0052h UART0 Transmit Interrupt Control Register SOTIC XXXXX000b 0052h 0052h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0053h 0053h UART0 Receive Interrupt Control Register SORIC XXXXX000b 0055h 0055h INT2 Interrupt Control Register INT2IC XX0XX000b 0055h Timer RA Interrupt Control Register TRBIC XXXXX000b 0055h INT3 Interrupt Control Register INT3IC XX0XX000b 0055h INT3 Interrupt Control Register INT3IC XX00X000b 0055h INT3 Interrupt Control Register INT0IC XX00X000b 0055h INT0 Interrupt Control Register INT0IC XX00X000b 0055h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXXX000b 0056h 0066h 0066h 0066h 0066h 0062h 0068h 0066h 0066h 0066h 0068h 0066h 0066h 0066h 0066h 0066h </td <td>004Ch</td> <td>UART2 Receive Interrupt Control Register</td> <td>S2RIC</td> <td></td>	004Ch	UART2 Receive Interrupt Control Register	S2RIC	
005Ph		Key Input Interrupt Control Register		
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Ossentration		INT2 Interrunt Control Register	INITOIC	XX00X000h
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0059h		Timer RB Interrupt Control Register	TRBIC	XXXXX000b
005Ah	0059h	INT1 Interrupt Control Register		
005Bh		INT3 Interrupt Control Register		
0050h INTO Interrupt Control Register INTOIC XX0X000b 0056h UART2 Bus Collision Detection Interrupt Control Register U2BCNIC XXXXX000b 0056h 0060h	005Bh			
Mart				
005Fh 0060h 0061h 0062h 0062h 0063h 0063h 0065h 0066h 0066h 0066h 0067h 0068h 0068		INT0 Interrupt Control Register		
0060h 0061h 0062h 0063h 0064h 0065h 0066h 0067h 0066h 0067h 0068h 0068h 0068h 0069h 0068h 0068h 0066h 0066		UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
0061h 0062h 0063h 0064h 0066h 0060h 0066h 0066				
0062h 0063h 0064h 0065h 0066h 0066h 0066h 0066h 0069h 0069h 0069h 0069h 0060h 0060				
0063h 0064h 0065h 0065h 0067h 0068h 0067h 0068h 0069h 0069h 006Ah Sensor Control Unit Interrupt Control Register SCUIC XXXXX000b 006Bh 006Ch 006Ch 006Eh 006Eh 006Fh 0070h 0070h 0071h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0075h 0076h 0076h 0078h 0078h 0078h 0078h 0078h 007Ch 007Dh 007Dh 007Dh 007Ch 007Dh 007Dh 007Dh				
0064h 0065h				
0065h 0066h 0067h 0068h 0069h 0068h 0069h 0068h 0060h Sensor Control Unit Interrupt Control Register 006Dh 006Dh 006Eh 006Fh 0070h 0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0077h 0078h 0079h 0078h 0078h 007Bh 007Ch 007Dh 007Dh 007Dh 007Dh 007Dh 007Dh				
0066h 0067h 0068h 0069h 006Ah Sensor Control Unit Interrupt Control Register SCUIC XXXXX000b 006Bh 006Ch 006Ch 006Ch 006Eh 006Fh 006Fh 0070h 0070h 0070h 0070h 0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b XXXXX000b 0074h 0074h 0074h 0074h 0075h 0076h 0077h 0078h 0078h <td></td> <td></td> <td></td> <td></td>				
0067h 0068h 0069h				
0068h 0069h 006Ah Sensor Control Unit Interrupt Control Register SCUIC XXXXX000b 006Bh 006Ch 009Dh 006Eh 006Eh 006Eh 006Eh 006Eh 0070h 0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b VCMP2IC XXXXXX000b VCMP2IC XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
0069h Sensor Control Unit Interrupt Control Register SCUIC XXXXX000b 006Bh 006Ch 006Dh 006Eh 006Eh 006Fh 006Fh 0070h 0070h 0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXXX000b 0074h 0075h 0076h 0077h 0078h 0078h 0078h 0078h 0078h 0078h 0078h 0077h 0				
006Ah Sensor Control Unit Interrupt Control Register SCUIC XXXXX000b 006Bh				+
006Bh 006Ch 006Dh 006Eh 006Fh 0070h 0071h 0072h 0073h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0077h 0078h 0079h 007Ah 0078h 007Ah 007Bh 007Ch 007Ch 007Dh 007Ch 007Dh 007Eh		Sensor Control Unit Interrupt Control Register	SCUIC	XXXXX000h
006Ch 006Dh 006Eh 006Fh 0070h 0070h 0071h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0076h 0077h 0078h 0079h 007Ah 007Bh 007Ch 007Ch 007Ch 007Dh 007Eh 007Eh 007Eh				
006Dh 006Eh 006Fh 0070h 0071h 0072h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0077h 0078h 0079h 007Ah 007Ah 007Ch 007Ch 007Dh 007Dh 007Dh 007Dh				
006Fh 0070h 0071h 0072h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0077h 0078h 0079h 007Ah 007Ah 007Bh 007Ch 007Ch 007Dh 007Dh 007Dh 007Eh 007Dh				
0070h 0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0076h 0077h 0078h 0079h 007Ah 007Bh 007Ch 007Ch 007Dh 007Dh 007Dh 007Eh 007Eh 007Eh	006Eh			
0071h 0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0077h 0077h 0078h 0079h 007Ah 007Ah 007Bh 007Ch 007Ch 007Dh 007Dh 007Dh 007Dh				
0072h Voltage Monitor 1 Interrupt Control Register VCMP1IC XXXXX000b 0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0077h 0078h 0079h 0079h 007Ah 007Bh 007Ch 007Dh 007Dh 007Dh 007Eh 007Eh				
0073h Voltage Monitor 2 Interrupt Control Register VCMP2IC XXXXX000b 0074h 0075h 0076h 0076h 0077h 0078h 0078h 0079h 0078h 0078				
0074h 0075h 0076h 0077h 0078h 0078h 0079h 007Ah 007Bh 007Ch 007Dh				
0075h 0076h 0077h 0078h 0079h 007Ah 007Bh 007Ch 007Dh 007Dh 007Eh		Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0076h 0077h 0078h 0079h 007Ah 007Bh 007Ch 007Dh 007Eh				
0077h 0078h 0079h 007Ah 007Ah 007Bh 007Ch 007Ch 007Dh				
0078h 0079h 007Ah 007Bh 007Ch 007Dh 007Dh 007Eh				
0079h 007Ah 007Bh 007Ch 007Dh 007Eh				
007Ah 007Bh 007Ch 007Dh 007Dh				
007Bh 007Ch 007Dh 007Eh				
007Ch 007Dh 007Eh			+	
007Dh 007Eh				
007Eh				
007Fh	007Eh			
	007Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Desistan	0:	A4 D
	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh	I man the times of the great	1112111	
0110h			
0111h			
0111h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0120h	Timer RC Control Register 1	TRCCR1	00h
012111 0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0122II			
	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			
			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh FFh
012Ah 012Bh	Timer RC General Register B	TRCGRB	
	1	TRCGRB	FFh
012Bh 012Ch	Timer RC General Register B Timer RC General Register C		FFh FFh FFh
012Bh 012Ch 012Dh	Timer RC General Register C	TRCGRC	FFh FFh FFh FFh
012Bh 012Ch 012Dh 012Eh	1		FFh FFh FFh FFh FFh
012Bh 012Ch 012Dh 012Eh 012Fh	Timer RC General Register C Timer RC General Register D	TRCGRC TRCGRD	FFh FFh FFh FFh FFh FFh
012Bh 012Ch 012Dh 012Eh 012Fh 0130h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2	TRCGRC TRCGRD TRCCR2	FFh FFh FFh FFh FFh O0011000b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register	TRCGRC TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh FFh 00011000b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register	TRCGRC TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh FFh 00011000b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Ch 012Dh 012Eh 013Fh 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0138h 0139h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Ch 012Dh 012Eh 013Fh 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0138h 0139h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Dh 012Eh 012Fh 0130h 0131h 0133h 0134h 0135h 0136h 0137h 0138h 0138h 0138h 0138h 0138h	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b 00h 01111111b
012Bh 012Ch 012Ch 012Dh 012Eh 013Fh 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h 013Ah	Timer RC General Register C Timer RC General Register D Timer RC Control Register 2 Timer RC Digital Filter Function Select Register Timer RC Output Master Enable Register	TRCGRC TRCGRD TRCCR2 TRCDF TRCOER	FFh FFh FFh FFh O0011000b O0h

Note:

^{1.} The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Table 4.7	of K information (r) (r)		
Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	<u> </u>		
0185h			
0186h			+
0187h			
	TIADTO Die Colort Desistes	Hoop	OOL-
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch			
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h	Low-Voltage Signal Mode Control Register	TSMR	00h
0191h	Tonago orgina modo control registor		00.1
0191h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			+
01A011			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			-
01B0H			
	Flook Mamony Chatus Dovistor	FCT	40000V001-
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B8h			
01B8h 01B9h			
01B8h 01B9h 01BAh			
01B8h 01B9h 01BAh 01BBh			
01B8h 01B9h 01BAh 01BBh 01BCh			
01B8h 01B9h 01BAh 01BBh 01BCh 01BDh			
01B8h 01B9h 01BAh 01BBh 01BCh			

X: Undefined

Note:

The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h	1		XXh
2CD2h	1		XXh
2CD3h	1		XXh
2CD4h	1		XXh
2CD5h	1		XXh
2CD6h	1		XXh
2CD7h	1		XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h	1		XXh
2CDAh	1		XXh
2CDBh	1		XXh
2CDCh			XXh
2CDDh	1		XXh
2CDEh	†		XXh
2CDFh	†		XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h	1		XXh
2CE2h	†		XXh
2CE3h	†		XXh
2CE4h	+		XXh
2CE5h	+		XXh
2CE6h	+		XXh
2CE7h	-		XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h	- Dio Gonii oi Bala 21	316321	XXh
2CEAh	-		XXh
2CEBh	-		XXh
2CECh	+		XXh
2CEDh	-		XXh
2CEEh	-		XXh
2CEFh	-		XXh
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h	B 10 doint of Bata 22	D10022	XXh
2CF2h	-		XXh
2CF3h	-		XXh
2CF4h	-		XXh
2CF5h	-		XXh
2CF6h	-		XXh
2CF7h	-		XXh
2CF7fi 2CF8h	DTC Control Data 23	DTCD23	XXh
2CF8h	DIO CONTION DATA 23	D1CD23	XXh
2CF9fi 2CFAh	-		XXh
	-		
2CFBh	-		XXh
2CFCh 2CFDh	4		XXh
ZUFUN	-		XXh
2000			XXh
2CFEh			V/VI-
2CFEh 2CFFh 2D00h			XXh

X: Undefined

Note:

^{1.} The blank areas are reserved and cannot be accessed by users.

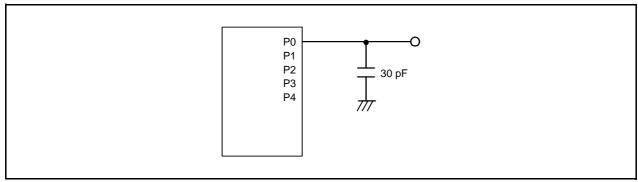


Figure 5.1 Ports P0 to P4 Timing Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Cumbal	Parameter	Conditions		Standa	ard	Lloit	
Symbol	Parameter	Conditions		Тур.	Max.	Unit	
_	Program/erase endurance (2)		1,000 (3)	_	_	times	
_	Byte program time		_	80	500	μS	
_	Block erase time		_	0.3	_	S	
td(SR-SUS)	Time delay from suspend request until suspend		_	_	5 + CPU clock × 3 cycles	ms	
_	Interval from erase start/restart until following suspend request		0	_	_	μS	
_	Time from suspend until erase restart		_	_	30 + CPU clock × 1 cycle	μS	
td(CMDRST -READY)	Time from when command is forcibly terminated until reading is enabled		_	_	30 + CPU clock × 1 cycle	μS	
_	Program, erase voltage		2.7	_	5.5	V	
_	Read voltage		1.8	_	5.5	V	
_	Program, erase temperature		0	_	60	°C	
_	Data hold time (7)	Ambient temperature = 55°C	20	_	_	year	

Notes

- 1. Vcc = 2.7 V to 5.5 V at Topr = 0°C to 60°C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

- However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
Symbol	Farameter	Conditions	Min.	Тур.	p. Max.	
_	Program/erase endurance (2)		10,000 (3)	_	_	times
_	Byte program time (program/erase endurance ≤ 1,000 times)		_	160	1,500	μS
_	Byte program time (program/erase endurance > 1,000 times)		_	300	1,500	μS
1	Block erase time (program/erase endurance ≤ 1,000 times)		_	0.2	1	S
1	Block erase time (program/erase endurance > 1,000 times)		_	0.3	1	S
td(SR-SUS)	Time delay from suspend request until suspend		_	_	5 + CPU clock × 3 cycles	ms
_	Interval from erase start/restart until following suspend request		0		_	μS
_	Time from suspend until erase restart		_	_	30 + CPU clock × 1 cycle	μS
td(CMDRST -READY)	Time from when command is forcibly terminated until reading is enabled		_	_	30 + CPU clock × 1 cycle	μS
_	Program, erase voltage		2.7	_	5.5	V
_	Read voltage		1.8	_	5.5	V
_	Program, erase temperature		-20	_	85	°C
_	Data hold time (7)	Ambient temperature = 55°C	20	_	_	year

Notes:

- 1. Vcc = 2.7 V to 5.5 V at Topr = -20° C to 85°C (N version), unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

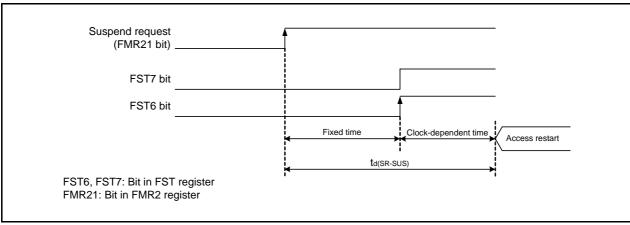


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
Syllibol	Faranietei	Condition	Min.	Тур.	Max.	Offic
Vdet0	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
_	Voltage detection 0 circuit response time (4)	At the falling of Vcc from 5 V to (Vdet0_0 - 0.1) V	_	6	150	μS
_	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	_	1.5		μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts (3)		_	_	100	μS

Notes:

- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20° C to 85°C (N version).
- 2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
- 4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.7 Voltage Detection 1 Circuit Electrical Characteristics

Cumbal	Doromotor	Condition		Standard		Unit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Vdet1	Voltage detection level Vdet1_0 (2)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of Vcc	4.20	4.45	4.75	V
_	Hysteresis width at the rising of Vcc in voltage	Vdet1_0 to Vdet1_5 selected	_	0.07	_	V
	detection 1 circuit	Vdet1_6 to Vdet1_F selected	_	0.10	_	V
_	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_0 - 0.1) V	_	60	150	μS
_	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	_	1.7	_	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		_	_	100	μS

Notes:

- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and $Topr = -20 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (N version).
- 2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
- 3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Timing Requirements

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C)

Table 5.15 External Clock Input (XOUT)

Symbol	bol Parameter -		Standard	
Symbol	Faidilletei	Min.	Max.	Unit
tc(XOUT)	XOUT input cycle time	50	_	ns
twh(xout)	XOUT input "H" width	24	_	ns
tWL(XOUT)	XOUT input "L" width	24	_	ns

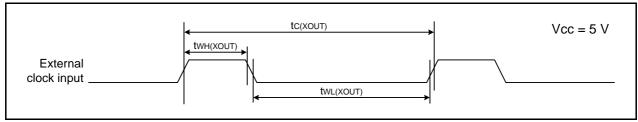


Figure 5.4 External Clock Input Timing Diagram when Vcc = 5 V

Table 5.16 TRAIO Input

Symbol	ol Parameter –		dard	Unit
Symbol			Max.	Offic
tc(TRAIO)	TRAIO input cycle time	100	_	ns
twh(traio)	TRAIO input "H" width	40	_	ns
tWL(TRAIO)	TRAIO input "L" width	40	_	ns

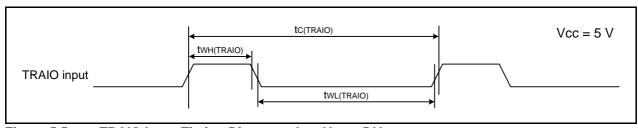


Figure 5.5 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.19 Electrical Characteristics (3) [2.7 V \leq Vcc < 4.2 V]

Symbol		Parameter	Condition		Condition Standard		Condition		Standard	Unit
Symbol		raiaillelei	Conditio	711	Min.	Тур.	Max.	Offic		
Vон	Output "H"	Other than XOUT	Drive capacity High	Iон = −5 mA	Vcc - 0.5	_	Vcc	V		
	voltage		Drive capacity Low	Iон = −1 mA	Vcc - 0.5	_	Vcc	V		
		XOUT		Ioн = -200 μA	1.0	_	Vcc	V		
Vol	Output "L"	Other than XOUT	Drive capacity High	IoL = 5 mA	_	_	0.5	V		
	voltage		Drive capacity Low	IoL = 1 mA	_	_	0.5	V		
		XOUT		IoL = 200 μA	_	_	0.5	V		
VT+-VT-	Hysteresis	INTO, INT1, INT2, INT3, KIO, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD2, CLK0, CLK2, SCL2, SDA2	Vcc = 3.0 V		0.1	0.4		V		
Iн	Input "H" cu	rrent	VI = 3 V, Vcc = 3.0 V		_		4.0	μА		
lıL	Input "L" cu	rrent	VI = 0 V, Vcc = 3.0 V		_	_	-4.0	μΑ		
RPULLUP	Pull-up resis	stance	VI = 0 V, Vcc = 3.0 V		42	84	168	kΩ		
RfXIN	Feedback resistance	XIN			_	0.3	_	МΩ		
VRAM	RAM hold v	oltage	During stop mode		1.8	_	_	V		

Note:

^{1.} $2.7 \text{ V} \le \text{Vcc} < 4.2 \text{ V}$ at Topr = -20°C to 85°C (N version), f(XIN) = 10 MHz, unless otherwise specified.

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C)

Table 5.21 External Clock Input (XOUT)

Symbol	nbol Parameter -		dard	Unit
Symbol	Falanielei	Min.	Max.	Offic
tc(XOUT)	XOUT input cycle time	50	_	ns
twh(xout)	XOUT input "H" width	24	_	ns
tWL(XOUT)	XOUT input "L" width	24	_	ns

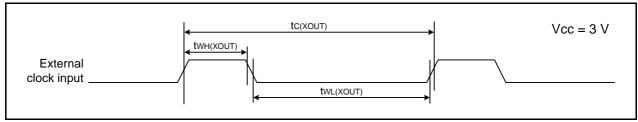


Figure 5.8 External Clock Input Timing Diagram when Vcc = 3 V

Table 5.22 TRAIO Input

Symbol	Symbol Parameter		dard	Unit
Symbol			Max.	Offic
tc(TRAIO)	TRAIO input cycle time	300	_	ns
tWH(TRAIO)	TRAIO input "H" width	120	_	ns
tWL(TRAIO)	TRAIO input "L" width	120	_	ns

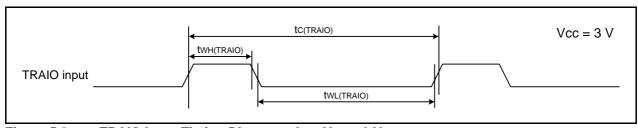


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.26 Electrical Characteristics (6) [1.8 V \leq Vcc < 2.7 V] (Topr = -20° C to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
Symbol	i alametei		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 1.8 V to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	2.2	_	mA
	other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	0.8	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.7	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTTRD = MSTTRC = 1		1	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	_	90	300	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	15	90	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	4	80	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	_	3.5	_	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2	5	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0		5	_	μΑ

Timing requirements

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.27 External Clock Input (XOUT)

Symbol	Symbol Parameter -		Standard	
Symbol			Max.	Unit
tc(XOUT)	XOUT input cycle time	200	_	ns
twh(xout)	XOUT input "H" width	90	_	ns
twl(xout)	XOUT input "L" width	90	_	ns

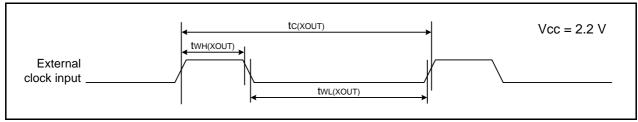


Figure 5.12 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.28 TRAIO Input

Symbol	Symbol Parameter -		dard	Unit
Symbol			Max.	Offic
tc(TRAIO)	TRAIO input cycle time	500	_	ns
tWH(TRAIO)	TRAIO input "H" width	200	_	ns
tWL(TRAIO)	TRAIO input "L" width	200	_	ns

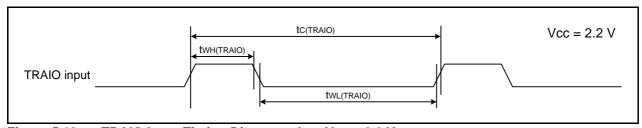


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.29 Serial Interface	Table	5.29	Serial	Interface
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Symbol	Parameter	Stan	Unit	
Symbol	Falameter	Min.	Max.	Offic
tc(CK)	CLKi input cycle time	800	_	ns
tW(CKH)	CLKi input "H" width	400	_	ns
tW(CKL)	CLKi input "L" width	400	_	ns
td(C-Q)	TXDi output delay time	_	200	ns
th(C-Q)	TXDi hold time	0	_	ns
tsu(D-C)	RXDi input setup time	150	_	ns
th(C-D)	RXDi input hold time	90	_	ns

i = 0, 2

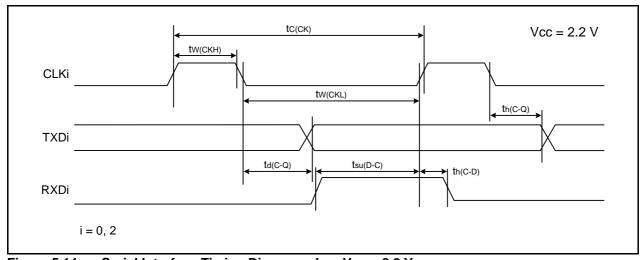


Figure 5.14 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.30 External Interrupt INTi (i = 0 to 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard		
Symbol	i didiffeter	Min.	Max.	Unit	
tW(INH)	INTi input "H" width, KIi input "H" width	1000 (1)	_	ns	
tW(INL)	INTi input "L" width, Kli input "L" width	1000 (2)		ns	

Notes:

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

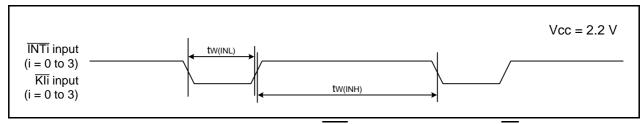


Figure 5.15 Input Timing for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 2.2 V