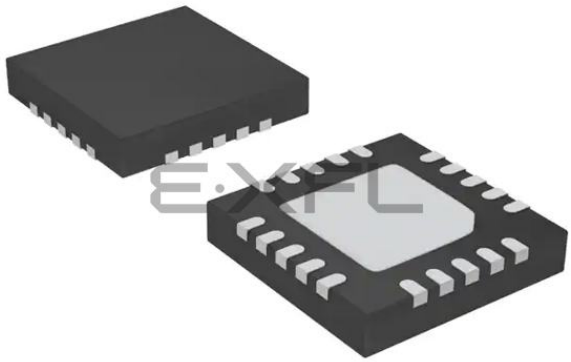

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.25V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f530-im

List of Tables

List of Registers

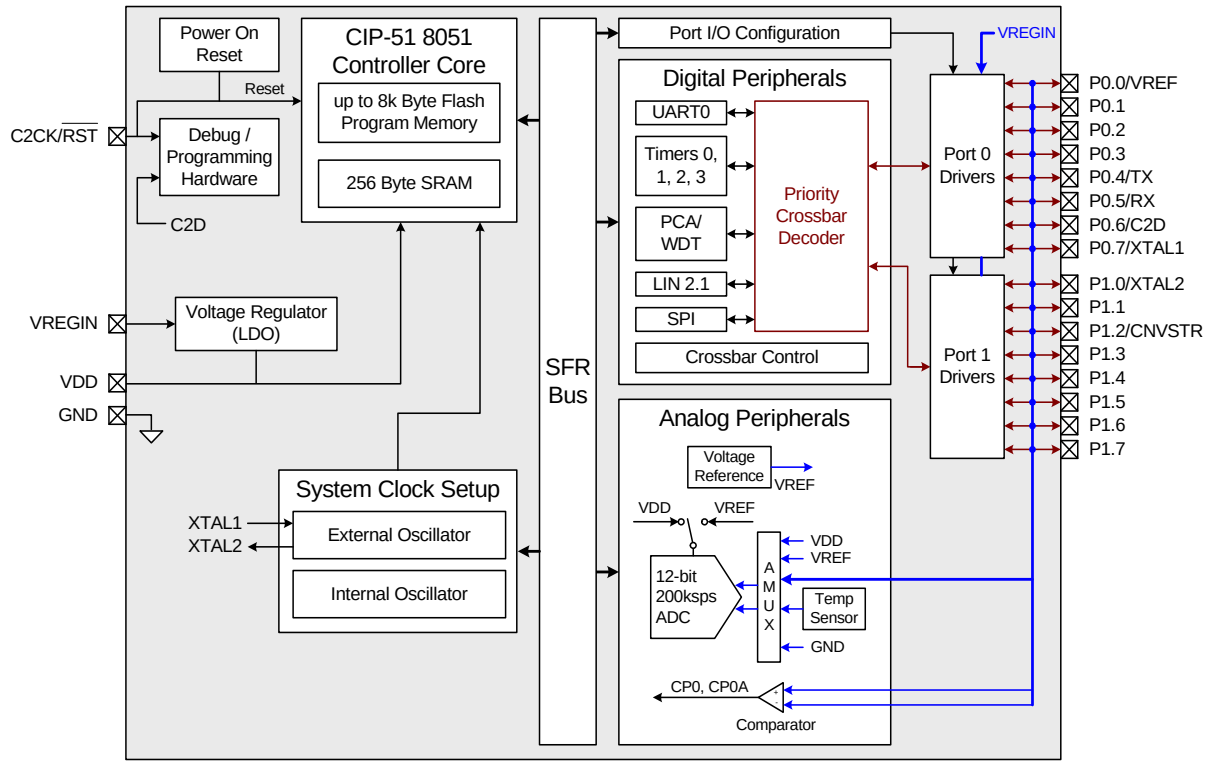

Figure 1.1. C8051F53xA/F53x-C Block Diagram

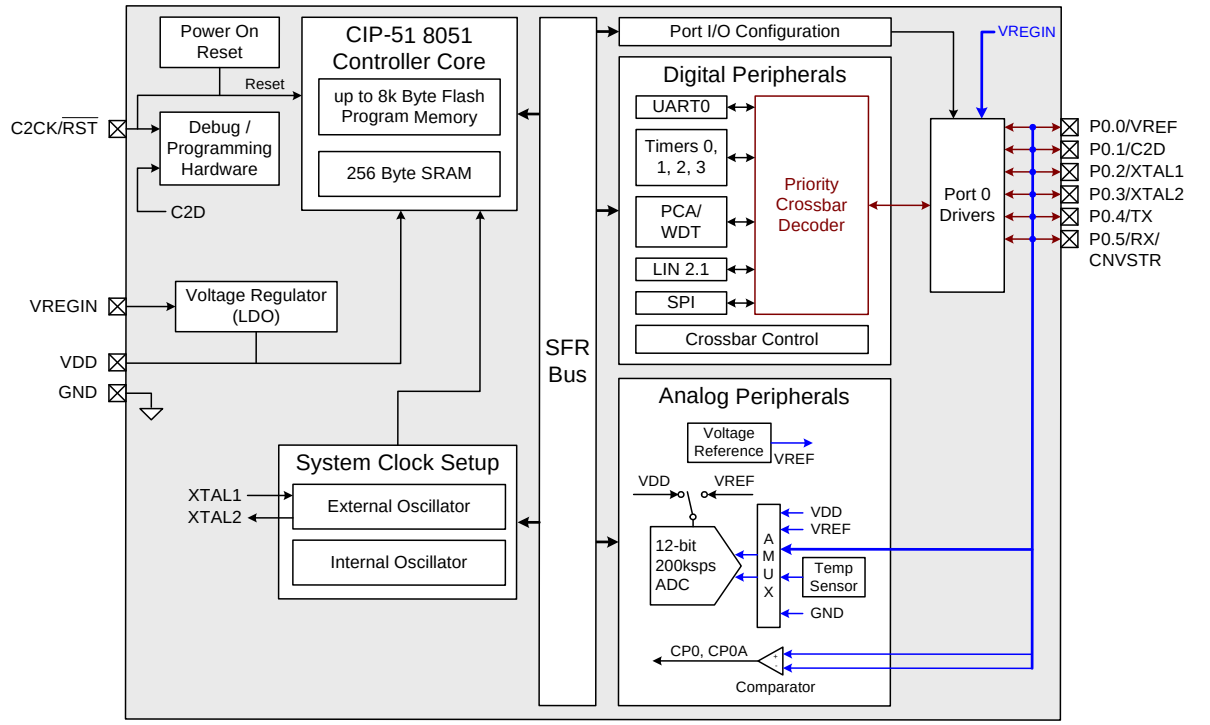

Figure 1.2. C8051F52xA/F52x-C Block Diagram

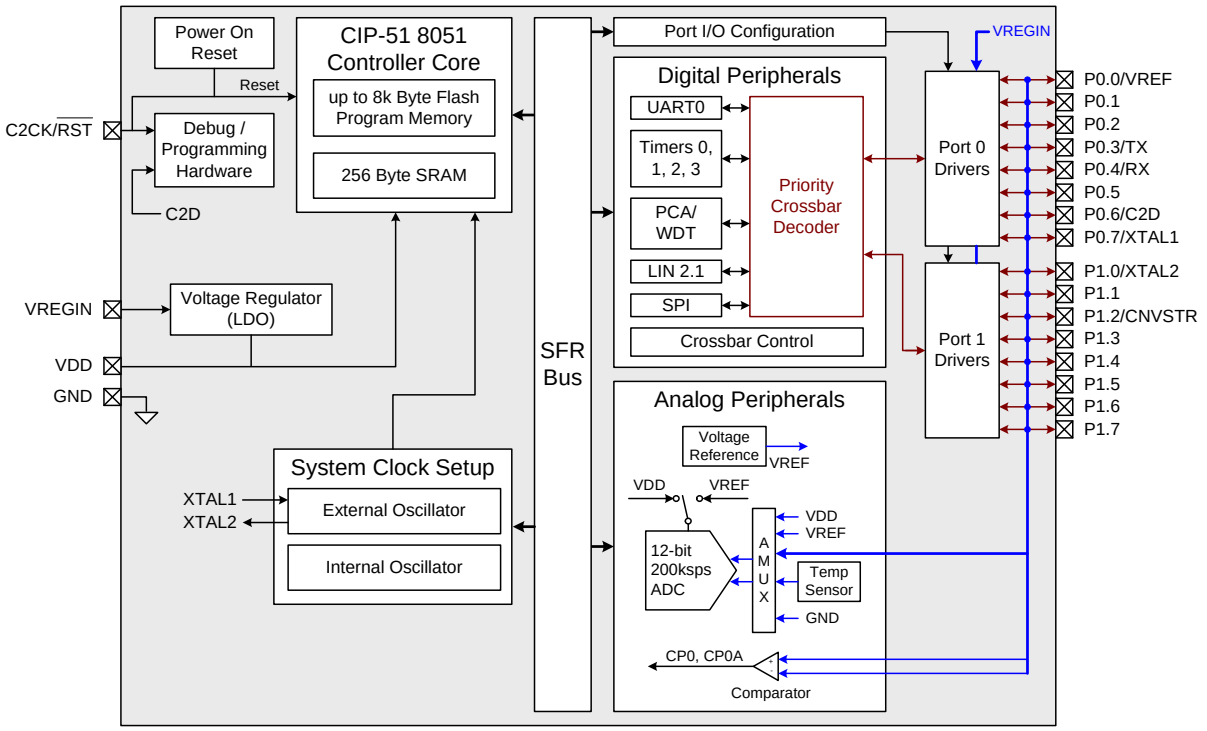

Figure 1.3. C8051F53x Block Diagram (Silicon Revision A)

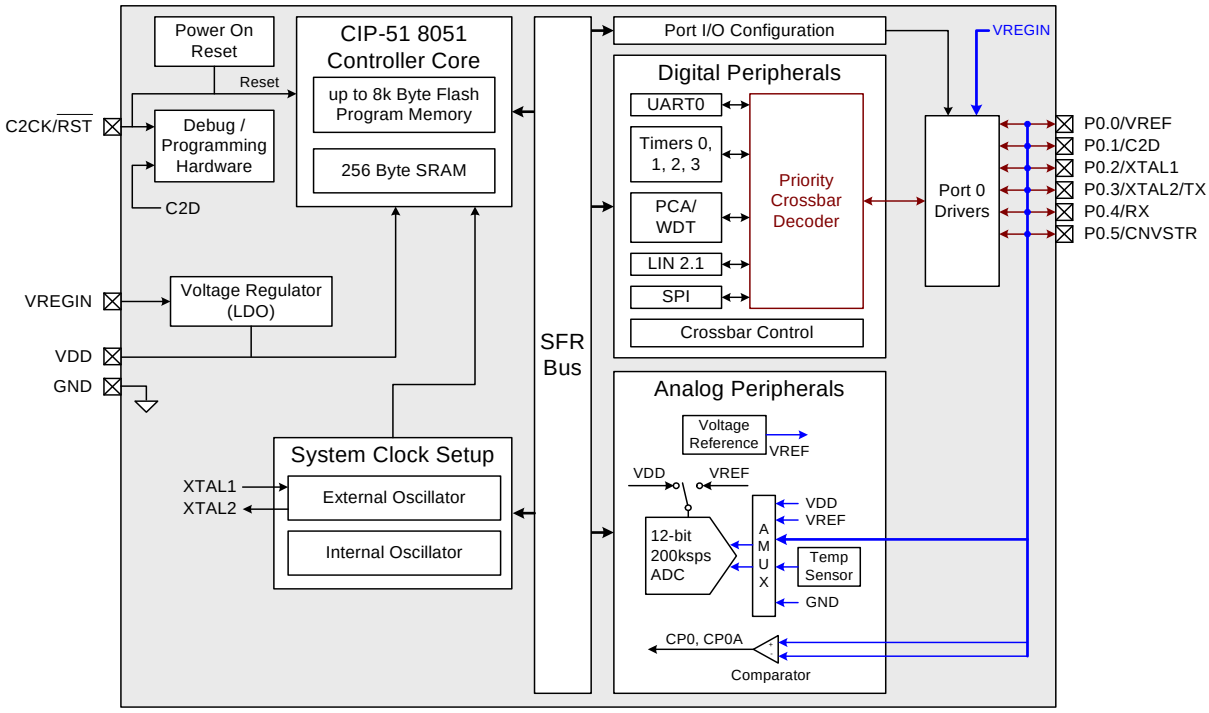

Figure 1.4. C8051F52x Block Diagram (Silicon Revision A)

1.9. Port Input/Output

C8051F52x/F52xA/F53x/F53xA devices include up to 16 I/O pins. Port pins are organized as two byte-wide ports. The port pins behave like typical 8051 ports with a few enhancements. Each port pin can be configured as a digital or analog I/O pin. Pins selected as digital I/O can be configured for push-pull or open-drain operation. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled to save power.

The Digital Crossbar allows mapping of internal digital system resources to port I/O pins. On-chip counter/timers, serial buses, hardware interrupts, and other digital signals can be configured to appear on the port pins using the Crossbar control registers. This allows the user to select the exact mix of general-purpose port I/O, digital, and analog resources needed for the application.

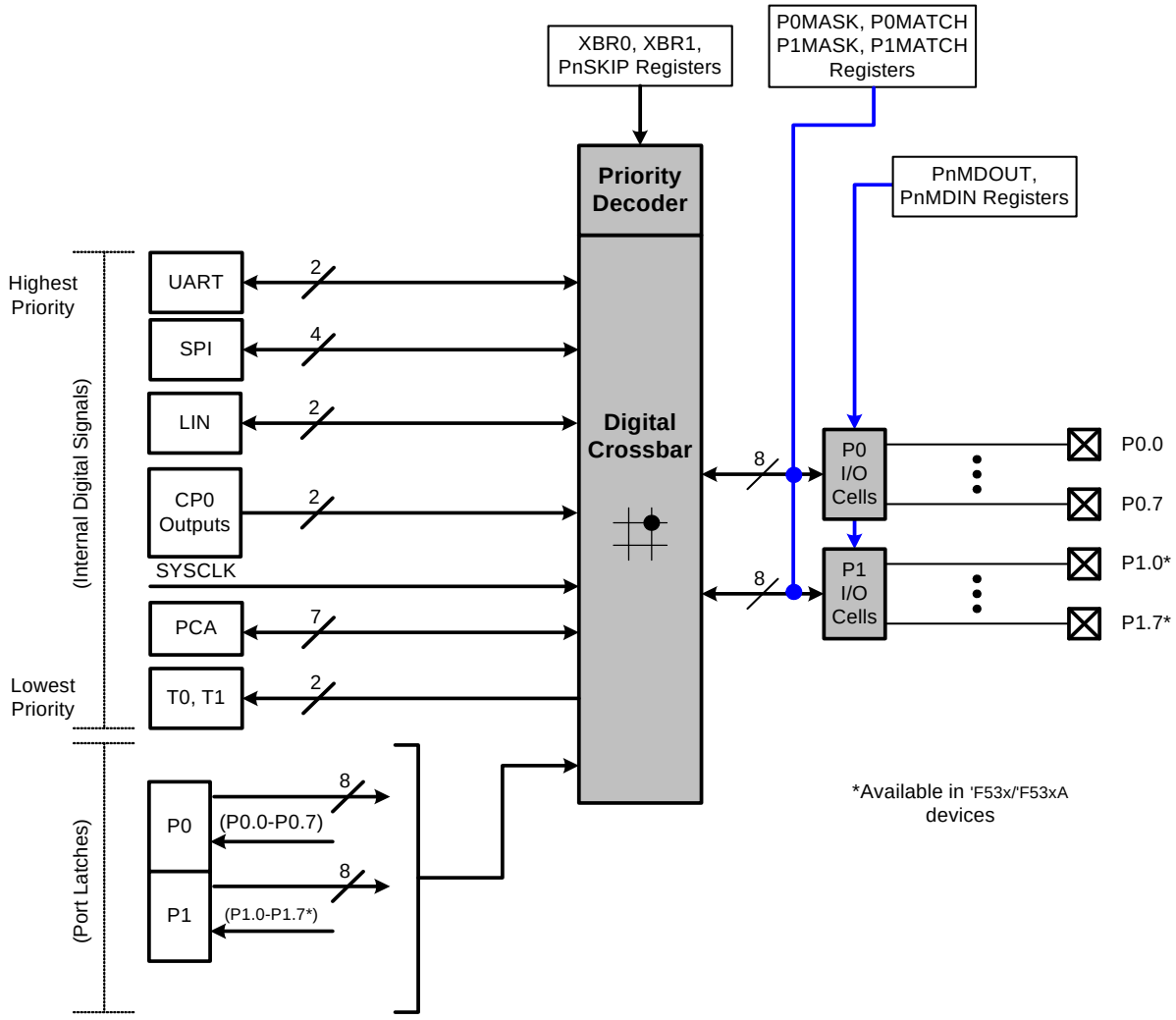

Figure 1.9. Port I/O Functional Block Diagram

Table 3.7. Pin Definitions for the C8051F53x and C805153xA (QFN 20)

Name	Pin Numbers		Type	Description
	‘F53xA ‘F53x-C	‘F53x		
$\overline{RST}$/ C2CK	1	1	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least the minimum $\overline{RST}$ low time to generate a system reset, as defined in Table 2.8 on page 32. A 1 kΩ pullup to V_{REGIN} is recommended. See Reset Sources Section for a complete description. Clock signal for the C2 Debug Interface.
P0.0/ V_{REF}	2	2	D I/O or A In A O or D In	Port 0.0. See Port I/O Section for a complete description. External V_{REF} Input. See V_{REF} Section.
GND	3	3		Ground.
V_{DD}	4	4		Core Supply Voltage.
V_{REGIN}	5	5		On-Chip Voltage Regulator Input.
P1.7	6	6	D I/O or A In	Port 1.7. See Port I/O Section for a complete description.
P1.6	7	7	D I/O or A In	Port 1.6. See Port I/O Section for a complete description.
P1.5	8	8	D I/O or A In	Port 1.5. See Port I/O Section for a complete description.
P1.4	9	9	D I/O or A In	Port 1.4. See Port I/O Section for a complete description.
P1.3	10	10	D I/O or A In	Port 1.3. See Port I/O Section for a complete description.
P1.2/ CNVSTR	11	11	D I/O or A In D In	Port 1.2. See Port I/O Section for a complete description. External Converter start input for the ADC0, see Section “4. 12-Bit ADC (ADC0)” on page 52 for a complete description.
P1.1	12	12	D I/O or A In	Port 1.1. See Port I/O Section for a complete description.
Note: Please refer to Section “20. Device Specific Behavior” on page 210.				

4. 12-Bit ADC (ADC0)

The ADC0 on the C8051F52x/F52xA/F53x/F53xA Family consists of an analog multiplexer (AMUX0) with 16/6 total input selections, and a 200 ksps, 12-bit successive-approximation-register (SAR) ADC with integrated track-and-hold, programmable window detector, programmable gain, and hardware accumulator. The ADC0 subsystem has a special Burst Mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. The AMUX0, data conversion modes, and window detector are all configurable under software control via the Special Function Registers shown in Figure 4.1. ADC0 inputs are single-ended and may be configured to measure P0.0-P1.7, the Temperature Sensor output, V_{DD}, or GND with respect to GND. The voltage reference for the ADC is selected as described in Section “5. Voltage Reference” on page 72. ADC0 is enabled when the AD0EN bit in the ADC0 Control register (ADC0CN) is set to logic 1, or when performing conversions in Burst Mode. ADC0 is in low power shutdown when AD0EN is logic 0 and no Burst Mode conversions are taking place.

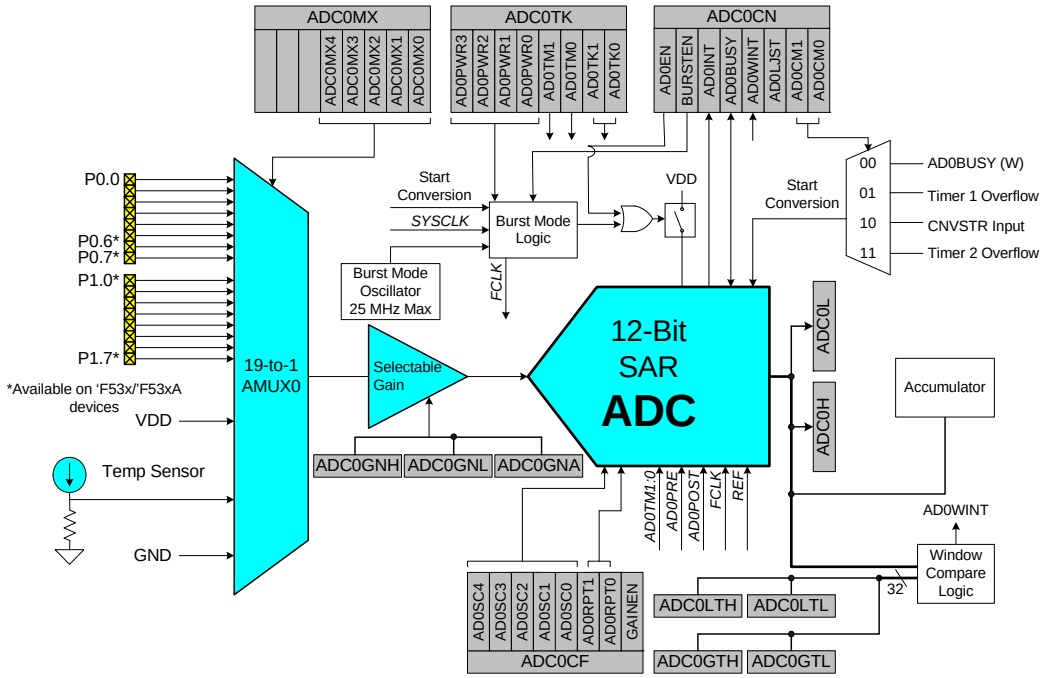

Figure 4.1. ADC0 Functional Block Diagram

4.1. Analog Multiplexer

AMUX0 selects the input channel to the ADC. Any of the following may be selected as an input: P0.0–P1.7, the on-chip temperature sensor, the core power supply (V_{DD}), or ground (GND). **ADC0 is single-ended and all signals measured are with respect to GND.** The ADC0 input channels are selected using the ADC0MX register as described in SFR Definition 4.4.

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN (for n = 0,1). To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP (for n = 0,1). See Section “13. Port Input/Output” on page 120 for more Port I/O configuration details.

SFR Definition 6.1. REG0CN: Regulator Control

R/W	R/W	R	R/W	R	R	R	R	Reset Value
REGDIS	Reserved	—	REG0MD	—	—	—	DROPOUT	01010000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC9

Bit7: **REGDIS**: Voltage Regulator Disable Bit.
This bit disables/enables the Voltage Regulator.
0: Voltage Regulator Enabled.
1: Voltage Regulator Disabled.
Bit6: **RESERVED**. Read = 1b. Must write 1b.
Bit5: **UNUSED**. Read = 0b. Write = don't care.
Bit4: **REG0MD**: Voltage Regulator Mode Select Bit.
This bit selects the Voltage Regulator output voltage.
0: Voltage Regulator output is 2.1 V.
1: Voltage Regulator output is 2.6 V (default).
Bits3–1: **UNUSED**. Read = 000b. Write = don't care.
Bit0: **DROPOUT**: Voltage Regulator Dropout Indicator Bit.
0: Voltage Regulator is not in dropout.
1: Voltage Regulator is in or near dropout.

Table 8.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit to Carry	2	2
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	4/5
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 9.1 lists the SFRs implemented in the CIP-51 System Controller.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the data sheet, as indicated in Table 9.2, for a detailed description of each register.

Table 9.1. Special Function Register (SFR) Memory Map

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0			VDDMON
F0	B	P0MDIN	P1MDIN				EIP1	
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2			RSTSRC
E0	ACC	XBR0	XBR1		IT01CF		EIE1	
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2			
D0	PSW	REF0CN			P0SKIP	P1SKIP		P0MAT
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H		P1MAT
C0				ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	P0MASK
B8	IP		ADC0TK	ADC0MX	ADC0CF	ADC0L	ADC0	P1MASK
B0	OSCIFIN	OSCXCN	OSCICN	OSCICL				FLKEY
A8	IE	CLKSEL						
A0		SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT		
98	SCON0	SBUF0		CPT0CN		CPT0MD		CPT0MX
90	P1		LINADDR	LINDATA		LINCF		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH				PCON
	0(8) (bit addressable)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

SFR Definition 10.2. IP: Interrupt Priority

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	PSPI0	PT2	PS0	PT1	PX1	PT0	PX0	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
							SFR Address:	0xB8

Bit7: **UNUSED**. Read = 1b; Write = don't care.
Bit6: **PSPI0**: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.
Bit5: **PT2**: Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupt.
0: Timer 2 interrupt set to low priority level.
1: Timer 2 interrupt set to high priority level.
Bit4: **PS0**: UART0 Interrupt Priority Control.
This bit sets the priority of the UART0 interrupt.
0: UART0 interrupt set to low priority level.
1: UART0 interrupt set to high priority level.
Bit3: **PT1**: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupt.
0: Timer 1 interrupt set to low priority level.
1: Timer 1 interrupt set to high priority level.
Bit2: **PX1**: External Interrupt 0 Priority Control.
This bit sets the priority of the external interrupt 1.
0: INT1 interrupt set to low priority level.
1: INT1 interrupt set to high priority level.
Bit1: **PT0**: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupt.
0: Timer 0 interrupt set to low priority level.
1: Timer 0 interrupt set to high priority level.
Bit0: **PX0**: External Interrupt 0 Priority Control.
This bit sets the priority of the external interrupt 0.
0: INT0 interrupt set to low priority level.
1: INT0 interrupt set to high priority level.

11.8. Software Reset

Software may force a reset by writing a 1 to the SWRSF bit (RSTSRC.4). The SWRSF bit will read 1 following a software forced reset. The state of the RST pin is unaffected by this reset.

12. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface or by software using the MOVX write instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operations is not required. Code execution is stalled during Flash write/erase operations. Refer to Table 2.9 on page 33 for complete Flash memory electrical characteristics.

12.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Laboratories or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section “21. C2 Interface” on page 214.

To protect the integrity of Flash contents, the V_{DD} monitor must be enabled to the higher setting (VDMLVL = '1') and selected as a reset source if software contains routines which erase or write Flash memory. If the V_{DD} monitor is not enabled, any erase or write performed on Flash memory will cause a Flash Error device reset. See Section “11.2. Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)” on page 108 for more information regarding the VDD monitor and the high threshold setting.

The V_{DD} monitor must be enabled before it is selected as a reset source. Selecting the V_{DD} monitor as a reset source before it is enabled and stabilized may cause a system reset. The procedure for re-enabling the V_{DD} monitor and configuring the V_{DD} monitor as a reset source is shown below:

1. Enable the V_{DD} monitor (VDMEN bit in VDDMON = 1).
2. Wait for the V_{DD} monitor to stabilize (see Table 2.8 on page 32 for the V_{DD} Monitor turn-on time). **Note: This delay should be omitted if software contains routines which write or erase Flash memory.**
3. Select the V_{DD} monitor as a reset source (PORSF bit in RSTSRC = 1).

Note: 8-bit MOVX instructions cannot be used to erase or write to Flash memory at addresses higher than 0x00FF.

Important Note: For –I (industrial Grade) parts, flash should be programmed (erase/write) at a minimum temperature of 0 °C for reliable flash operation across the entire temperature range of –40 to +125 °C. This minimum programming temperature does not apply to –A (Automotive Grade) parts.

12.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in SFR Definition 12.2.

SFR Definition 13.13. P0SKIP: Port0 Skip

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4

Bits7–0: **P1SKIP[7:0]**: Port1 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P1.n pin is not skipped by the Crossbar.
1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 13.14. P1MAT: Port1 Match

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xCF

Bits7–0: **P1MAT[7:0]**: Port1 Match Value.
These bits control the value that unmasked P0 Port pins are compared against. A Port Match event is generated if (P1 & P1MASK) does not equal (P1MAT & P1MASK).

SFR Definition 13.15. P1MASK: Port1 Mask

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBF

Bits7–0: **P1MASK[7:0]**: Port1 Mask Value.
These bits select which Port pins will be compared to the value stored in P1MAT.
0: Corresponding P1.n pin is ignored and cannot cause a Port Match event.
1: Corresponding P1.n pin is compared to the corresponding bit in P1MAT.

15.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 15.2), which is not user-accessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.

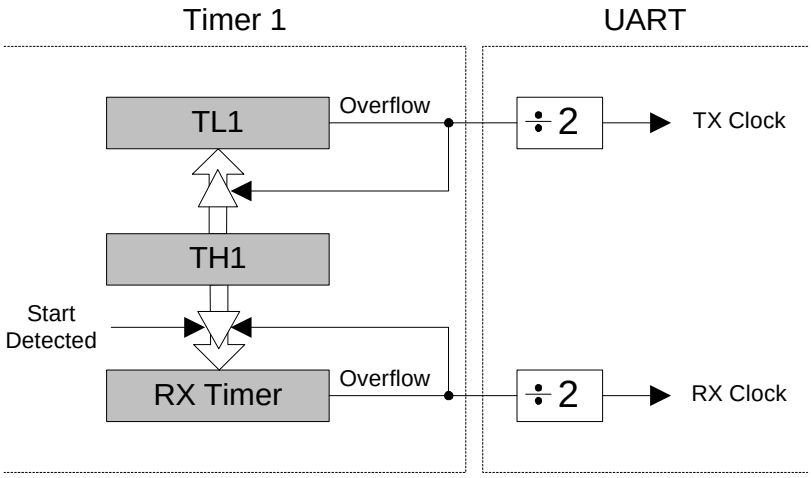

Figure 15.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload (see Section “18.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload” on page 184). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK / 4, SYSCLK / 12, SYSCLK / 48, the external oscillator clock / 8, or an external input T1. The UART0 baud rate is determined by Equation 15.1-A and Equation 15.1-B.

A) $$\text{UartBaudRate} = \frac{1}{2} \times \text{T1\_Overflow\_Rate}$$

B) $$\text{T1\_Overflow\_Rate} = \frac{\text{T1}_{CLK}}{256 - \text{TH1}}$$

Equation 15.1. UART0 Baud Rate

Where $T1_{CLK}$ is the frequency of the clock supplied to Timer 1, and *T1H* is the high byte of Timer 1 (8-bit auto-reload mode reload value). Timer 1 clock frequency is selected as described in Section “18. Timers” on page 182. A quick reference for typical baud rates and system clock frequencies is given in Table 15.1. Note that the internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.

16. Enhanced Serial Peripheral Interface (SPI0)

The Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

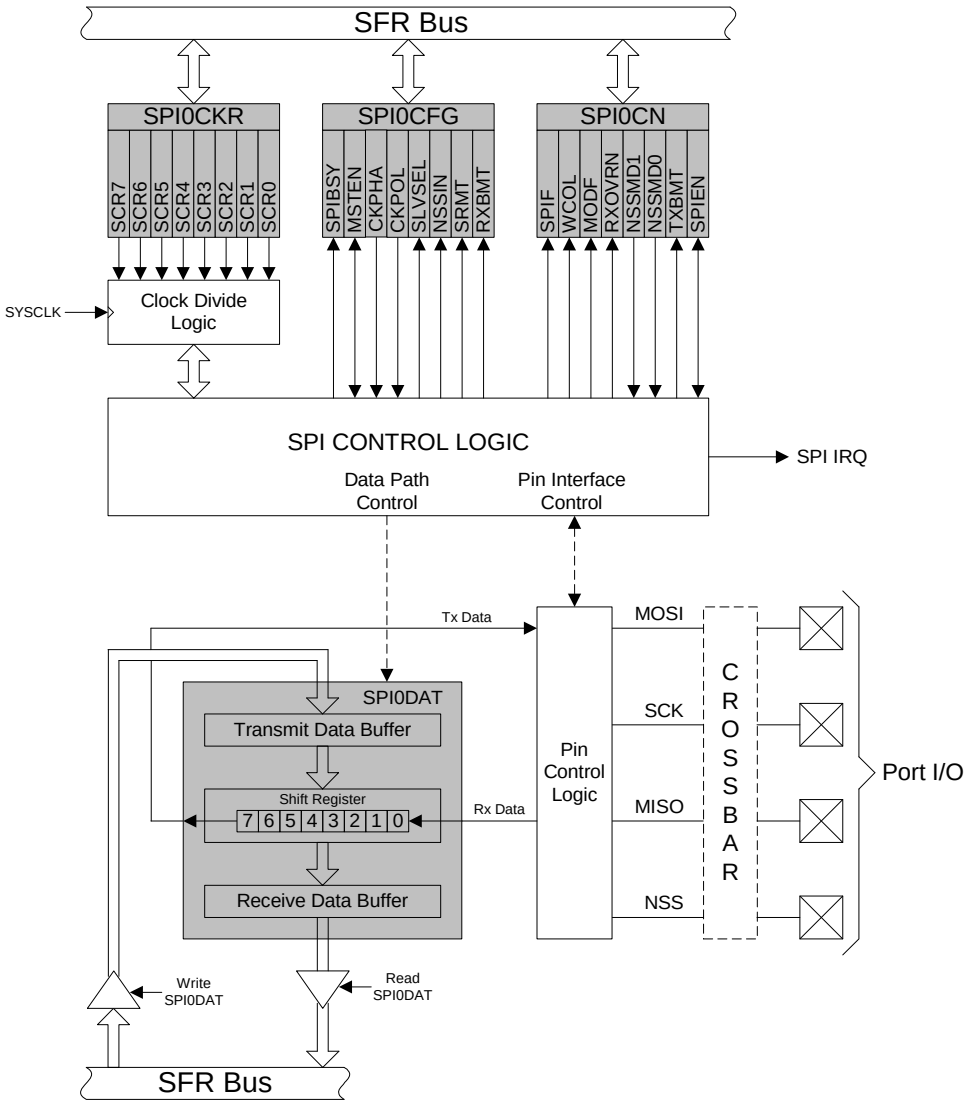

Figure 16.1. SPI Block Diagram

SFR Definition 17.3. LINCF Control Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
LINEN	MODE	ABAUD						00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x95

Bit7: **LINEN**: LIN Interface Enable bit
0: LIN0 is disabled.
1: LIN0 is enabled.

Bit6: **MODE**: LIN Mode Selection
0: LIN0 operates in Slave mode.
1: LIN0 operates in Master mode.

Bit5: **ABAUD**: LIN Mode Automatic Baud Rate Selection (**slave mode only**).
0: Manual baud rate selection is enabled.
1: Automatic baud rate selection is enabled.

SFR Definition 19.3. PCA0CPMn: PCA Capture/Compare Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPM0: 0xDA, PCA0CPM1: 0xDB, PCA0CPM2: 0xDC

Bit7: **PWM16n**: 16-bit Pulse Width Modulation Enable.
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit6: **ECOMn**: Comparator Function Enable.
This bit enables/disables the comparator function for PCA module n.
0: Disabled.
1: Enabled.

Bit5: **CAPPn**: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit4: **CAPNn**: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA module n.
0: Disabled.
1: Enabled.

Bit3: **MATn**: Match Function Enable.
This bit enables/disables the match function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic 1.
0: Disabled.
1: Enabled.

Bit2: **TOGn**: Toggle Function Enable.
This bit enables/disables the toggle function for PCA module n. When enabled, matches of the PCA counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic 1, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit1: **PWMn**: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is cleared; 16-bit mode is used if PWM16n is set to logic 1. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit0: **ECCFn**: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

SFR Definition 19.4. PCA0L: PCA Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9

Bits7–0: **PCA0L**: PCA Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.

SFR Definition 19.5. PCA0H: PCA Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xFA

Bits7–0: **PCA0H**: PCA Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer.

SFR Definition 19.6. PCA0CPLn: PCA Capture Module Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPL0: 0xFB, PCA0CPL1: 0xE9, PCA0CPL2: 0xEB

Bits7–0: **PCA0CPLn**: PCA Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.

SFR Definition 19.7. PCA0CPHn: PCA Capture Module High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPH0: 0xFC, PCA0CPH1: 0xE9, PCA0CPH2: 0xEC

Bits7–0: **PCA0CPHn**: PCA Capture Module High Byte.
The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n.

- Replaced minimum VDD value for Flash write/erase operations in Table 2.9 on page 33 with references to the $V_{RST-HIGH}$ theshold specified in Table 2.8 on page 32.
- Removed Output Low Voltage values for condition 'V_{REGIN} = 1.8 V' from Table 2.10, "Port I/O DC Electrical Characteristics," on page 33.
- Corrected minor typo ("IFCN = 111b") in Table 2.11, "Internal Oscillator Electrical Characteristics," on page 34.
- Removed the typical value and added the maximum value for the 'Wake-up Time From Suspend' specification with the 'ZTCEN = 0' condition in Table 2.11, "Internal Oscillator Electrical Characteristics," on page 34.
- Added Internal Oscillator Supply current values at specific temperatures for conditions 'ZTCEN = 1' and 'ZTCEN = 0' in Table 2.11, "Internal Oscillator Electrical Characteristics," on page 34. Also updated the table name to clarify that the specifications apply to the internal oscillator.
- Updated Section "1.1. Ordering Information" on page 14 and Table 1.1 with new C8051F52x-C/F53x-C part numbers.
- Updated Table 1.2, "Product Selection Guide (Not Recommended for New Designs)," on page 15 to include C8051F52xA/F53xA part numbers.
- Updated Figure 1.1, Figure 1.2, Figure 1.3, and Figure 1.4 titles to clarify applicable silicon revisions.
- Added figure references to pinout diagrams (Figure 3.1, Figure 3.4, and Figure 3.7) and updated labels to clarify applicable part numbers.
- Updated Table 3.1, Table 3.4, and Table 3.7 to indicate pinouts applicable to C8051F52x-C/F53x-C devices.
- Added note in Section "6. Voltage Regulator (REG0)" on page 74 to indicate the need for bypass capacitors for voltage regulator stability.
- Updated Figure 11.1 on Page 106 and text in Section "11.1. Power-On Reset" on page 107 and Section "11.2. Power-Fail Reset / VDD Monitors (VDDMON0 and VDDMON1)" on page 108 to describe the new level-sensitive V_{DD} monitor (VDDMON1).
- Updated SFR Definition 11.1. "VDDMON: VDD Monitor Control" on page 109 to include the VDM1EN bit (bit 4) that controls the new level-sensitive V_{DD} monitor (VDDMON1).
- Added notes in Section 11.1 on page 107, Section 11.2 on page 108, and Section 11.3 on page 110 with references to relevant parts of Section "20. Device Specific Behavior" on page 210.
- Moved some notes related to VDD Monitor (VDDMON0) High Threshold setting ($V_{RST-HIGH}$) from Section 11.2 on page 108 to Section 20.5 on page 212 in Section "20. Device Specific Behavior".
- Added Section "11.2.1. VDD Monitor Thresholds and Minimum VDD" on page 108 to describe the recommendations for minimum V_{DD} as it relates to the V_{DD} monitor thresholds.
- Clarified text in Section "11.7. Flash Error Reset" on page 110.
- Clarified text in items 2, 3 and 4 in Section "12.2.1. V_{DD} Maintenance and the V_{DD} monitor" on page 115 to reference appropriate specification tables and specify "VDDMON0".