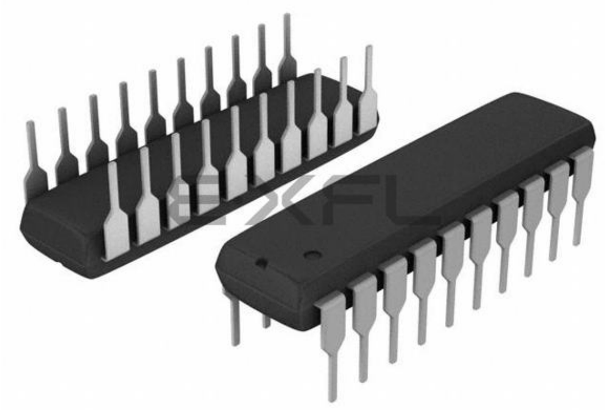

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c781-i-p

FIGURE 2-3: REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	PMDATL	10Ch	PMCON1	18Ch
	0Dh		8Dh	PMADRL	10Dh		18Dh
TMR1L	0Eh	PCON	8Eh	PMDATH	10Eh		18Eh
TMR1H	0Fh		8Fh	PMADRH	10Fh		18Fh
T1CON	10h		90h	CALCON	110h		190h
	11h		91h	PSMCCON0	111h		191h
	12h		92h	PSMCCON1	112h		192h
	13h		93h		113h		193h
	14h		94h		114h		194h
	15h	WPUB	95h		115h		195h
	16h	IOCB	96h		116h		196h
	17h		97h		117h		197h
	18h		98h		118h		198h
	19h		99h	CM1CON0	119h		199h
	1Ah		9Ah	CM2CON0	11Ah		19Ah
	1Bh	REFCON	9Bh	CM2CON1	11Bh		19Bh
	1Ch	LVDCON	9Ch	OPACON	11Ch		19Ch
	1Dh	ANSEL	9Dh		11Dh		19Dh
ADRES	1Eh		9Eh	DAC	11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh	DACON0	11Fh		19Fh
General Purpose Register 96 Bytes	20h–7Fh	General Purpose Register 32 Bytes	A0h–BFh		120h		1A0h
			EFh				
		accesses 70h-7Fh	F0h–FFh	accesses 70h-7Fh	170h–17Fh	accesses 70h-7Fh	1F0h–1FFh

☐ Unimplemented data memory locations, read as '0'.

* Not a physical register.

2.4 OPTION_REG Register

The OPTION_REG register is a readable and writable register which contains various control bits to configure:

- TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler)
- External INT interrupt
- TMR0
- Weak pull-ups on PORTB

Note:	To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION REGISTER (OPTION_REG: 81h, 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

bit7 bit0

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit(1)
`1` = PORTB weak pull-ups are disabled
`0` = PORTB weak pull-ups are enabled by the WPUB register

bit 6 **INTEDG:** Interrupt Edge Select bit
`1` = Interrupt on rising edge of RB0/INT pin
`0` = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
`1` = Transition on RA4/T0CKI pin
`0` = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
`1` = Increment on high-to-low transition on RA4/T0CKI pin
`0` = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
`1` = Prescaler is assigned to the WDT
`0` = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
`000`	1 : 2	1 : 1
`001`	1 : 4	1 : 2
`010`	1 : 8	1 : 4
`011`	1 : 16	1 : 8
`100`	1 : 32	1 : 16
`101`	1 : 64	1 : 32
`110`	1 : 128	1 : 64
`111`	1 : 256	1 : 128

Note 1: Individual weak pull-ups on RB pins can be enabled/disabled from the weak pull-up PORTB register (WPUB).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

3.0 I/O PORTS

Most pins for the I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC Mid-Range Reference Manual (DS33023)

3.1 I/O Port Analog/Digital Mode

The PIC16C781/782 has two I/O ports: PORTA and PORTB. Some of these port pins are mixed signal (can be digital or analog). When an analog signal is present on a pin, the pin must be configured as an analog input to prevent unnecessary current drawn from the power supply. The Analog Select register (ANSEL) allows the user to individually select the Digital/Analog mode on these pins. When the Analog mode is active, the port pin always reads as a logic 0.

> **Note 1:** On a Power-on Reset, the ANSEL register configures these mixed signal pins as Analog mode: RA<3:0>, RB<3:0>.
>
> **2:** If a pin is configured as Analog mode, the pin always reads '0', even if the digital output is active.

REGISTER 3-1: ANALOG SELECT REGISTER (ANSEL: 9Dh)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

bit 7-0 **ANS<7:0>:** Select Analog Input Function on AN<7:0> bits
1 = Analog input
0 = Digital I/O

Note: Setting a pin to an analog input disables the digital input buffer. The corresponding TRIS bit should be set to input mode when using pins as analog inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

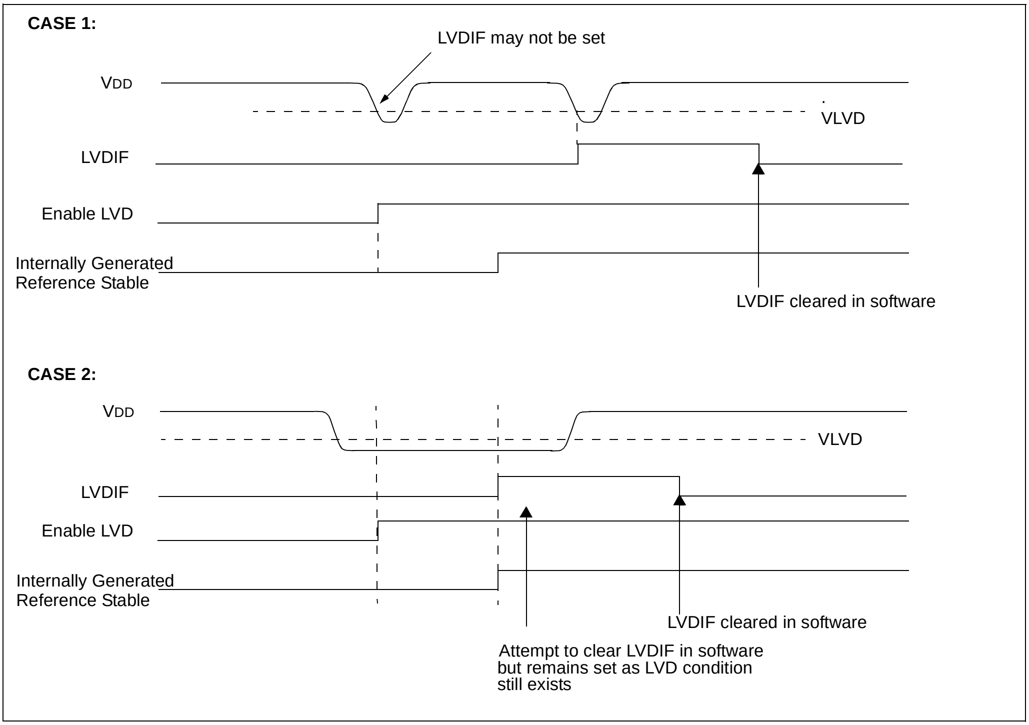
If another module has enabled the bandgap, then the reference will be stable when the PLVD module is enabled and the BGST flag can be ignored. However, if the bandgap has not been previously enabled, the LVDIF bit will not be valid until the BGST bit is set (see Figure 8-3). Systems using the PLVD interrupt should not enable the interrupt until after the reference is stable to prevent spurious interrupts.

8.2.1 SETTING UP THE PLVD MODULE

The following steps are needed to set up the PLVD Module:

1. Write the value to the LV3:LV0 bits (LVDCON register), which selects the desired PLVD Trip Point.
2. Ensure that PLVD interrupts are disabled (the LVDIE bit is cleared, or the GIE bit is cleared).
3. Enable the PLVD module (set the LVDEN bit in the LVDCON register).
4. Wait for the PLVD module to stabilize (the BGST bit to become set).
5. Clear the PLVD interrupt flag, which may have falsely become set until the PLVD module has stabilized (clear the LVDIF bit).
6. Enable the PLVD interrupt (set the LVDIE and the GIE bits).

FIGURE 8-3: LOW VOLTAGE DETECT WAVEFORMS



9.1.2 ADCON1 REGISTER

The ADCON1 register, shown in Register 9-3, controls the reference voltage selection for the ADC module.

Bits VCFG<1:0> select the reference voltage (ADCREF).

9.1.3 ADRES REGISTER

The ADRES register, shown in Register 9-2, contains the 8-bit result of the conversion. At the completion of the ADC conversion:

- 8-bit result is loaded into ADRES.
- GO/$\overline{\text{DONE}}$ bit (ADOCN0<2>) is cleared.
- ADC interrupt flag bit ADIF (INTCON<6> and PIR1<6>) are set.
- If the ADC interrupt is enabled, an interrupt is also generated.

REGISTER 9-2: ADC RESULT REGISTER (ADRES: 1Eh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
bit 7							bit 0

bit 7-0 **AD<7:0>:** ADC Conversion Results bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 9-3: ADC CONTROL REGISTER 1 (ADCON1: 9Fh)

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ’0’

bit 5-4 **VCFG<1:0>:** Voltage Reference Configuration bits
`00` = AVDD
`01` = VREF1
`10` = VR
`11` = VDAC

bit 3-0 **Unimplemented:** Read as ’0’

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

11.0 OPERATIONAL AMPLIFIER (OPA) MODULE

The Operational Amplifier (OPA) Module can be configured as either an OPAMP or Voltage Comparator. The OPA module has the following features:

- External connections to all ports
- Gain Bandwidth Product selectable:
  - 70 kHz nom.
  - 2 MHz nom.
- Low leakage inputs
- Input Offset Voltage Automatic Calibration Module (ACM)
- Input Offset Voltage calibration at a programmable common mode voltage using the DAC
- Interrupt-on-change in Comparator mode using IOCB

11.1 Control Registers

The OPACON register, shown in Register 11-1, controls the OPA module. The CALCON register, shown in Register 11-2, controls the Automatic Calibration Module.

11.1.1 OPACON REGISTER

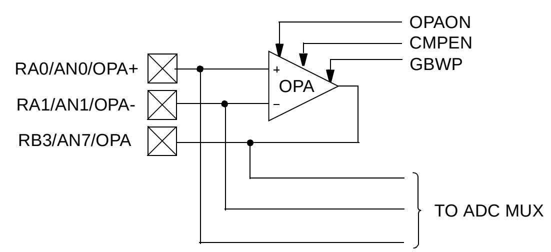
The OPA module is enabled by setting the OPAON bit (OPACON<7>). When enabled, the OPA forces the output driver of RB3/AN7/OPA into tri-state to prevent contention between the driver and the OPA output.

Clearing the CMPEN bit (OPACON,6>) configures the module as an OPAMP. Setting CMPEN configures the module as a voltage comparator.

The GBWP bit (OPACON<0>) controls the speed of the module in both comparator and OPAMP configurations. Setting GBWP results in a Gain Bandwidth Product (GBWP) of 2 MHz typical. Clearing GBWP0 results in a GBWP of the OPA of 70 kHz typical.

> **Note 1:** When the OPA module is enabled, the RB3/AN7/OPA pin is driven by the OPAMP output, not by the PORTB driver. Refer to the Electrical specifications for the OPAMP output drive capability.
>
> **2:** In Comparator mode (CMPEN = 1), an interrupt can be generated using the IOCB feature of RB3. RB3 must be programmed as a digital input with IOCB enabled.

FIGURE 11-1: OPA MODULE BLOCK DIAGRAM



12.0 COMPARATOR MODULE

The comparator module has two separate voltage comparators: Comparator C1 and Comparator C2 (see Figure 12-1).

Each comparator offers the following list of features:

- Control and configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from SLEEP
- Configurable as feedback input to the PSMC
- Programmable four input multiplexer
- Programmable reference selections
- Programmable speed
- Output synchronization to Timer1 clock input (Comparator C2 only)

12.1 Control Registers

Both comparators have separate control and configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

12.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 12-1) contains the control and status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> (CM1CON0<1:0>) select the comparator input from the four analog pins AN<7:4>.

Note:	To use AN<7:4> as analog inputs, the appropriate bits must be programmed in the ANSEL register.

Setting C1R (CM1CON0<2>) selects the output of the DAC module as the reference voltage for the comparator. Clearing C1R selects the VREF1 input on the RA3/AN3/VREF1 pin.

The output of the comparator is available internally via the C1OUT flag (CM1CON0<6>). To make the output available for an external connection, the C1OE flag (CM1CON0<5>) must be set. If the module is disabled with C1OE set, the output will be driven as shown in Table 12-2:

The polarity of the comparator output can be inverted by setting the C1POL flag (CM1CON0<4>). Clearing C1POL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 12-2.

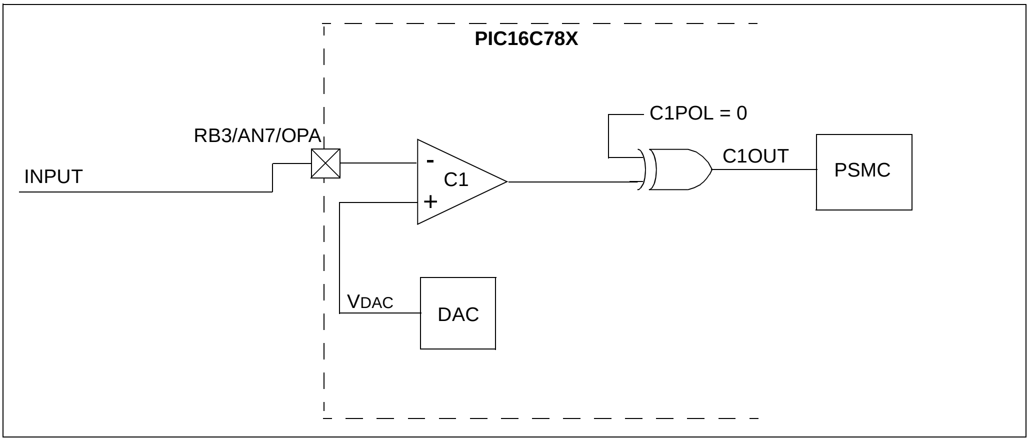
TABLE 12-1: OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	For the output of C1 on RB6/C1/PSMC1A, the PSMC must be disabled and TRISB<6> must be '0'.

C1SP (CM1CON0<3>) configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low power mode.

FIGURE 12-4: CONFIGURATION OF COMPARATOR C1 WITH DAC



EXAMPLE 12-2: PROGRAMMING C1 FOR PSMC FEEDBACK

```
;*  This code block will configure Comparator
;*  C1 for normal speed and output polarity,
;*  input on AN7, and Reference from the DAC

    BANKSEL    TRISA      ; Select Bank 1
    BSF        TRISB,RB3  ; RB3 as input
    BSF        ANSEL,AN7  ; Set RB3 as analog

    BANKSEL    DACON0     ; Select Bank 2
    CLRF       DAC        ; DAC=00h
    MOVLW      B'10000000'; Enable, no out
    MOVWF      DACON0     ; DACREF = VDD
    MOVLW      DAC_VALUE
    MOVWF      DAC        ; Trip Level

    MOVLW      B'10001111'; C1; no out,
    MOVWF      CM1CON0    ; VREF1, AN7
```

12.2.3 EXAMPLE: LOW POWER WINDOW COMPARATOR WITH INTERRUPT

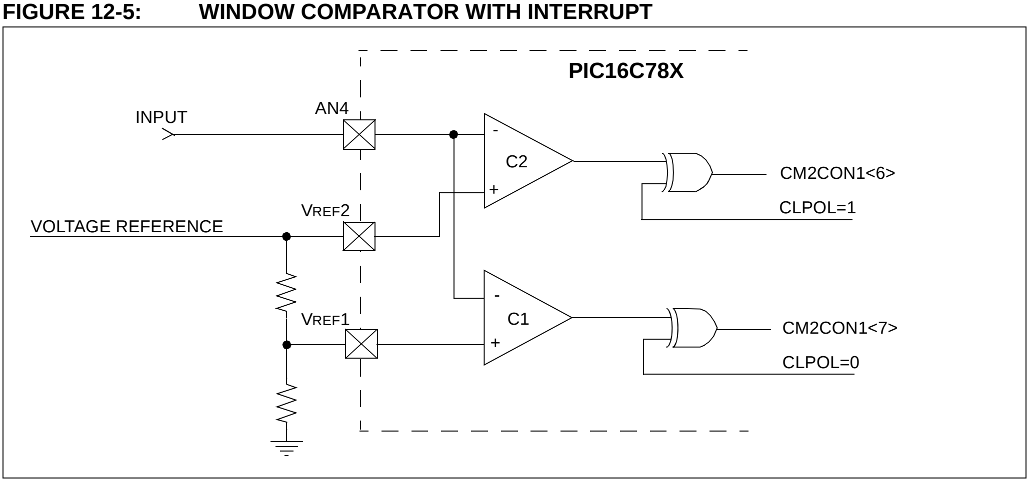
To form a low power window comparator, Comparators C1 & C2 are configured as follows:

- Common input RB0/INT/AN4/VREF
- Separate external reference voltages
- Programmed for slow speed operation

In addition, the output of comparator C2 must be inverted for common polarity with C1.

A block diagram of the window comparator with external connections is shown in Figure 12-4.

FIGURE 12-5: WINDOW COMPARATOR WITH INTERRUPT



 Preliminary

13.1.1 PULSE SKIP MODULATION (PSM)

In PSM (Pulse Skip Modulation), the PSMC operates as a fixed duty cycle pulse generator, with its output gated by the analog feedback (see Figure 13-3). Immediately prior to the initiation of a pulse, the analog feedback is sampled. If the comparator output = H, a pulse is initiated and held active for the programmed duty cycle. If the comparator output = L, no pulse is initiated and the PSMC waits for the start of the next pulse (see Table 13-3 and Table 13-4). In this mode, both the frequency and duty cycle of the output pulse are programmable. The analog feedback gates the presence or absence of the pulse on a pulse-by-pulse basis.

FIGURE 13-3: PSMC MODULE IN SINGLE OUTPUT PSM MODE (SIMPLIFIED BLOCK DIAGRAM)

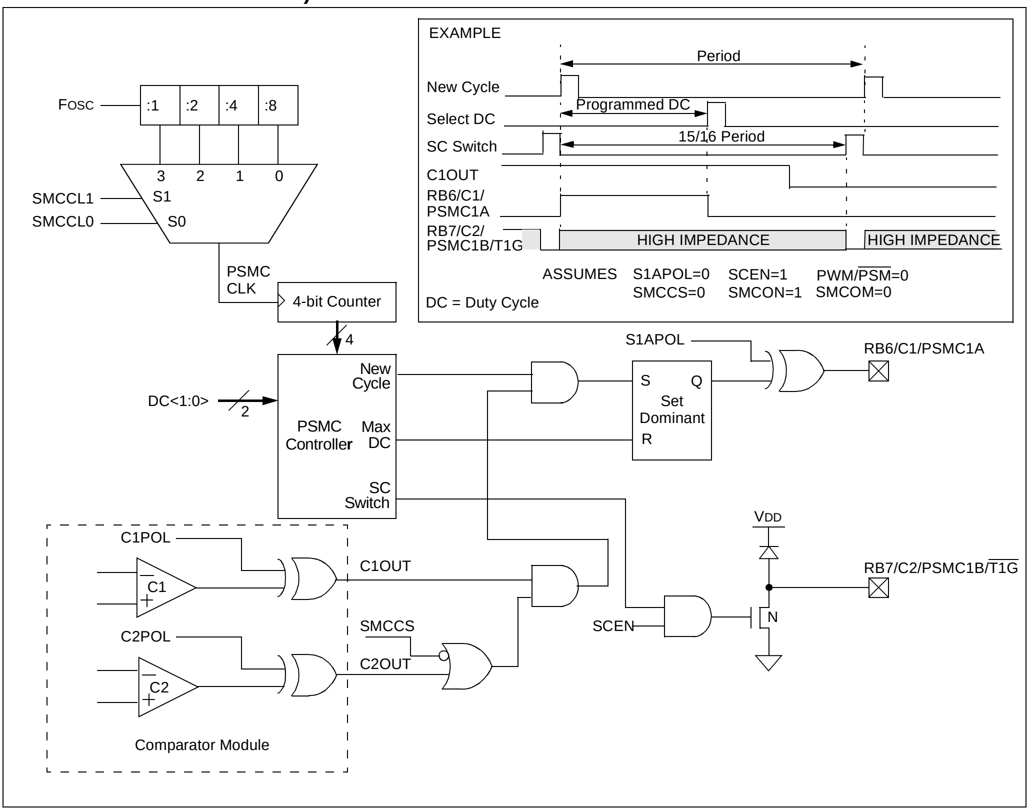


TABLE 13-3: PSMC1A OPERATION IN PSM MODE USING C1 COMPARATOR ONLY

Time	C1OUT	PSMC1A Output Signal
Beginning of PSM cycle	H	0 → 1
	L	0
During Pulse	x	No Change
		1
End of Pulse	x	1 → 0

Legend: x = Don't Care 0 = Inactive 1 = Active H = High L = Low

 Preliminary

13.4 Effects of SLEEP and RESET

A device RESET forces all registers to their RESET state. This disables the PSMC and resets its outputs to digital inputs. It is good design practice to include a fail-safe resistor bias in all power transistor drive circuitry. The fail-safe circuit should disable the power device when the PSMC output drive transistor is held tri-state. This protects the power device and its associated circuitry from the stress of prolonged operation without feedback.

Placing the PIC16C781/782 into SLEEP mode will stop the main oscillator for the microcontroller. The PSMC derives its timing from the main oscillator. Therefore, operation of the PSMC will halt when the microcontroller enters SLEEP mode. To prevent damage, the outputs of the PSMC are gated so that they are driven to their inactive state whenever the device enters SLEEP mode. When the microcontroller wakes up, the PSMC resumes operation per its previously programmed configuration.

TABLE 13-6: REGISTERS ASSOCIATED WITH THE PSMC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
86h,186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
111h	PSMCCON0	SMCCL1	SMCCL0	MINDC1	MINDC0	MAXDC1	MAXDC0	DC1	DC0	0000 0000	0000 0000
112h	PSMCCON1	SMCON	S1APOL	S1BPOL	—	SCEN	SMCOM	PWM/$\overline{\text{PSM}}$	SMCCS	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for PSMC.

14.9 Interrupts

The devices have up to eight sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on RESET.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT/AN4/VR pin interrupt, the RB port Interrupt-on-Change (IOCB) and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function register PIR1. The corresponding interrupt enable bits are contained in special function register PIE1, and the peripheral interrupt enable bit is contained in special function register INTCON.

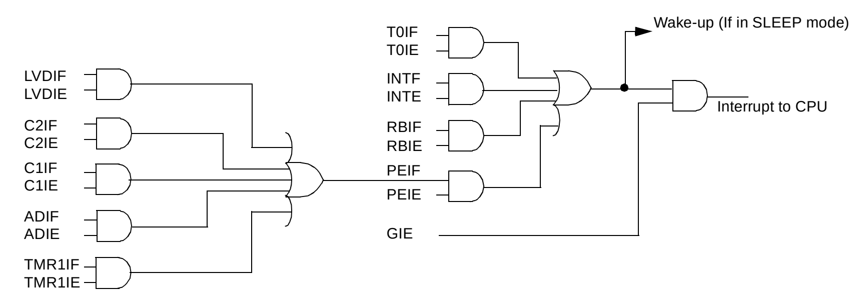
When an interrupt is serviced, the GIE bit is cleared to disable any further interrupt. The return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency is three or four instruction cycles. The exact latency depends on when the interrupt event occurs. The latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

14.9.1 INT INTERRUPT

External interrupt on RB0/INT/AN4/VR pin is edge triggered: either rising, if bit INTEDG (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can awaken the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following a wake-up sequence. See Section 14.12 for details on SLEEP mode.

FIGURE 14-10: INTERRUPT LOGIC



15.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND’ed with the eight bit literal 'k'. The result is placed in the W register.

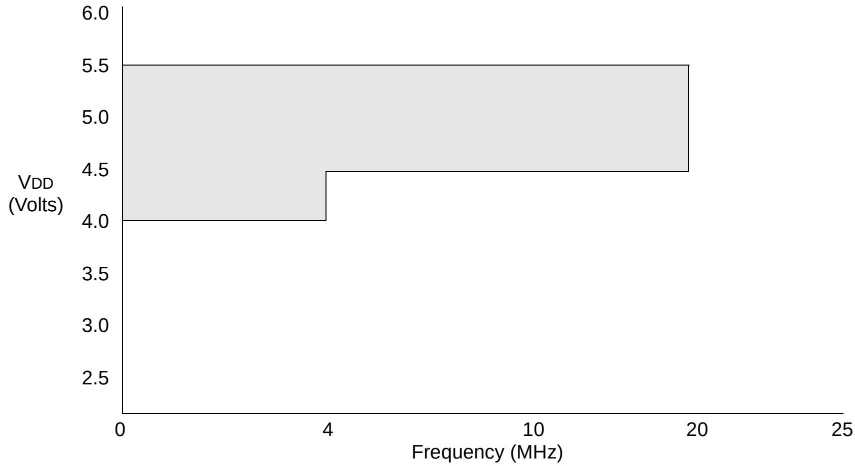
ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

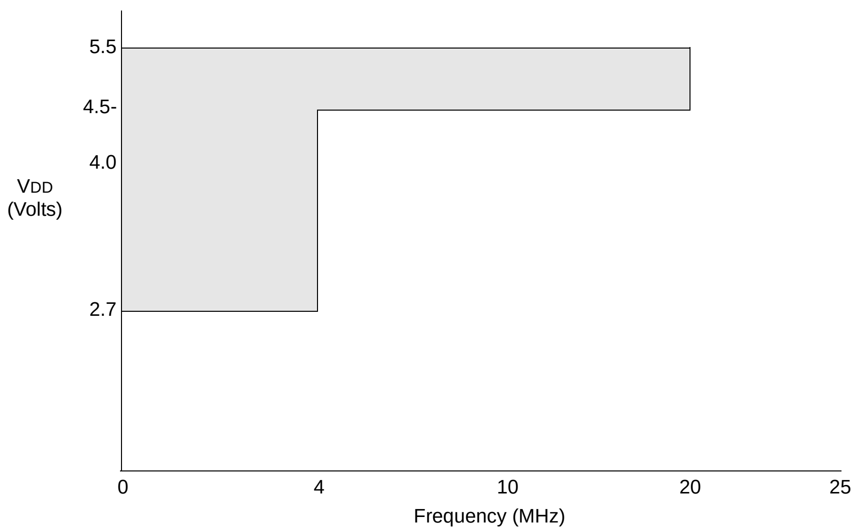
BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a `NOP` is executed instead, making this a $2T_{CY}$ instruction.

FIGURE 17-1: PIC16C781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: PIC16LC781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

17.2 DC Characteristics: Input/Output Pins

TABLE 17-2: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and Operating voltage VDD range as described in DC spec Section 17-1				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	I/O ports:					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	For entire VDD range
D032		$\overline{\text{MCLR}}$	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS, LP and EC)	VSS	—	0.3 VD	V	
		Input High Voltage					
	VIH	I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25VDD + 0.8V)	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		$\overline{\text{MCLR}}$	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS, LP and EC)	0.7VDD	—	VDD	V	
D070	IPURB	**PORTB Weak Pull-up Current Per Pin**	50	250	400	μA	VDD = 5V, VPIN = VSS
		Input Leakage Current(1,2)					
D060	IIL	I/O ports (with digital functions)	—	—	±1	μA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D060A	IIL	I/O ports (with analog functions)	—	—	±100	nA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		RA5/$\overline{\text{MCLR}}$/VPP	—	—	±5	μA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	μA	Vss ≤ VPIN ≤ VDD, XT, HS, LP and EC osc configuration
		Output Low Voltage					
D080	VOL	I/O ports (Includes CLKOUT)	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
		Output High Voltage					
D090	VOH	I/O ports(2) (Includes CLKOUT)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D150*	VOD	**Open Drain High Voltage**	—	—	10.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins*					
D100	Cosc2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	

* These parameters are characterized but not tested.

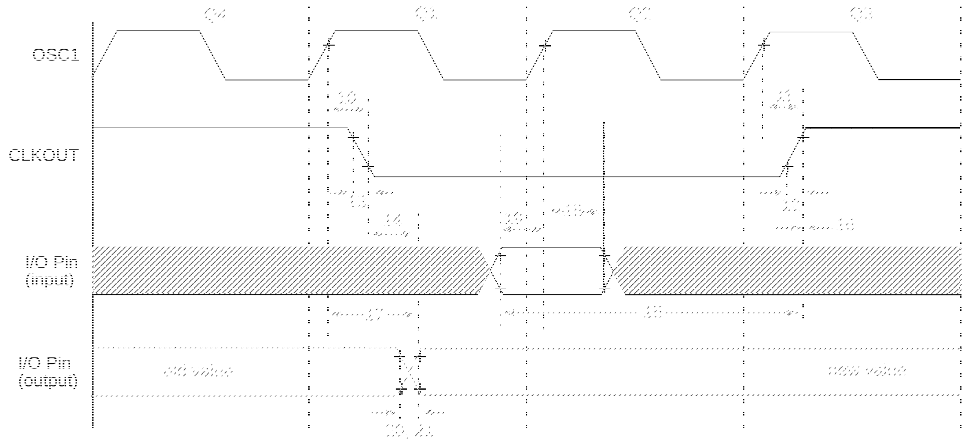
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

17.3.2 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 17-4: CLKOUT AND I/O TIMING



Note 1: Refer to Figure 17-3 for load conditions.

TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
10*	TOSH2CKL	OSC1↑ to CLKOUT↓		—	75	200	ns	**(Note 1)**
11*	TOSH2CKH	OSC1↑ to CLKOUT↑		—	75	200	ns	**(Note 1)**
12*	TCKR	CLKOUT rise time		—	35	100	ns	**(Note 1)**
13*	TCKF	CLKOUT fall time		—	35	100	ns	**(Note 1)**
14*	TCKL2IOV	CLKOUT ↓ to Port out valid		—	—	0.5TCY + 20	ns	**(Note 1)**
15*	TIOV2CKH	Port in valid before CLKOUT ↑		0.25TCY + 25	—	—	ns	**(Note 1)**
16*	TCKH2IOI	Port in hold after CLKOUT ↑		0	—	—	ns	**(Note 1)**
17*	TOSH2IOV	OSC1↑ (Q1 cycle) to Port out valid		—	50	150	ns	
18*	TOSH2IOI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	PIC16**C**781/782	100	—	—	ns	
			PIC16**LC**781/782	200	—	—	ns	
19*	TIOV2OSH	Port input valid to OSC1↑ (I/O in setup time)		0	—	—	ns	
20*	TIOR	Port output rise time	PIC16**C**781/782	—	10	25	ns	
			PIC16**LC**781/782	—	—	60	ns	
21*	TIOF	Port output fall time	PIC16**C**781/782	—	10	25	ns	
			PIC16**LC**781/782	—	—	60	ns	
22††*	TINP	INT pin high or low time		TCY	—	—	ns	
23††*	TRBP	RB7:RB0 change INT high or low time		TCY	—	—	ns	

* These parameters are characterized but not tested.

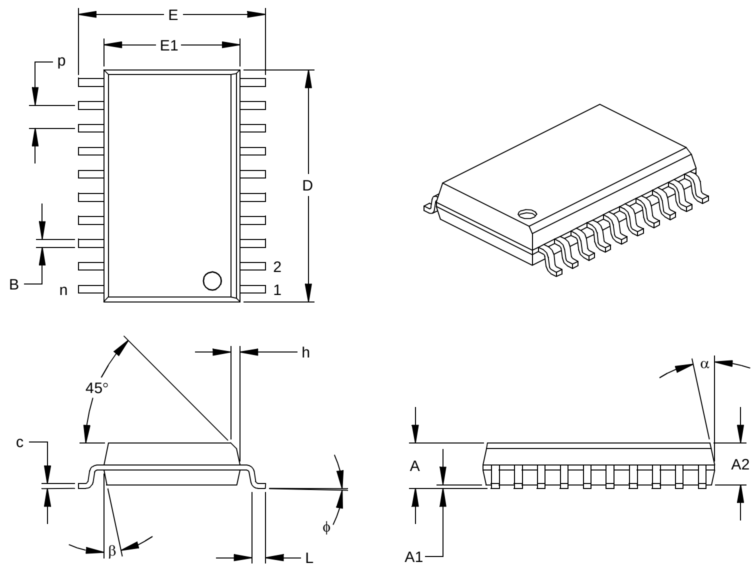
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

20-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.496	.504	.512	12.60	12.80	13.00
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

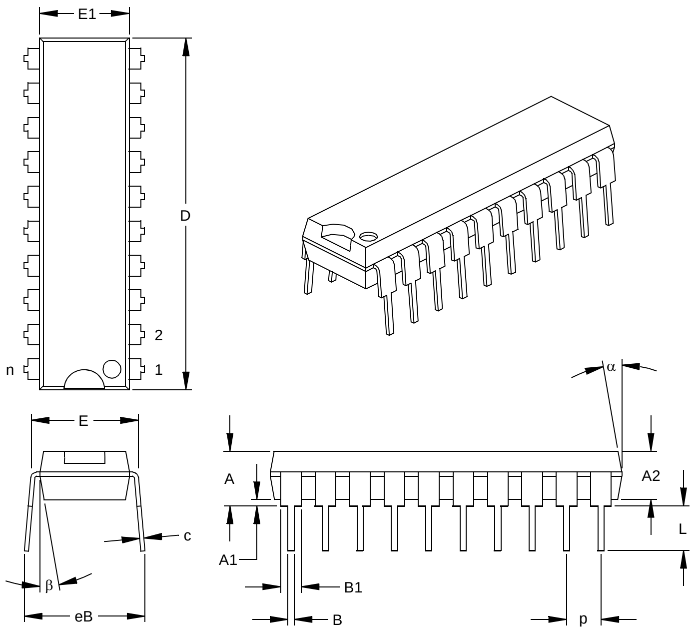
* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

 Preliminary

20-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019

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