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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c781-i-so

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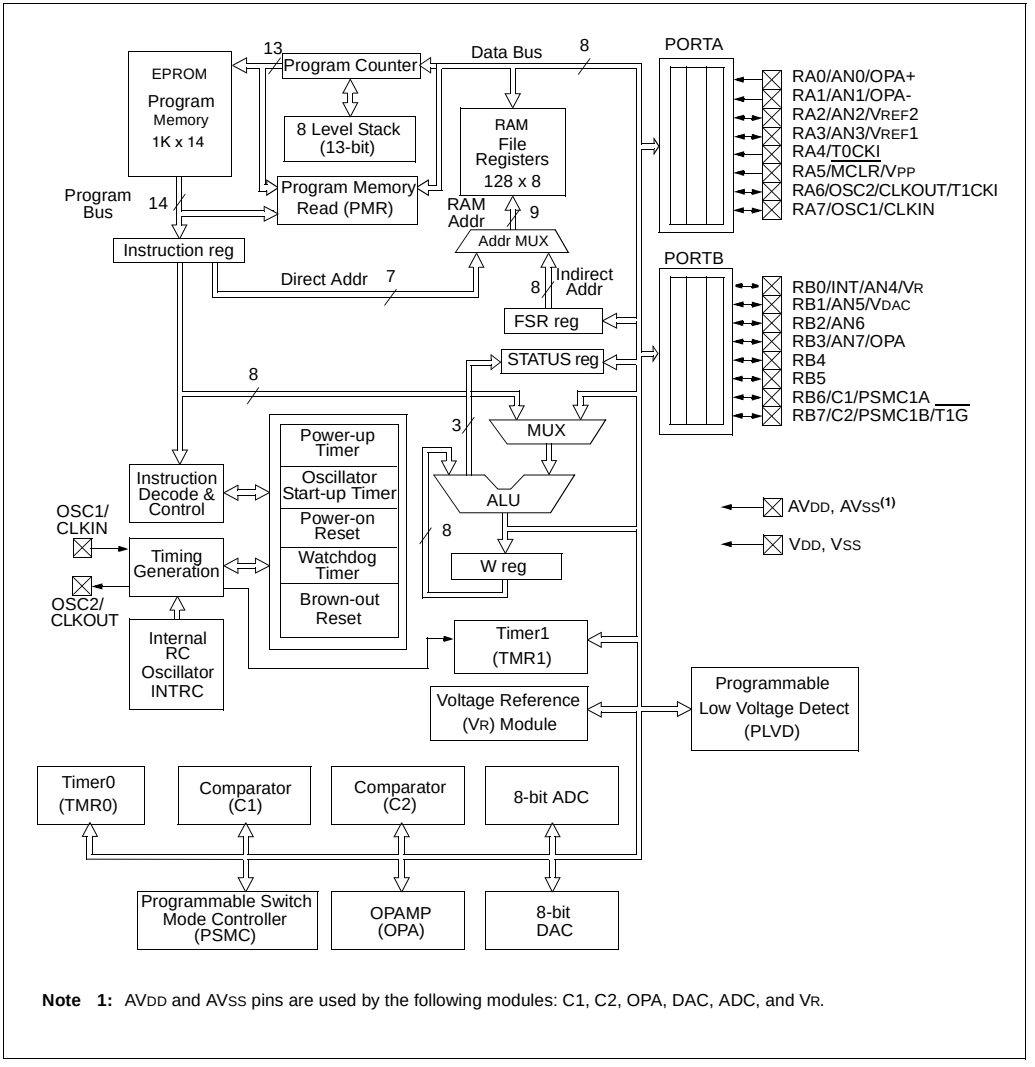
1.0 DEVICE OVERVIEW

This document contains device-specific information. Additional information may be found in the PIC Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference manual should be considered a complementary document to this data sheet. The Reference manual is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

This data sheet covers two devices: PIC16C781 and PIC16C782. Both devices come in a variety of 20-pin packages.

The following figures are block diagrams of the PIC16C781 and the PIC16C782.

FIGURE 1-1: PIC16C781 BLOCK DIAGRAM



Note 1: AVDD and AVSS pins are used by the following modules: C1, C2, OPA, DAC, ADC, and VR.

TABLE 1-1: PIC16C781/782 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7/C2/PSMC1B/$\overline{T1G}$	RB7	TTL	CMOS	Bi-directional I/O
	C2	—	CMOS	Comparator 2 Output
	PSMC1B	—	CMOS	PSMC Output 1B
	$\overline{T1G}$	ST	—	Timer 1 Gate Input
AVDD	AVDD	Power	—	Positive Supply for Analog
AVSS	AVSS	Power	—	Ground Reference for Analog
VDD	VDD	Power	—	Positive Supply for Logic and I/O pins
VSS	VSS	Power	—	Ground Reference for Logic and I/O pins

Legend: ST = Schmitt Trigger AN = Analog OD = open drain TTL = Logic Level
XTAL = Crystal CMOS = CMOS Output Power = Power Supply

2.6 PIE1 Register

The PIE1 register contains the individual enable bits for the peripheral interrupts.

Note:	Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt (see Register 2-3).

REGISTER 2-4: PERIPHERAL INTERRUPT ENABLE REGISTER (PIE1: 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
LVDIE	ADIE	C2IE	C1IE	—	—	—	TMR1IE
bit7							bit0

bit 7 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = LVD interrupt is enabled
0 = LVD interrupt is disabled

bit 6 **ADIE:** Analog-to-Digital Converter Interrupt Enable bit
1 = Enables the Analog-to-Digital Converter interrupt
0 = Disables the Analog-to-Digital Converter interrupt

bit 5 **C2IE:** Comparator C2 Interrupt Enable bit
1 = Enables the Comparator C2 interrupt
0 = Disables the Comparator C2 interrupt

bit 4 **C1IE:** Comparator C1 Interrupt Enable bit
1 = Enables the Comparator C1 interrupt
0 = Disables the Comparator C1 interrupt

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.9 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13-bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register occur through the PCLATH register.

2.9.1 PROGRAM MEMORY PAGING

PIC16C781/782 devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When performing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When performing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. A return instruction pops a PC address off the stack onto the PC register. Therefore, manipulation of the PCLATH<4:3> bits is not required for the return instructions (which POPs the address from the stack).

2.10 Stack

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed, or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW, or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.11 INDF

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is known as *indirect addressing*.

Reading INDF itself, indirectly (FSR = 0), produces 00h. Writing to the INDF register indirectly results in a no operation (although STATUS bits may be affected).

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
          movlw  0x20  ;initialize pointer
          movwf  FSR   ;  to RAM
NEXT      clrf   INDF  ;clear INDF register
          incf   FSR   ;inc pointer
          btfss  FSR,4 ;all done?
          goto   NEXT  ;NO, clear next
CONTINUE
          :            ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-5.

FIGURE 2-4: LOADING OF PC IN DIFFERENT SITUATIONS

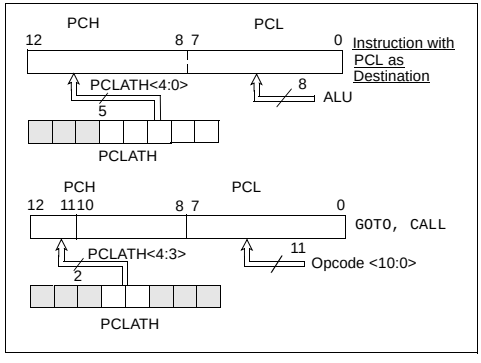
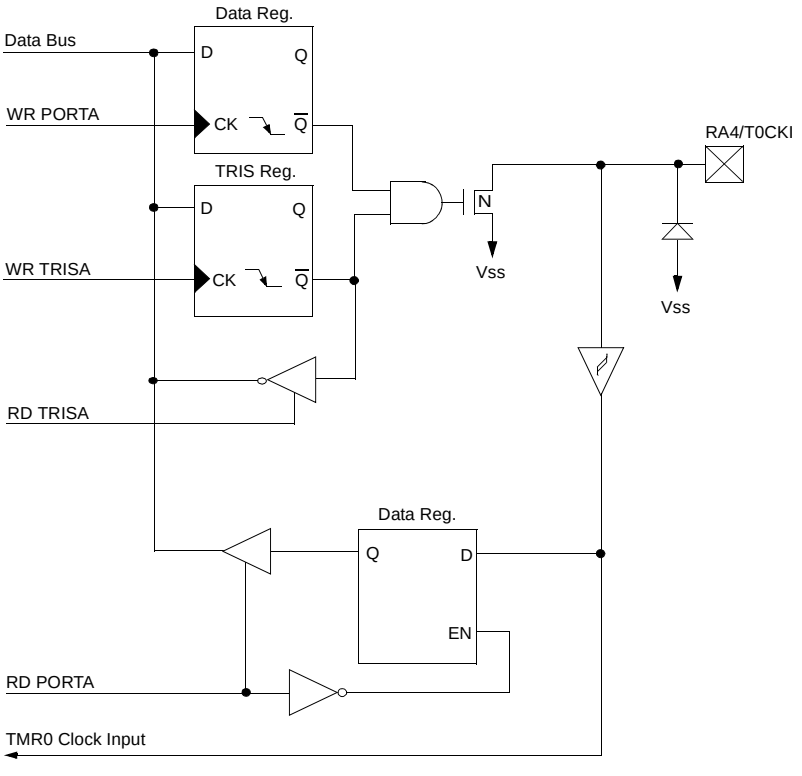


FIGURE 3-5: BLOCK DIAGRAM OF RA4/T0CKI PIN



TRISA<4>	PORTA<4>	FUNCTION	PORTA<4> READ
1	x	Digital In	Pin
0	0	0 Output	Pin
0	1	Hi-Z Output	Pin

REGISTER 3-2: WEAK PULL-UP PORTB REGISTER (WPUB: 95h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit7							bit0

bit 7-0 **WPUB<7:0>:** PORTB Weak Pull-Up Control bits

1 = Weak pull-up enabled for corresponding pin

0 = Weak pull-up disabled for corresponding pin

Note 1: For the WPUB register setting to take effect, the $\overline{\text{RBPU}}$ bit in the OPTION_REG register must be cleared.

2: The weak pull-up device is automatically disabled if the pin is in output mode, i.e., (TRISB = 0) for corresponding pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-3: INTERRUPT-ON-CHANGE PORTB REGISTER (IOCB: 96h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
IOCB7	IOCB6	IOCB5	IOCB4	IOCB3	IOCB2	IOCB1	IOCB0
bit7							bit0

bit 7-0 **IOCB<7:0>:** Interrupt-on-Change PORTB Control bits

1 = Interrupt-on-change enabled for corresponding pin

0 = Interrupt-on-change disabled for corresponding pin

Note 1: The interrupt enable bits, GIE and RBIE in the INTCON register, must be set for individual interrupts to be recognized.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

3.3.3 TRISB, ANSEL, AND CONTROL PRECEDENCE

The ANSEL and TRISB registers are the primary controls for the configuration of PORTB pins. TRISB tri-states the output drivers of PORTB, and the ANSEL register disables the input buffers. It is important to program both registers when configuring a port pin, since most peripherals do not have precedence over the TRISB and ANSEL registers' control of the pin. Even if a peripheral has the ability to override the control of the TRISB and ANSEL registers, it is good practice to program both registers appropriately.

Note 1: Upon RESET, the ANSEL register configures the RB<3:0> pins as analog inputs.

2: When programmed as analog inputs, RB<3:0> pins will read as '0'.

3: There are specific cases in which the functions of the TRISB and ANSEL registers can be overridden by a peripheral or configuration word (see Figure 3-9 through Figure 3-16 for details).

REGISTER 4-3: PROGRAM MEMORY DATA LOW (PMDATL: 10Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0
bit7							bit0

bit 7-0 **PMD<7:0>:** Program Memory Data bits
The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-4: PROGRAM MEMORY ADDRESS HIGH (PMADRH: 10Fh)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8
bit7							bit0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-3 **Reserved:** Read state is not guaranteed

bit 2-0 **PMA<10:8>**: PMR Address bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-5: PROGRAM MEMORY ADDRESS LOW (PMADRL: 10Dh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0
bit7							bit0

bit 7-0 **PMA<7:0>:** PMR Address bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

9.1.2 ADCON1 REGISTER

The ADCON1 register, shown in Register 9-3, controls the reference voltage selection for the ADC module.

Bits VCFG<1:0> select the reference voltage (ADCREF).

9.1.3 ADRES REGISTER

The ADRES register, shown in Register 9-2, contains the 8-bit result of the conversion. At the completion of the ADC conversion:

- 8-bit result is loaded into ADRES.
- GO/$\overline{\text{DONE}}$ bit (ADOCN0<2>) is cleared.
- ADC interrupt flag bit ADIF (INTCON<6> and PIR1<6>) are set.
- If the ADC interrupt is enabled, an interrupt is also generated.

REGISTER 9-2: ADC RESULT REGISTER (ADRES: 1Eh)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
bit 7							bit 0

bit 7-0 **AD<7:0>:** ADC Conversion Results bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 9-3: ADC CONTROL REGISTER 1 (ADCON1: 9Fh)

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ’0’

bit 5-4 **VCFG<1:0>:** Voltage Reference Configuration bits

00 = AVDD
01 = VREF1
10 = VR
11 = VDAC

bit 3-0 **Unimplemented:** Read as ’0’

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

TABLE 11-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
11Ch	OPACON	OPAON	CMPEN	—	—	—	—	—	GBWP	00-- ---0	00-- ---0
110h	CALCON	CAL	CALERR	CALREF	—	—	—	—	—	000- ----	000- ----
9Dh	ANSEL	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	1111 1111	1111 1111
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
85h	TRISA	PORTA Data Direction Register								1111 1111	1111 1111
11Eh	DAC	DA7	DA6	DA5	DA4	DA3	DA1	DA1	DA0	0000 0000	0000 0000
11Fh	DACON0	DAON	DAOE	—	—	—	—	DARS1	DARS0	00-- --00	00-- --00

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for the OPA module.

12.0 COMPARATOR MODULE

The comparator module has two separate voltage comparators: Comparator C1 and Comparator C2 (see Figure 12-1).

Each comparator offers the following list of features:

- Control and configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from SLEEP
- Configurable as feedback input to the PSMC
- Programmable four input multiplexer
- Programmable reference selections
- Programmable speed
- Output synchronization to Timer1 clock input (Comparator C2 only)

12.1 Control Registers

Both comparators have separate control and configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

12.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 12-1) contains the control and status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> (CM1CON0<1:0>) select the comparator input from the four analog pins AN<7:4>.

Note:	To use AN<7:4> as analog inputs, the appropriate bits must be programmed in the ANSEL register.

Setting C1R (CM1CON0<2>) selects the output of the DAC module as the reference voltage for the comparator. Clearing C1R selects the VREF1 input on the RA3/AN3/VREF1 pin.

The output of the comparator is available internally via the C1OUT flag (CM1CON0<6>). To make the output available for an external connection, the C1OE flag (CM1CON0<5>) must be set. If the module is disabled with C1OE set, the output will be driven as shown in Table 12-2:

The polarity of the comparator output can be inverted by setting the C1POL flag (CM1CON0<4>). Clearing C1POL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 12-2.

TABLE 12-1: OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C1 interrupt will operate correctly with C1OE set or cleared.
3:	For the output of C1 on RB6/C1/PSMC1A, the PSMC must be disabled and TRISB<6> must be '0'.

C1SP (CM1CON0<3>) configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low power mode.

TABLE 13-2: PSMC1A OUTPUT SEQUENCE IN PWM MODE USING C1 AND C2 COMPARATORS

Time	MINDC<1:0>	C1OUT	C2OUT	PSMC1A Output Signal
Beginning of PWM cycle	00	H	H	0 → 1
		L	x	0
		x	L	0
	non-zero	x	x	0 → 1
During Min Duty Cycle	non-zero	x	x	1
After Min Duty Cycle, Before Max Duty Cycle	x	H → L	H	q → 0
		L → H	x	0
		H	H → L	q → 0
		x	L → H	0
Max Duty Cycle	x	x	x	q → 0

Legend: x = Don't Care q = Prior State 0 = Inactive 1 = Active H = High L = Low

TABLE 13-4: PSMC1A OUTPUT SEQUENCE IN PSM MODE USING C1 AND C2 COMPARATORS

Time	C1OUT	C2OUT	PSMC1A Output Signal
Beginning of PSM cycle	H	H	0 → 1
	L	x	0
	x	L	0
During Pulse Duty Cycle	x	x	No Change
	x	x	No Change
After Pulse Duty Cycle	x	x	1 → 0

Legend: x = Don't Care 0 = Inactive 1 = Active H = High L = Low

13.1.2 SINGLE OR DUAL OUTPUT

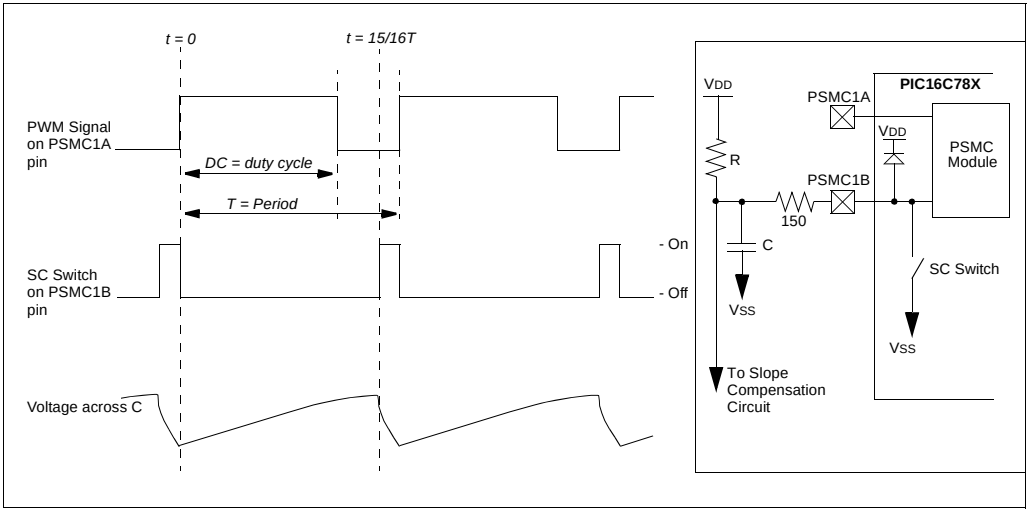
The PSMC has the capability to operate with either a single output, or dual alternating outputs. In the single output mode, the PSMC generates an output pulse on PSMC1A output only. The pulses are at the programmed frequency, and are variable between the programmed minimum and maximum duty cycle limits. In the dual output mode, the PSMC generates output pulses which alternate between PSMC1A and PSMC1B. The pulses generated at each output are generated at one half of the programmed frequency, and between 50% of the programmed minimum. and 50% maximum of the output duty cycle. The maximum duty cycle for either output is 50%.

13.1.3 SLOPE COMPENSATION

An optional feature of the PSMC single output mode is the ability to configure the PSMC1B output for use as a slope compensation ramp generator. In this mode, the PSMC1B output is pulled low for the last 1/16 of each pulse cycle. Connecting the PSMC1B output to an RC network, similar to Figure 13-4, results in a positive going pseudo ramp function. This pseudo ramp function is useful as an offset function for the loop error signal in unstable conditions at a duty cycle of greater than 50%.

Note:	When the Slope Compensation switch is enabled (SMCOM = 0, and SCEN = 1), the S1BPOL bit has no effect (see RC Network on next page for more detail).

FIGURE 13-4: SLOPE COMPENSATION (SC) SWITCH OPERATION



EXAMPLE 13-3: PERIPHERAL CONFIGURATION EXAMPLE

```
;***********************************************
;*  This code block will configure the PSMC and
;*  all additional peripherals for a motor speed
;*  control.
;*
;*  Order of configuration
;*  1.  PORTA/B I/O and analog configured
;*  2.  DAC enabled, configured, and preset
;*  3.  Op Amp enabled and configured
;*  4.  Comparator C1 enabled and configured
;*  5.  PSMC configured
;*  6.  PSMC enabled
;*
;***********************************************
;*  This code block will configure all analog ports.

    BANKSEL     TRISA               ; Select Bank 1
    MOVLW       B'01000011'
    MOVWF       TRISA               ; Set RA0,1 & 6 as inputs
    MOVLW       B'00001100'
    MOVWF       TRISB               ; Set RB2 & 3 as inputs
    MOVLW       B'11000011'
    MOVWF       ANSEL               ; Set AN0,1,6,& 7 as analog

;***********************************************
;*  This code block will configure the DAC for VR as
;*  DACREF, and no output.

    BANKSEL     REFCON
    BSF         REFCON, VREN        ; Enable VR
    BANKSEL     DACON0              ; Select Bank 2

    CLRF        DAC                 ; Set DAC to safe value
    MOVLW       B'10000010'         ; Enable DAC, no output
    MOVWF       DACON0              ;  and set DACREF = VR

    MOVLW       OUTPUT_VALUE
    MOVWF       DAC                 ; Set DAC output level

;***********************************************
;*  This code block will configure the OPA module
;*  as an Op Amp, with a 2 MHz GBWP

    MOVLW       B'10000001'         ; Set Op Amp mode and
    MOVWF       OPACON              ;  2 MHz GBWP

;***********************************************
*   This code block will configure Comparator C1
*   for normal speed and output polarity,
*   input on AN6, and Reference from the VDAC

    MOVLW       B'10001110'         ; Set C1; no ext out, norm
    MOVWF       CM1CON0             ;  speed & pol, VDAC, AN6

;***********************************************
;*  This code block will configure the PSMC module
;*  for PWM, Fosc/16, Single input, Single output
;*  Non-inverting out, DC min = 0%, DC max = 94%

    MOVLW       B'11001100'
    MOVWF       PSMCCON0            ; Set DCmin 0, DCmax 94, Fosc/16
    MOVLW       B'00000010'
    MOVWF       PSMCCON1            ; Set PWM, Sngl in/out, noninvert
    BSF         PSMCCON1,SMCON      ; Enable PSMC
```

14.8 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON, has two status bits that provide indication of which power-up type RESET occurred.

PCON<0> is Brown-out Reset Status bit, $\overline{BOR}$. Bit $\overline{BOR}$ is set on a Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if bit $\overline{BOR}$ cleared, indicating a BOR occurred. However, if the brown-out circuitry is disabled, the $\overline{BOR}$ bit is a "Don't Care" bit and is considered unknown upon a POR.

PCON<1> is $\overline{POR}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

When the CPU is running under the INTRC oscillator mode, the frequency of the INTRC oscillator can be switched to a power saving 37 kHz (nominal) mode. Clearing the OSCF (PCON<3>) enables oscillation at 37kHz, setting OSCF returns the oscillator to operation at 4MHz.

The Watchdog Timer is a free running, on-chip dedicated oscillator and timer, which does not require any external components to operate. The WDT provides a system RESET in the event that software does not execute a `CLRWDT` instruction within a specified interval. For reliability, the WDT will run even if the CPU clock has been stopped (for example, by the execution of a `SLEEP` instruction).

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to awaken and resume normal operation (Watchdog Timer Wake-up).

The WDT can be enabled either by setting the WDTE bit in the configuration register during programming, or by setting the WDTON bit (PCON<4>).

TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	TPWRT + 1024TOSC	1024TOSC	TPWRT + 1024TOSC	1024TOSC
EC, RC, INTRC	TPWRT	—	TPWRT	—

14.9 Interrupts

The devices have up to eight sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set, regardless of the status of the GIE bit. The GIE bit is cleared on RESET.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT/AN4/VR pin interrupt, the RB port Interrupt-on-Change (IOCB) and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function register PIR1. The corresponding interrupt enable bits are contained in special function register PIE1, and the peripheral interrupt enable bit is contained in special function register INTCON.

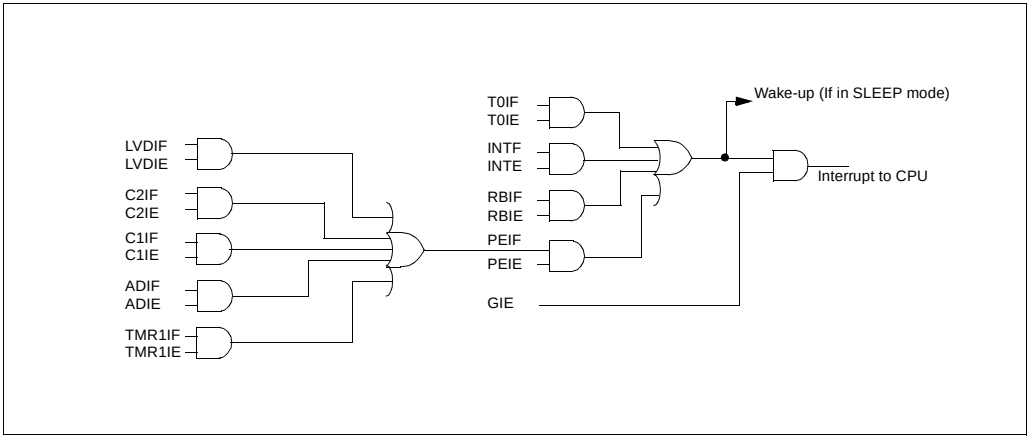
When an interrupt is serviced, the GIE bit is cleared to disable any further interrupt. The return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency is three or four instruction cycles. The exact latency depends on when the interrupt event occurs. The latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

14.9.1 INT INTERRUPT

External interrupt on RB0/INT/AN4/VR pin is edge triggered: either rising, if bit INTEDG (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can awaken the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following a wake-up sequence. See Section 14.12 for details on SLEEP mode.

FIGURE 14-10: INTERRUPT LOGIC



MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) → (destination)
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 127
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

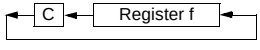
NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

RETLW	Return with Literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



17.1 DC Characteristics: Power Supply

TABLE 17-1: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	4.0 4.5	— —	5.5 5.5	V —	XT, EC, RC, INTRC Oscillator HS Oscillator
D001A	VDD	**Supply Voltage** (DSTEMP)	2.7 4.5	— —	5.5 5.5	V V	XT, EC, RC, INTRC Oscillator HS Oscillator
D002*	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	TBD	—	V	See section on Power-on Reset for details
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	IDD	**Supply Current(2)**	— — — —	TBD TBD TBD TBD	TBD TBD TBD TBD	mA mA mA mA	FOSC = 20 MHz, VDD = 5.5V* HS Oscillator FOSC = 20 MHz, VDD = 4.5V HS Oscillator FOSC = 4 MHz, VDD = 4.0V* XT, RC w/CLKOUT FOSC = 32 kHz, VDD = 4.0V LP Oscillator
D020 D020A	IPD	**Power-down Current(3)**	— —	TBD 1.5	TBD 19	µA µA	VDD = 5.5V VDD = 4.0V
	IOPA	**Operational Amplifier**	—	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, GBWP = 0 VDD = 5.0V, GBWP = 1
	IVC*	**Voltage Comparators C1 and C2**	— —	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, VID>100 mV C1SP = 0 VDD = 5.0 , VID>100 mV C1SP = 1
	IADC*	**Digital to Analog Converter (DAC)**	—	TBD	TBD	mA	VDD = 5.0V
D021	IWDT*	**Watchdog Timer**	—	TBD	TBD	mA	VDD = 4.0V
D026	IAD*	**Analog-to-Digital Converter (ADC)**	—	TBD	TBD	mA	VDD = 5.5V, ADC not converting
	IPLVD*	**Programmable Low Voltage Detect**		TBD	TBD	mA	VDD = 4.0V
	IPBOR*	**Programmable Brown-out Reset**		TBD	TBD	mA	VDD = 5.0V
1A	FOSC	**LP Oscillator, Operating Freq.** **INTRC Oscillator Operating Freq.** **XT Oscillator Operating Freq.** **HS Oscillator Operating Freq.**	9 — — 0 0	— 4 37 — —	200 — — 4 20	kHz MHz kHz MHz MHz	All temperatures All temperatures, OSCF = 1 All temperatures, OSCF = 0 All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins configured as inputs, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins configured as iputs and tied to VDD or VSS.

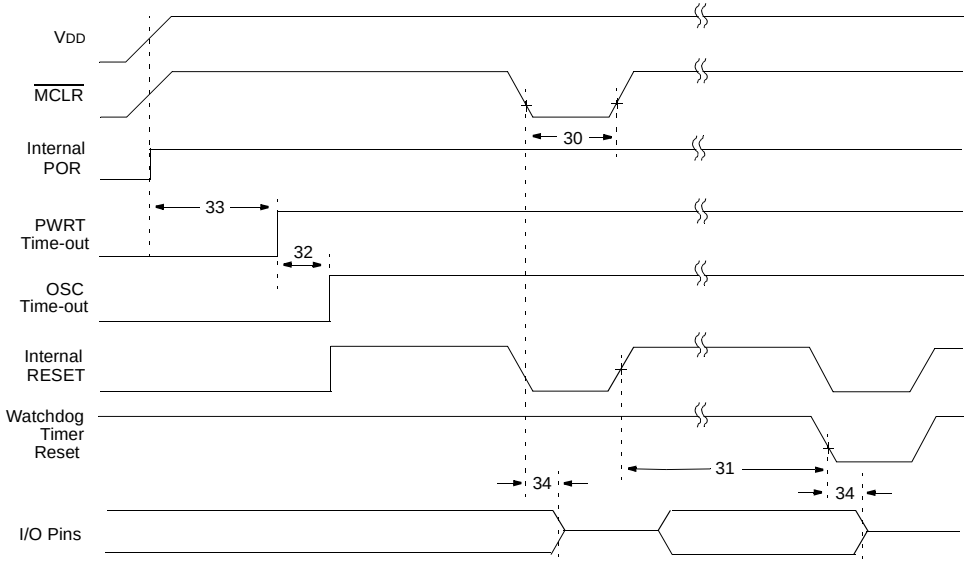
TABLE 17-5: INTERNAL RC OSCILLATOR CALIBRATED FREQUENCIES PIC16C781/782, DSTEMP

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40×C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 17-1.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Internal Calibrated RC Frequency	3.65	4.00	4.28	MHz	VDD = 5.0V
		Internal Calibrated RC Frequency	3.55*	4.00	4.31*	MHz	VDD = 2.5V

* These parameters are characterized but not tested.

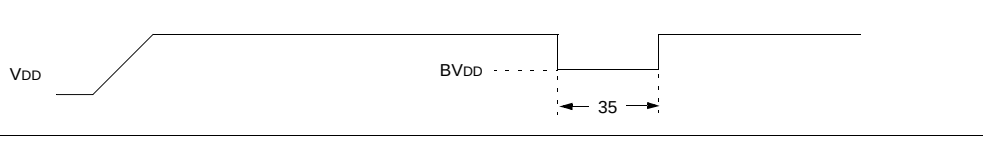
Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Refer to Figure 17-3 for load conditions.

FIGURE 17-7: BROWN-OUT RESET TIMING



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