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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c781-i-ss

2.7 PIR1 Register

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PERIPHERAL INTERRUPT REGISTER (PIR1 0Ch)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
LVDIF	ADIF	C2IF	C1IF	—	—	—	TMR1IF
bit7							bit 0

bit 7 **LVDIF:** Low Voltage Detect Interrupt Flag bit
1 = The supply voltage has fallen below the specified LVD voltage (must be cleared in software)
0 = The supply voltage is greater than the specified LVD voltage

bit 6 **ADIF:** Analog-to-Digital Converter Interrupt Flag bit
1 = An ADC conversion completed (must be cleared in software)
0 = The ADC conversion is not complete

bit 5 **C2IF:** Comparator C2 Interrupt Flag bit
1 = Comparator C2 input has crossed the threshold (must be cleared in software)
0 = Comparator C2 input has not crossed the threshold

bit 4 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Comparator C1 input has crossed the threshold (must be cleared in software)
0 = Comparator C1 input has not crossed the threshold

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.8 PCON Register

The Power Control (PCON) register contains two flag bits to allow determination of the source of the most recent RESET:

- Power-on Reset ($\overline{POR}$)
- External $\overline{MCLR}$ Reset
- Power Supply Brown-out ($\overline{BOR}$) Reset

The Power Control register also contains frequency select bits for the INTRC oscillator and the WDT software enable bit.

Note: $\overline{BOR}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{BOR}$ is clear, indicating a brown-out has occurred. The $\overline{BOR}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

Direction of Change	Typical Time Inactive	
	Minimum	Maximum
4 MHz → 37 kHz	100 μs	300 μs
37 kHz→4 MHz	1.25 μs	3.25 μs

Note: When changing the internal oscillator speed (i.e., the OSCF bit, INTRC mode), the processor will be inactive during the oscillator frequency change.

REGISTER 2-6: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	R/W-q	R/W-1	U-0	R/W-q	R/W-q
—	—	—	WDTON	OSCF	—	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled

bit 3 **OSCF:** Oscillator Speed INTRC Mode bit

1 = 4 MHz typical
0 = 37 kHz typical
All other oscillator modes (X = Ignored)

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit

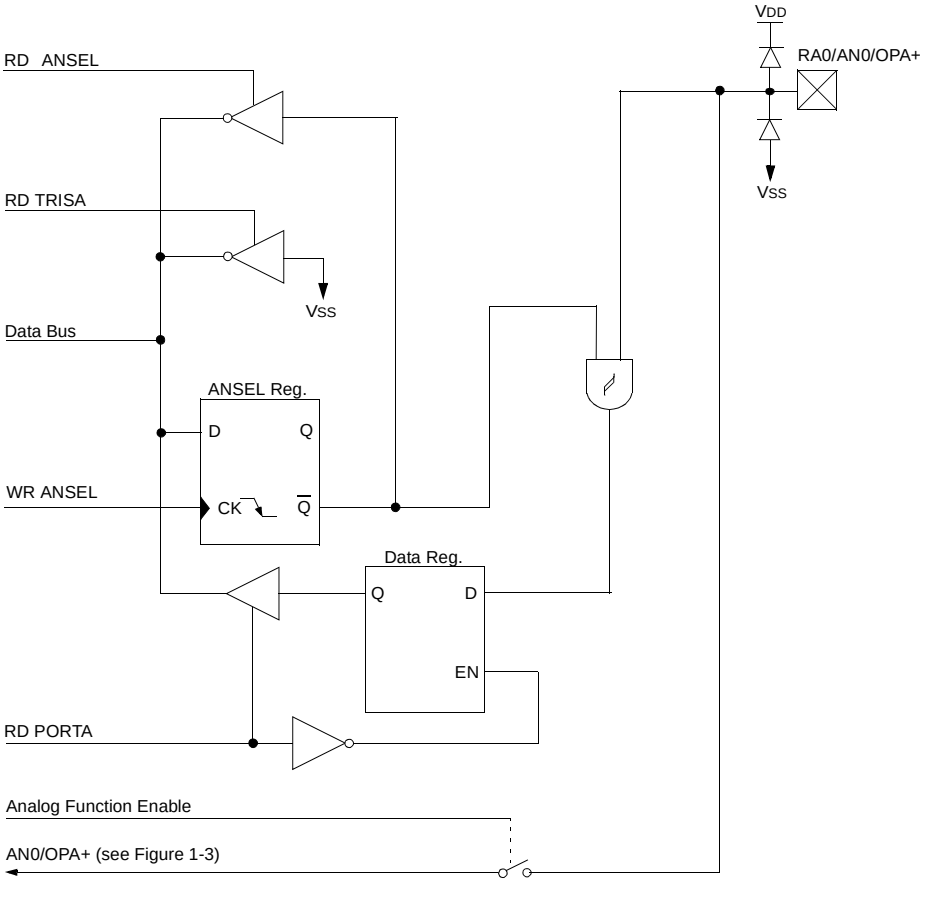
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred

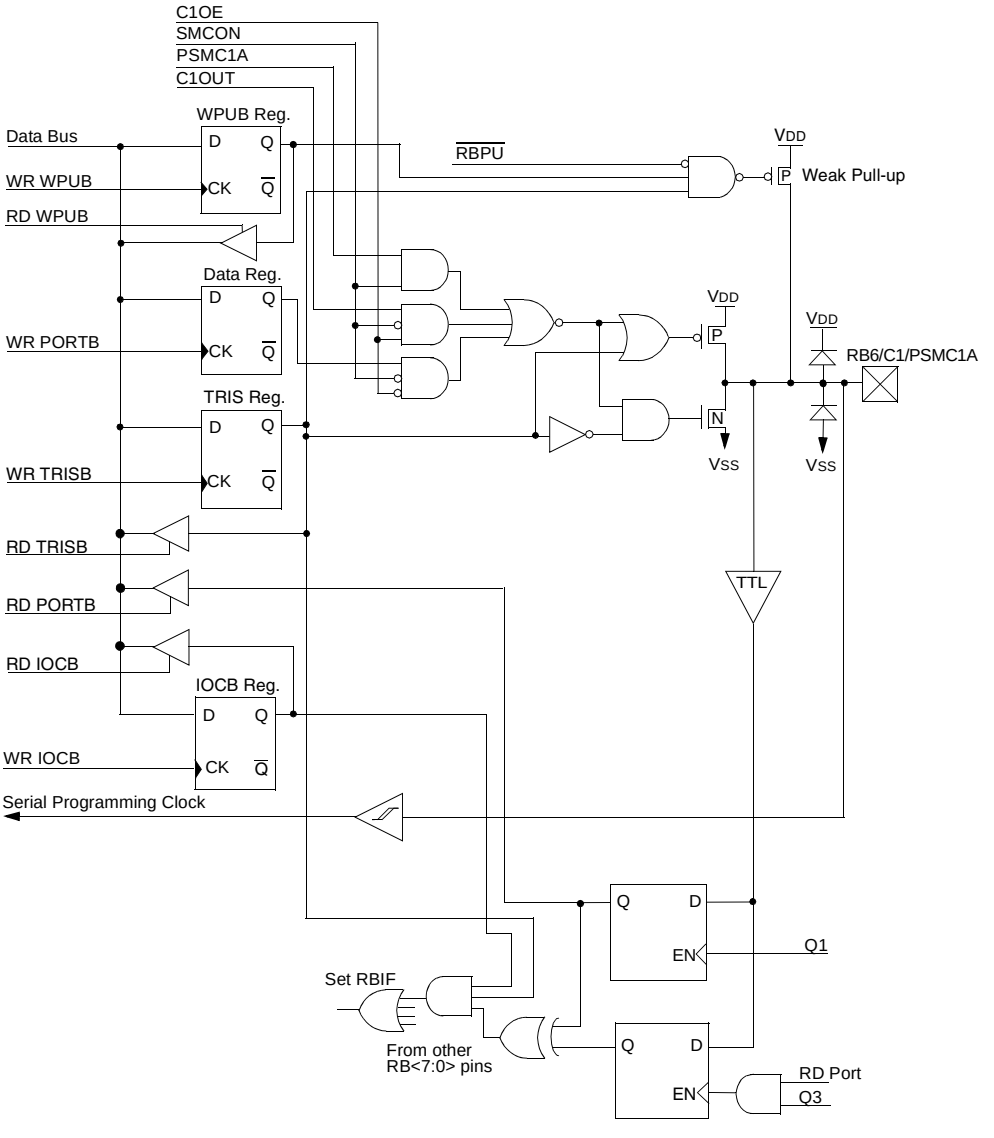
Legend:			
q = Value depends on conditions			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 3-1: BLOCK DIAGRAM OF RA0/AN0/OPA+ PIN



ANSEL<0>	TRISA<0>	FUNCTION	PORTA<0> READ
0	x	Digital In	Pin
1	x	Analog In	0

FIGURE 3-15: BLOCK DIAGRAM OF RB6/C1/PSMC1A PIN



PSMC SMCON	COMPARATOR C1OE	PORTB TRISB<6>	FUNCTION
x	x	1	Digital In
0	0	0	Digital Out
0	1	0	C1OUT
1	x	0	PSMC1A

NOTES:

4.0 PROGRAM MEMORY READ (PMR)

Program memory is readable during normal operation (full VDD range). It is read by indirect addressing through the following Special Function Registers:

- PMCON1: Control
- PMDATH: Data High
- PMDATL: Data Low
- PMADRH: Address High
- PMADRL: Address Low

When interfacing to the program memory block, the PMDATH and PMDATL registers form a 2-byte word, which holds the 14-bit data. The PMADRH and PMADRL registers form a 2-byte word, which holds the 12-bit address of the program memory location being accessed. Mid-range devices have up to 8K words of program EPROM with an address range from 0h to 3FFFh. When the device contains less memory than the full address range of the PMADRH:PMARDL registers, the Most Significant bits of the PMADRH register are ignored.

4.1 PMCON1 Register

PMCON1 is the control register for program memory accesses.

Control bit RD initiates a read operation. This bit cannot be cleared, only set, in software. It is cleared in hardware at completion of the read operation.

4.2 PMDATH and PMDATL Registers

The PMDATH:PMDATL registers are loaded with the contents of program memory addressed by the PMADRH and PMADRL registers upon completion of a Program Memory Read command.

REGISTER 4-1: PROGRAM MEMORY READ CONTROL REGISTER 1 (PMCON1: 18Ch)

R-1	U-0	U-0	U-0	U-0	U-0	U-0	R/S-0
Reserved	—	—	—	—	—	—	RD
bit7							bit0

bit 7 **Reserved:** Read as ‘1’

bit 6-1 **Unimplemented:** Read as '0

bit 0 **RD**: Read Control bit

1 = Initiates a Program memory read (read takes 2 cycles, RD is cleared in hardware)
0 = Reserved

Legend:			
S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

REGISTER 4-2: PROGRAM MEMORY DATA HIGH (PMDATH: 10Eh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8
bit7							bit0

bit 7-6 **Unimplemented:** Read as '0

bit 5-0 **PMD<13:8>:** Program Memory Data bits
The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

4.4 Program Memory Read With Code Protect Set

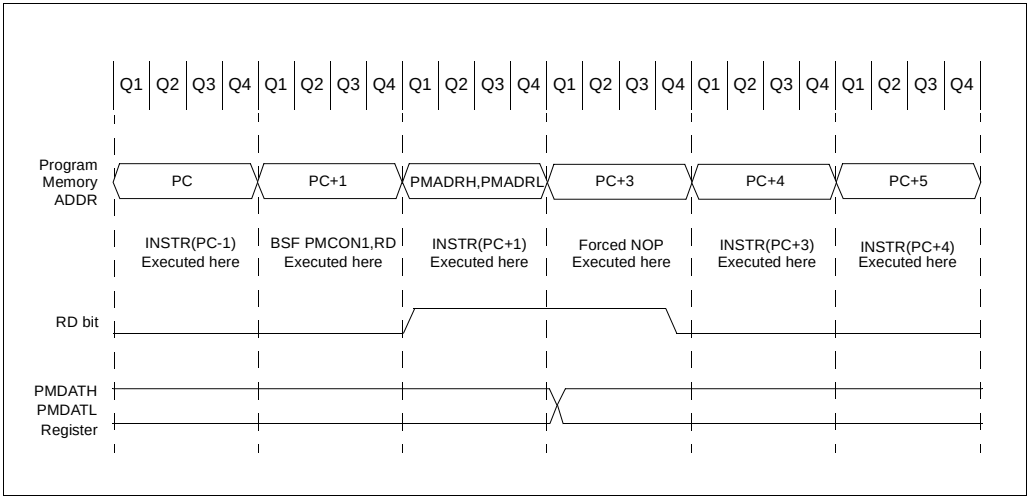
When the device is code protected, the CPU can still perform the program memory read function.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PMR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
10Ch	PMDATL	PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000 0000	0000 0000
10Dh	PMADRL	PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0	xxxx xxxx	uuuu uuuu
10Eh	PMDATH	—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8	--00 0000	--00 0000
10Fh	PMADRH	—	—	—	Reserved	Reserved	PMA10	PMA9	PMA8	---x xxxx	---u uuuu
18Ch	PMCON1	Reserved	—	—	—	—	—	—	RD	1--- ---0	1--- ---0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PMR.

FIGURE 4-1: PROGRAM MEMORY READ CYCLE EXECUTION



6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
  (two 8-bit registers:TMR1H and TMR1L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- External enable input ($\overline{T1G}$ pin with TMR1GE bit = 1)
- Option for Timer1 to use LP oscillator if device is configured to use INTRC w/o CLKOUT

Timer1 Control register (T1CON) is shown in Register 6-1.

Figure 6-2 is a simplified block diagram of the Timer1 module.

6.1 Timer1 Operation

Timer1 can operate in one of three modes:

1. 16-bit timer with prescaler.
2. 16-bit synchronous counter.
3. 16-bit asynchronous counter.

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI (RA6/OSC2/CLKOUT/T1CKI). In addition, the Counter mode clock can be synchronized to the microcontroller clock or run asynchronously.

In Counter and Timer modes, the counter/timer clock can be gated by the $\overline{T1G}$ input.

If an external clock oscillator is needed (and the microcontroller is using INTRC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note 1: In Counter mode, the counter increments on the rising edge of the clock.

EXAMPLE 6-1: TIMER1 INITIALIZATION

```
;* This code block will configure Timer1 for
;* Polling, Ext gate of int clk (Fosc/4), &
;* 1:1 prescaler.
;*
;* Wait for TMR1 overflow code included
;*
   BANKSEL  TMR1L           ; Select Bank 0
   CLRF     TMR1L           ; Clear TMR1 LSB
   CLRF     TMR1H           ; Clear TMR1 MSB
   MOVLW    B'01000000'     ; Gate, Ps 1:1
   MOVWF    T1CON           ; Int clk
   BSF      T1CON,TMR1ON    ; Enable timer

;*****************************************
;* Wait for TMR1 overflow

T1_OVFL_WAIT
   BANKSEL  PIR1            ; Select Bank 0
   T1_WAIT                  ;
   TBFSS    PIR1,TMR1IF     ; Overflow?
   GOTO     T1_WAIT         ; If 0, again

   BCF      PIR1,TMR1IF     ; Clear flag
```

9.1 Control Registers

The ADC module has three registers. These registers are:

- ADC Result Register: ADRES
- ADC Control Register 0: ADCON0
- ADC Control Register 1: ADCON1

The ADCON0 register, shown in Register 9-1, controls the operations and input channel selection for the ADC module. The ADCON1 register, shown in Register 9-3, selects the voltage reference used by the ADC module. The ADRES register, shown in Register 9-2, holds the 8-bit result of the conversion.

Additional information on using the ADC module can be found in the PIC Mid-Range MCU Family Reference Manual (DS33023) and in Application Note AN546 (DS00546).

9.1.1 ADCON0 REGISTER

The ADCON0 register, shown in Register 9-1, controls the following:

- Clock source and prescaler
- Input channel
- Conversion start/stop
- Enabling of the ADC module

Setting the ADON bit, ADCON0<0>, enables the ADC module. Clearing ADON disables the module and terminates any conversion in process.

The ADCS<1:0> bits (ADCON0<7:6>) determine the clock source used by the ADC module.

The CHS<3:0> bits (ADCON0<5:3,1>) determine the input channel to the ADC module. CHS<3> specifically determines whether the source is internal or external.

Setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) initiates the conversion process. The ADC clears this bit at the completion of the conversion process.

REGISTER 9-1: ADC CONTROL REGISTER 0 (ADCON0: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/S-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>:** ADC Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = ADRC (clock derived from a dedicated RC oscillator)

bit 5-3 **CHS<2:0>:** Analog Channel Select bits (select which channel to convert)

If CHS3 = 0:	If CHS3 = 1:
000 = channel 0 (AN0)	000 = VR
001 = channel 1 (AN1)	001 = VDAC
010 = channel 2 (AN2)	010 = Reserved. Do not use.
011 = channel 3 (AN3)	011 = Reserved. Do not use.
100 = channel 4 (AN4)	100 = Reserved. Do not use.
101 = channel 5 (AN5)	101 = Reserved. Do not use.
110 = channel 6 (AN6)	110 = Reserved. Do not use.
111 = channel 7 (AN7)	111 = Reserved. Do not use.

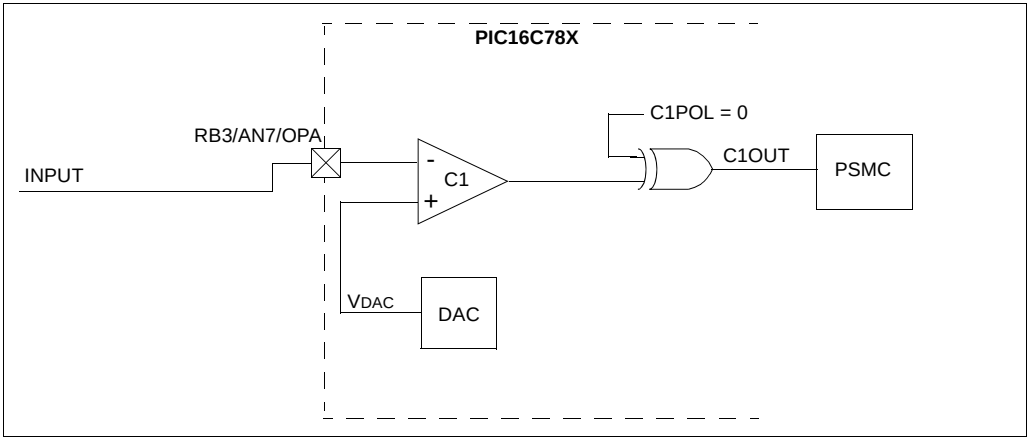
bit 2 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
0 = ADC conversion is not in progress (this bit is cleared by hardware when conversion is complete)

bit 1 **CHS3:** Analog Channel Select bit
1 = Internal channel selected for conversion
0 = External channel selected for conversion

bit 0 **ADON:** ADC On bit
1 = ADC enabled
0 = ADC disabled

Legend:			
S = Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 12-4: CONFIGURATION OF COMPARATOR C1 WITH DAC



EXAMPLE 12-2: PROGRAMMING C1 FOR PSMC FEEDBACK

```
;*  This code block will configure Comparator
;*  C1 for normal speed and output polarity,
;*  input on AN7, and Reference from the DAC

    BANKSEL     TRISA       ; Select Bank 1
    BSF         TRISB,RB3   ; RB3 as input
    BSF         ANSEL,AN7   ; Set RB3 as analog

    BANKSEL     DACON0      ; Select Bank 2
    CLRF        DAC         ; DAC=00h
    MOVLW       B'10000000' ; Enable, no out
    MOVWF       DACON0      ; DACREF = VDD
    MOVLW       DAC_VALUE
    MOVWF       DAC         ; Trip Level

    MOVLW       B'10001111' ; C1; no out,
    MOVWF       CM1CON0     ; VREF1, AN7
```

12.2.3 EXAMPLE: LOW POWER WINDOW COMPARATOR WITH INTERRUPT

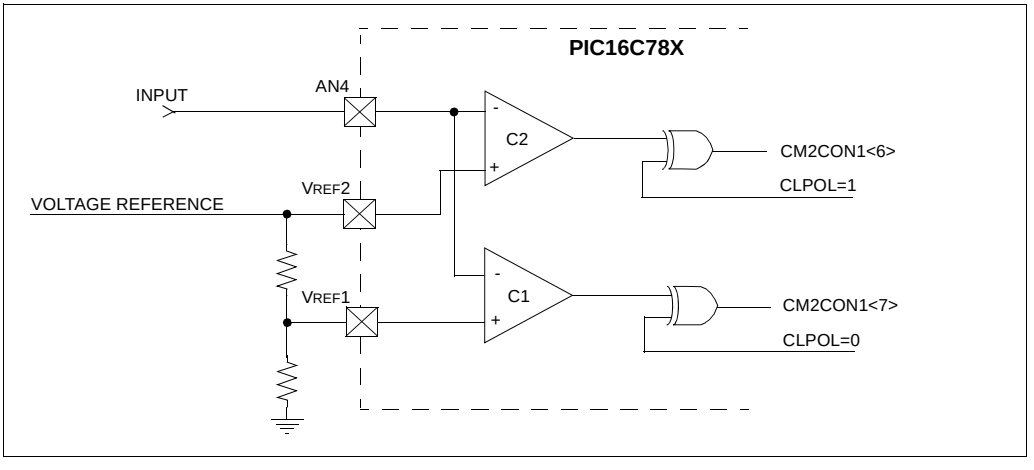
To form a low power window comparator, Comparators C1 & C2 are configured as follows:

- Common input RB0/INT/AN4/V_{REF}
- Separate external reference voltages
- Programmed for slow speed operation

In addition, the output of comparator C2 must be inverted for common polarity with C1.

A block diagram of the window comparator with external connections is shown in Figure 12-4.

FIGURE 12-5: WINDOW COMPARATOR WITH INTERRUPT



13.3 Configuration

The programmable nature of the PSMC lends itself to a wide variety of applications involving current or voltage management. The following examples are intended to provide suggested applications for the PSMC. The examples are not complete designs, but rather block diagrams of some potential applications of the PSMC. For a broader list of applications, including supporting math and firmware examples, please refer to Microchip web page for applicable Application Notes.

13.3.1 EXAMPLE BOOST LC SWITCHING POWER SUPPLY

In this example, the PSMC controls the boost configuration switching power supply in Figure 13-5.

The PSMC is configured as a two feedback loop PWM, current mode, switching power supply controller. The inner current feedback loops consist of:

- PSMC
- MOSFET driver
- Power MOSFET Q1
- Inductor L1
- Current transformer
- Comparator C1

The outer voltage feedback loop consists of:

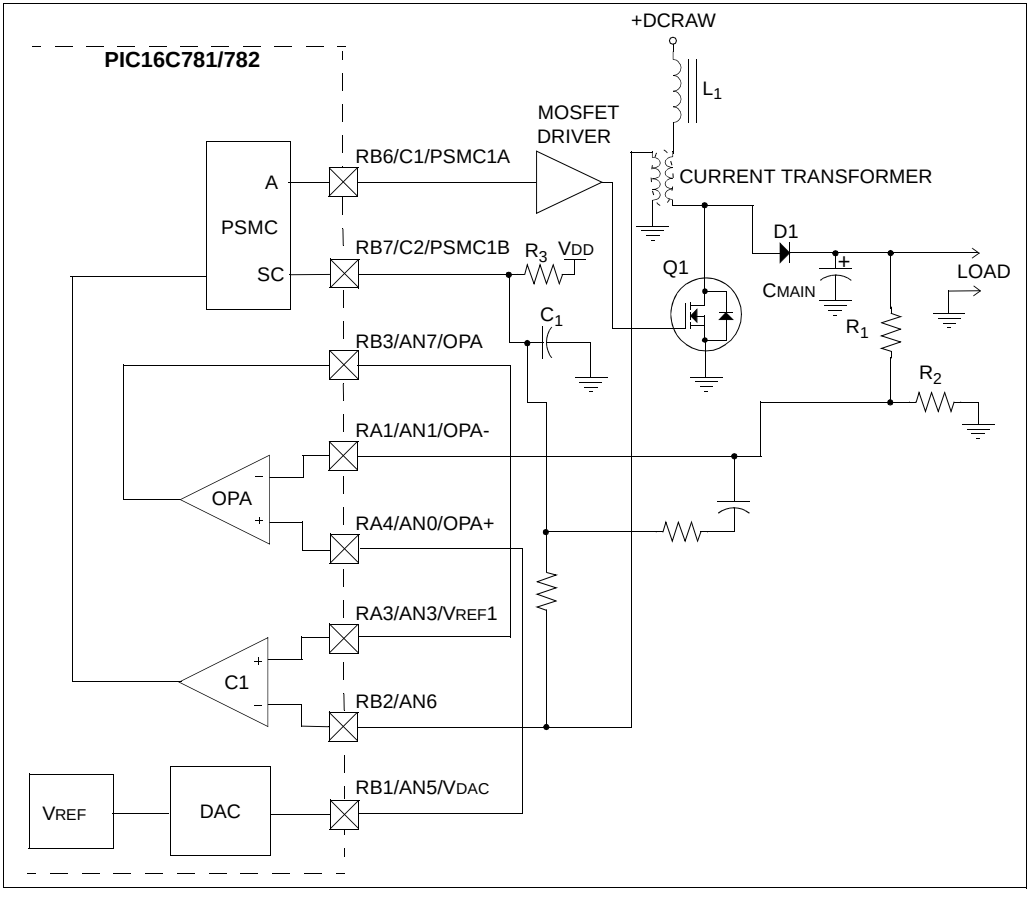
- Diode D1
- CMAIN
- OPAMP feedback filter
- DAC reference

The inner current loop is a pulsed current source driven by the PSMC. During the active phase of the output pulse, the inner loop builds up a current flow in inductor L1. The current in L1 is monitored by the current transformer. The output of the transformer is offset by the ramp from the slope compensation network R3/C1 and then fed into the comparator. When the voltage (proportional to the current flow in L1, offset by the slope compensation) exceeds the error voltage from the OPAMP, Q1 is turned off and L1 discharges through D1 into CMAIN for the remainder of the period.

The outer voltage loop monitors the output voltage across CMAIN using R1/R2. The reference voltage from the DAC is subtracted, generating the raw error voltage. The raw error voltage is filtered by the OPAMP and routed to Comparator C1 in the inner current loop.

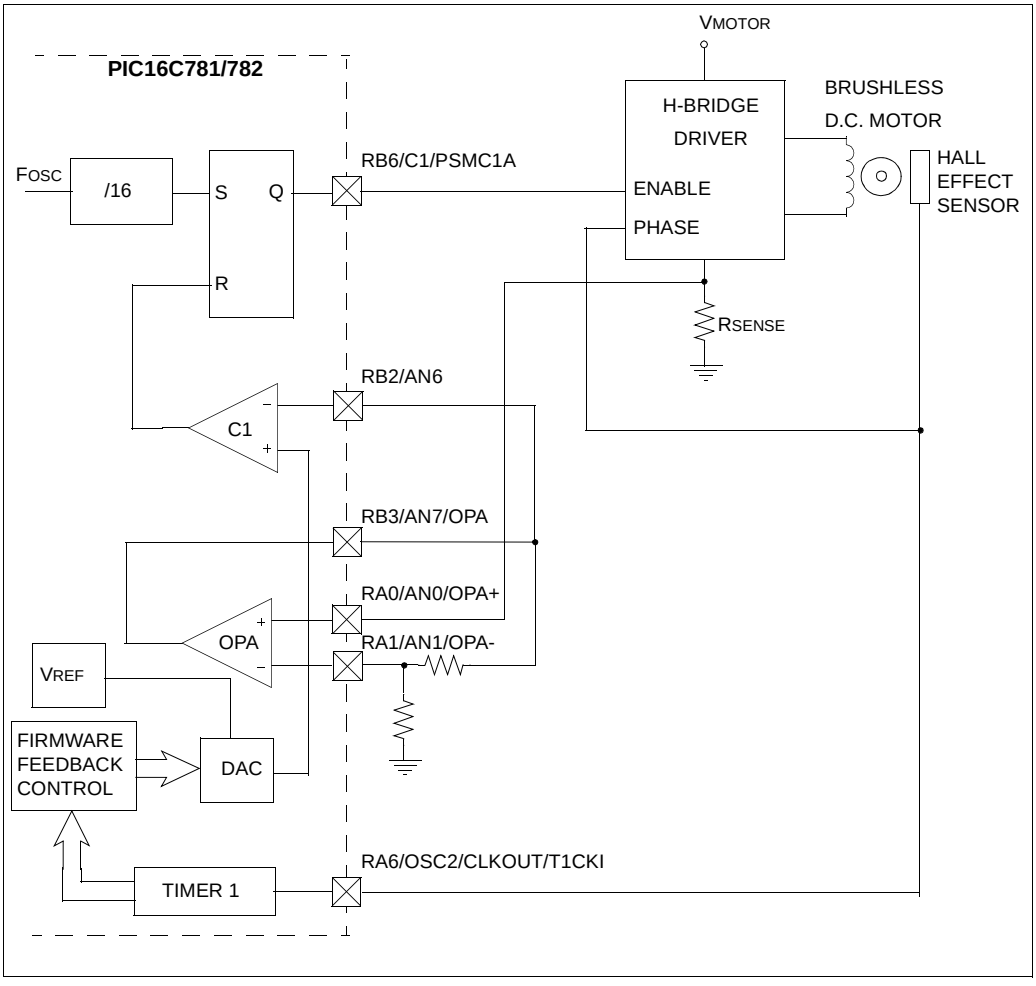
The phase compensation output of the PSMC acts to improve loop stability by adding a pseudo-ramp waveform to the current sense transformer feedback in the inner loop. In conditions where the charge phase of the cycle is greater then 50%, the increased current feedback reduces the current charge in L1, slowing the charging of CMAIN. The result is a reduction in the overall loop gain for duty cycles of >50%, maintaining loop stability.

FIGURE 13-5: EXAMPLE BOOST CONFIGURATION LC SWITCHING POWER SUPPLY



Note:	The OPAMP, Comparator and DAC must be configured, prior to enabling the PSMC to prevent unpredictable operation which may stress the power MOSFET transistors.

FIGURE 13-7: EXAMPLE BRUSHLESS D.C. MOTOR CONTROL



REGISTER 14-2: POWER CONTROL REGISTER (PCON: 8Eh)

U-0	U-0	U-0	R/W-q	R/W-1	U-0	R/W-q	R/W-x
—	—	—	WDTON	OSCF	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **WDTON:** WDT Software Enable bit

If WDTE bit (Configuration Word <3>) = 1:
This bit is not writable, always reads '1'

If WDTE bit (Configuration Word <3>) = 0:
1 = WDT is enabled
0 = WDT is disabled and cleared

bit 3 **OSCF:** Oscillator Speed bit (pending on new internal oscillator decision)

INTRC mode:
1 = 4 MHz typical
0 = 37 kHz typical

All other oscillator modes:
Ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
x = Bit is unknown	'q' = Value depends on condition	

TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Bit Significance
0	1	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP

RRF **Rotate Right f through Carry**

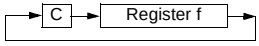
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped.

SUBLW **Subtract W from Literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.

XORLW **Exclusive OR Literal with W**

Syntax: [*label*]

Operands: $0 \le k \le 255$

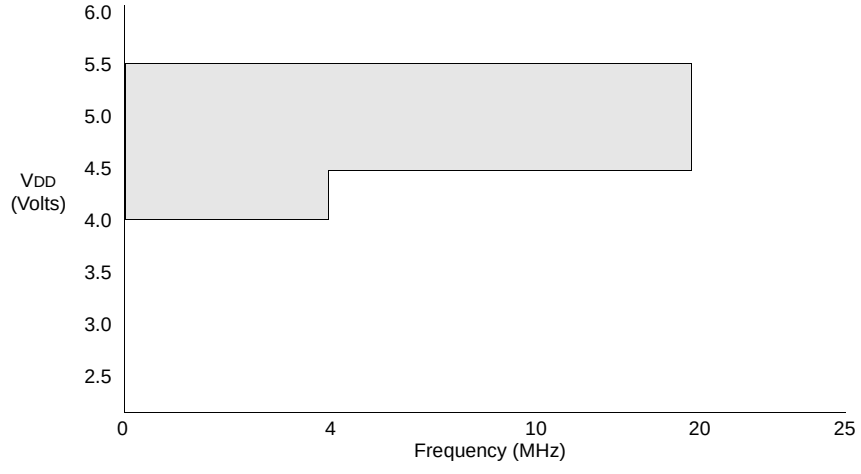
Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

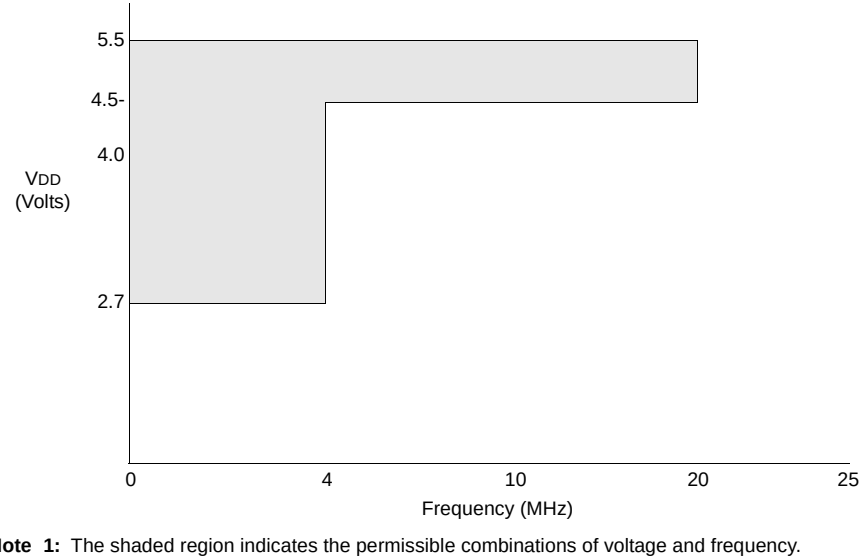
XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

FIGURE 17-1: PIC16C781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: PIC16LC781/782 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

17.1 DC Characteristics: Power Supply

TABLE 17-1: DC CHARACTERISTICS: PIC16C781/782, DSTEMP (INDUSTRIAL)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	4.0 4.5	— —	5.5 5.5	V —	XT, EC, RC, INTRC Oscillator HS Oscillator
D001A	VDD	**Supply Voltage** (DSTEMP)	2.7 4.5	— —	5.5 5.5	V V	XT, EC, RC, INTRC Oscillator HS Oscillator
D002*	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	TBD	—	V	See section on Power-on Reset for details
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details. PWRT enabled
D010	IDD	**Supply Current(2)**	— — — —	TBD TBD TBD TBD	TBD TBD TBD TBD	mA mA mA mA	FOSC = 20 MHz, VDD = 5.5V* HS Oscillator FOSC = 20 MHz, VDD = 4.5V HS Oscillator FOSC = 4 MHz, VDD = 4.0V* XT, RC w/CLKOUT FOSC = 32 kHz, VDD = 4.0V LP Oscillator
D020 D020A	IPD	**Power-down Current(3)**	— —	TBD 1.5	TBD 19	µA µA	VDD = 5.5V VDD = 4.0V
	IOPA	**Operational Amplifier**	—	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, GBWP = 0 VDD = 5.0V, GBWP = 1
	IVC*	**Voltage Comparators C1 and C2**	— —	TBD TBD	TBD TBD	mA mA	VDD = 5.0V, VID>100 mV C1SP = 0 VDD = 5.0 , VID>100 mV C1SP = 1
	IADC*	**Digital to Analog Converter (DAC)**	—	TBD	TBD	mA	VDD = 5.0V
D021	IWDT*	**Watchdog Timer**	—	TBD	TBD	mA	VDD = 4.0V
D026	IAD*	**Analog-to-Digital Converter (ADC)**	—	TBD	TBD	mA	VDD = 5.5V, ADC not converting
	IPLVD*	**Programmable Low Voltage Detect**		TBD	TBD	mA	VDD = 4.0V
	IPBOR*	**Programmable Brown-out Reset**		TBD	TBD	mA	VDD = 5.0V
1A	FOSC	**LP Oscillator, Operating Freq.** **INTRC Oscillator Operating Freq.** **XT Oscillator Operating Freq.** **HS Oscillator Operating Freq.**	9 — — 0 0	— 4 37 — —	200 — — 4 20	kHz MHz kHz MHz MHz	All temperatures All temperatures, OSCF = 1 All temperatures, OSCF = 0 All temperatures All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins configured as inputs, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins configured as iputs and tied to VDD or VSS.

17.5 Comparators

TABLE 17-10: DC CHARACTERISTICS: VOLTAGE COMPARATORS C1 AND C2

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Input Offset Voltage	V_{OS}	TBD TBD	±1 ± 2.5	TBD TBD	mV mV	C1SP = 1, C2SP = 1 C1SP = 0, C2SP = 0
	Input Current and Impedance Input Bias Current Input Offset Bias Current	 I_B I_{OS}	 TBD —	 — TBD	 — TBD	 nA nA	
	Common Mode Common Mode Input Range Common Mode Rejection	 V_{CM} CMR	 V_{SS} —	 — 70	 V_{DD}-1.4V	 V dB	 V_{DD} = 5V V_{CM} = V_{DD}/2, Frequency = DC
	Open Loop Gain DC Open Loop Gain	 A_{OL}	 —	 90	 —	 dB	
	Power Supply Rejection	PSR	—	TBD	—	dB	V_{DD} = 5V

TABLE 17-11: AC CHARACTERISTICS: COMPARATORS C1 AND C2

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated): V_{DD} = 2.7V to 5.5V, T_A = 25°C, V_{CM} = V_{DD}/2 Operating Temperature -40°C to +85°C for Industrial				
Param No.	**Parameters**	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
	Response Time Response Time	 t_r	 —	 75	 —	 ns	 V_{DD} = 5V, C1SP = 1, C2SP = 1, Comparator output signal is for internal use only, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	0.5	—	µs	V_{DD} = 5V, C1SP = 0, C2SP = 0, Comparator output signal is for internal use only, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	100	TBD	ns	V_{DD} = 5 , C_L = 100 pF, C1SP = 1, C2SP = 1, Comparator output is available on I/O pin, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
		t_r	—	0.5	TBD	µs	V_{DD} = 5 , C_L = 100 pF, C1SP = 0, C2SP = 0, Comparator output is available on I/O pin, Input overdrive = 10 mV, step = 110 mV, V_{CM} = V_{DD}/2.
	Turn On Time	T_{ON}	— —	10 TBD	TBD TBD	µs µs	C1SP = 0, C2SP = 0, V_{DD} = 5V C1SP = 1, C2SP = 1, V_{DD} = 5V

18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g., outside specified V_{DD} range.). This is for information only and devices are ensured to operate properly only within the specified range. The data presented in this section is a statistical summary of data collected on units from different lots over a period of time.

Standard deviation is denoted by sigma (σ).

Typ or Typical represents the mean of the distribution at 25°C.

Max or Maximum represents the mean +3σ over the temperature range of -40°C to 85°C.

Min or Minimum represents the mean -3σ over the temperature range of -40°C to 85°C.

Graphs and Tables are not available at this time.